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Principles and Designs for Self-Powered Microsystems

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Preface

Emerging ultra-low power applications such as wireless sensor nodes and implantable biomedical devices employ sophisticated energy harvesting techniques to extract power from the ambient environment. However, the power extracted can fluctuate considerably based on the intensity and availability of the power sources. Thus, modern self-powered devices require low power and efficient power converters to regulate the harvested energy appropriately, in order to effectively extend their operating lifetime.

Reconfigurable switched-capacitor (SC) DC–DC power converters are tailored to power these applications, due to advantages such as monolithic implementation, low power and low cost operation. Advanced reconfigurable charge pumps can optimize their operating structure 'on-the-fly' to provide various conversion gains. This can optimize the efficiency and provide a large dynamic range of output voltages. Moreover, interleaved charge pump topologies can minimize the output voltage ripples, enhance the load regulation and improve the robustness of self-powered devices. Hence, sophisticated modeling techniques, control algorithms, circuit design principles are urgently required to enable the development of state-of-the-art SC power converters, thereby advancing the growth of self-powered devices.

To cater to this need, this book combines in-depth theoretical analyses and principles with practical power IC designs, presenting a comprehensive study on state-of-the-art SC power converters. Each chapter presents several case studies and investigates various practical implementation issues in SC DC–DC converters. This will aid not only in validating the underlying fundamental principles, but will also promote the understanding of actual power IC chip designs. As a result, this book is jointly targeted towards university researchers, students and practicing industry design engineers.

This book provides an opportune venue to present key SC power converter principles and practical designs. Chapter 1 presents fundamental concepts in power management, energy harvesting and power converter designs. Chapter 2 addresses device level concepts in power converter designs. This includes a detailed discussion on several devices used in the field of power electronics such as power diodes, MOSFETs, BJT, IGBT and thyristors. Following this, Chap. 3 introduces

the premise behind fundamental charge pump topologies and their designs. The chapter also discusses on-chip implementation issues, such as integrated capacitors and power switches. Chapter 4 focuses on various power loss mechanisms in charge pumps, in order to better understand the efficiency optimization of SC power converters. The chapter investigates mechanisms causing switching power loss, conduction power loss, reversion and redistribution power loss in modern charge pumps. In Chap. 5, various state-of-the-art reconfigurable SC power converters are introduced. This chapter includes an in-depth discussion on reconfigurable charge pump topologies, corresponding control schemes and various case studies. Interleaved SC power converter designs are then presented in Chap. 6. Through interleaving regulation schemes, these power converters are capable of improving the output voltage ripples, input current ripples and the load regulation performance. Lastly, Chap. 7 presents the modeling and design of SC power converters in z-domain. By modeling the transfer function of the power stage, corresponding feedback controller and compensation circuits can be designed to better understand and further improve system closed-loop operation.

The work presented in this book is due to the research outcomes from current members from the Integrated Systems Design Laboratory (ISDL) at the University of Texas at Dallas and past alumni from the University of Arizona. The authors would like to acknowledge the contributions of Dr. Ling Su, Dr. Inshad Chowdhury, Minkyu Song, Mohankumar Somasundaram, and Chen Zheng.

Contents

Chapter 1
Fundamental Concepts

1.1 Background

Over the last decade, the semiconductor industry has experienced phenomenal growth, which has resulted in unprecedented research and technological developments in numerous domains of science and engineering. As per Moore's Law, the emergence of the nanometer generation of very-large scale integrated (VLSI) systems has led to chip densities of over a million transistors per square millimeter, which can operate at extremely high frequencies. This rapid growth has culminated in significant performance gains and breakthroughs in a plethora of fields ranging from advanced computing platforms, to communication, security, healthcare, biomedical systems and ultra-low power devices such as wireless micro-sensors. However, this tremendous growth has incurred extremely high levels of power dissipation, resulting in an energy crisis in modern ICs. High power dissipation levels also leads to significant heat generation, increasing risk of transistor breakdown effects. This places a tremendous stress on corresponding cooling and packaging solutions, thereby adding to size, cost and weight of the entire system. Moreover, the energy crisis is further exacerbated by a much slower pace in battery technology development.

In order to overcome the aforementioned crisis, advanced power management techniques are urgently required. It is expected that future VLSI systems should continuously monitor its own operating conditions and optimize its parameters including power dissipation. The associated power management techniques are applied into the system, circuit and/or device level, in order to tune in the parameters such as supply voltages, clock frequencies, biasing conditions, active/sleep time durations, critical path delays, etc. These techniques minimize energy consumption while maximizing the operation lifetime, by meeting necessary performance constraints. One representative technique is *dynamic power management*, wherein the device is shut down during periods of inactivity [1–3]. Other more sophisticated power management techniques exist, such as power moding, where each device is operated in one of several functional modes depending on its

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instantaneous workload. Among these, the most effective one is recognized as *dynamic voltage/frequency scaling* (DVFS) [4–8]. In this technique, the power delivered to a device is adaptively varied based on the instantaneous workload. This is achieved by continuously adjusting the supply voltages and operation frequencies to their optimal values. This leads to maximized power savings due to their quadratic and linear dependency on dynamic power, respectively.

Power management techniques require corresponding hardware enabling circuits, which directly influence the operation and performance of VLSI systems. As major power flow usually passes through power devices in these circuits, they should operate with high efficiency over a wide input and output voltage and power ranges, as determined by the working environment, energy sources and power management techniques. In addition, low volume and cost are highly desirable.

1.2 Renewable Energy Harvesting

Traditional electronic devices employ primary batteries as their main energy resource, as they require little or no environmental calibration, they do not depend on ambient conditions and have a very predictable behavior. However, batteries are associated with a very limited operation lifetime and require constant replacements. Further exacerbating this issue is that due to ageing effects, the energy stored in a battery is not completely usable and in the worst case, can be even lower than half the battery capacity [9]. Secondly, as a result of their bulky size, the use of batteries leads to an increase in system volume. This is undesirable for microsystems that place strict requirements on small form factor, such as biomedical implants and wireless sensor nodes. Moreover, battery technology has not improved with respect to energy density or size over the last decade, especially for low power applications. Lastly, the use of batteries has severe environmental implications, since they typically employ toxic metals as the chief constituent material of their electrodes. For example, Ni–Cd batteries employ nickel and cadmium metals, which are both toxic and generate hazardous residues. Moreover, their inadequate disposal is a potential source of contamination in soil and water bodies [10].

To overcome these drawbacks and to extend the operation lifetime, emerging electronic devices are becoming self-powered. These devices employ advanced energy harvesting techniques to supplement the battery or even operate as the entire power supply. To implement this, modern devices exploit the availability of the abundance of energy resources in the ambient environment, through sources or mechanisms such as solar, vibration energy, heat, etc. Corresponding harvesting and storage techniques are employed to extract and store this as useful electrical energy. Since many of these energy sources are ubiquitous, device operation lifetime can be largely enhanced. This section discusses the most widely used energy harvesting methods in modern self-powered, low power devices.

1.2.1 Solar Energy Harvesting

Solar energy is one of the most important and abundant renewable energy sources on earth. While a wide variety of harvesting modalities are now feasible, solar energy harvesting through photovoltaic conversion provides the highest power density and ubiquitous availability [9]. Moreover, since a DC voltage is directly available from solar cells, additional rectification circuits are not required. Solar energy is also clean and free of emissions, since it does not produce pollutants or byproducts that are harmful to the environment. Thus, these advantages make solar energy harvesting very popular for portable applications, such as wireless sensor networks, which are frequently operated in outdoor environments and have power consumption requirements in the order of mW.

The design of a solar energy harvesting system is quite sophisticated and involves complex tradeoffs due to the interaction of various factors. Firstly, the *I–V* characteristics define key parameters of the solar cell, such as the open circuit voltage, the short circuit current and the *maximum power point* (MPP). The MPP is the operating point at which the harvested power of the system is maximized. However, the *I–V* characteristics of the solar cell are strongly dependent on environmental conditions. For example, a change in the irradiation levels significantly alters the short-circuit current, while a change in ambient temperature affects the open-circuit voltage. This significantly varies the MPP of the solar cells, making it quite challenging to effectively harvest energy in a non-stationary environment. Secondly, under partial shading conditions, it is also possible for the *I–V* curves to have multiple local maxima. However, there still exists only a single global MPP. Thus, to ensure that the energy efficiency and operating lifetime of the entire system is optimal, the solar energy harvesting system requires sophisticated power tracking, conditioning and management modules. This involves a cross-layered design effort, from the device level to the circuit and system level.

1.2.2 Vibration Energy Harvesting

Another popular energy harvesting technique is to extract energy from vibrations, which are pervasive to all mechanically moving sources. It is possible to convert and condition vibration energy into electrical energy by harnessing the damping forces produced by piezoelectric materials [11, 12], electric fields [13, 14] or magnetic fields [15, 16]. In piezoelectric energy harvesting systems, mechanical strains due to pressure, vibrations or force leads to the generation of a surface charge. An oscillating mechanical strain leads to this charge being accumulated periodically. This results in the formation of an AC voltage across the piezoelectric device, which can be subsequently harnessed. In inductive systems, the mechanical motion can be applied to a magnet moving through a wound coil. The coil cuts through the magnetic flux of the magnet periodically, thereby creating an induced

voltage at the terminals of the coil. Lastly, electrical energy can also be harvested from mechanical motion through the electric fields between a parallel plate capacitor. Typically, charge is injected into the capacitor at maximum capacitance and pulled off at minimum capacitance. Between these points, external vibrations separate the plates against their attractive force, performing work on the injected charge, which is then harvested.

While significant research progress has been observed towards developing vibration energy harvesting methods, challenges continue to exist. Firstly, power densities achieved through current harvesting techniques are quite low at low frequencies and is traditionally limited by the vibrating kinetic source. In practical systems, typically only a small percentage of the initial mechanical energy can be effectively converted into viable electrical energy. Moreover, most designs are extremely sensitive to frequencies and can provide peak power only in a narrow bandwidth. While a network of energy harvesting systems operating over multiple vibration bands can be employed, this decreases the overall power density of the device. Another design challenge in vibration energy harvesting is associated with subsequent power conditioning systems. Since this energy harvesting method essentially generates an AC signal, it requires additional circuitry for rectification.

1.2.3 Thermal Energy Harvesting

A third method to harvest energy is to exploit temperature differences in the environment, through the use of thermoelectric generators (TEGs) [17]. A TEG converts thermal energy in the form of temperature differences into electrical energy and vice versa. The fundamental physical process involved in thermoelectrics is the *Seebeck* effect, which is observed in devices known as thermocouples [18]. A thermocouple is composed of an n-type material electrically connected in series with a p-type material. When a temperature difference applied across this material, charge carriers diffuse across the device, from the hot end to the cold end. This leads to a buildup of charge carriers at the cold end, resulting in an electrostatic potential. Equilibrium is reached when the thermal potential for diffusion equals the electrostatic repulsion due to the net charge at the cold end. The voltage that is generated is then harvested, conditioned and used to power load applications.

The implementation of thermal energy harvesting systems involves significant system and circuit design challenges. Firstly, the output voltages that are generated by TEGs are quite low, of the order of tens of millivolts. It is not possible to start up and ensure normal device operation directly from these low voltages. Typically, CMOS circuits require significantly higher voltage levels to guarantee robust operation. Moreover, changing external conditions cause the voltage and power generated by the TEG to vary considerably. This necessitates the development of efficient power conditioning and management systems that can extract the maximum power from these devices. Furthermore, the low power densities extracted

from TEGs necessitates aggressive low power circuit design techniques and efficient power delivery mechanisms, in order to meet system level power constraints.

1.2.4 Other Energy Harvesting Alternatives

Apart from the aforementioned energy harvesting methods, other alternatives exist. One alternate method is RF wireless powering [19]. This energy harvesting method involves the use of an inductive link between two resonant systems. An external electrical power source is used to drive a primary coil loop, which couples RF energy into a secondary loop through magnetic coupling. This is different from inductive based vibration energy harvesting technique, which converts mechanical energy imposed on a magnet moving through a coil, into an electrical current. RF wireless powering has become popular in advanced applications such as embedded biomedical systems, for in vivo diagnostic devices. In such devices, the secondary coil is implanted within human tissue and receives RF power from an external coil. However, numerous design challenges exist in this power delivery modality. Primarily, low power inductive links are typically characterized by very unfavorable coil coupling conditions. This can either be due to a large physical separation between the two coils or due to a very small coil diameter. The coupling factor can also vary significantly and unpredictably, with variations of the order of one decade, due to coil misalignments. This severely affects the coupled voltage and power levels, thereby placing challenging design constraints on corresponding power management circuits.

Another type of alternative energy harvesting method is from radioactive sources [20]. Radioactive materials have been used as a large scale energy source for decades. Recently, power sources for wireless sensor nodes that employ the radioactive decay of elements such as nickel (Ni) have been developed [21]. However, the use of such radioactive materials can pose a serious health and environmental hazard. Moreover, while the reported energy density numbers have been quite attractive, effective methods of converting this power to electrical energy, especially at small scales do not exist. Thus, currently the efficiencies of such methods are quite low and require further research and development.

1.3 Power Conditioning and Management for Energy Harvesting Applications

In contrast to traditional electronic devices, self-powered systems must ensure the reliability of energy harvesting, storage and facilitate efficient power conditioning and management. This introduces several new challenges that are essential for robust and efficient operation.

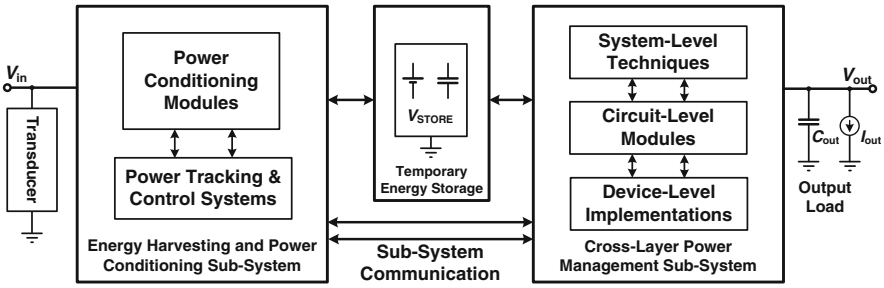

Fig. 1.1 Block diagram of an energy harvesting microsystem

The block diagram of an energy harvesting microsystem is illustrated in Fig. 1.1. The voltages generated and power extracted from energy harvesting modalities is typically low and fluctuate largely due to the varying intensity and availability of the energy sources. As a result, it cannot be directly used by load devices and requires suitable power conditioning circuits. These circuits guarantee the functionality and efficiency of the energy harvesting technique, through desired power conversion and voltage regulation. The energy extracted from the ambient environment is then stored in a storage device such as a rechargeable battery, supercapacitor or fuel cell, before being used to power load applications. However, to ensure the efficient operation of the load device, advanced power management schemes are essential. These schemes function at the system level, circuit or the device level to enhance the operation lifetime and robustness, and minimize the power consumption of the load. Hence, this section discusses each of these sub-systems and their roles in energy harvesting microsystems.

1.3.1 Power Conditioning

The primary role of power conditioning circuits is to guarantee the functionality of energy harvesting from renewable energy sources. These circuits ensure that the harvested energy, which is typically unusable in its direct form, is appropriately conditioned so that it can subsequently be used to power load devices. As a result, their designs are closely dependent on the harvesting modality being exploited. For example, in solar energy harvesting systems, the voltages generated by the PV cell can vary largely based on the environmental conditions. Power conditioning circuits ensure that the power generated by solar cells is harvested and converted to a desired fixed voltage. On the other hand, due to the nature of vibration based energy harvesting, the voltages generated are alternating in nature. Power conditioning circuits provide necessary voltage rectification, in order to convert the AC voltage into a DC value. For thermal energy harvesting, the generated voltages are quite low, typically of the order of tens of millivolts. In such harvesting methods, these circuits boost the harvested voltage to desired levels.

Since the power levels generated through energy harvesting is typically low, power conditioning circuits rely on additional control techniques and strategies to enhance the system efficiency. Depending on the type of harvester being used, various strategies can be employed, such as tracking the MPP in solar cells, resonant frequency tuning in piezoelectric devices, thermal impedance matching in TEGs and so on. In each of these strategies, power tracking circuits are used to monitor ambient environmental conditions, based on which the optimal operation points are identified. This enables power conditioning circuits to present an optimal electrical load by working at the desired operating point, thereby ensuring maximum power extraction from the energy transducers.

From Fig. 1.1, it can be seen that the energy extracted from the transducer is temporarily stored, before being further processed and supplied to the load applications. The storage element can either be a rechargeable battery, supercapacitor or fuel cell. Batteries are a relatively mature technology and have a higher energy density than supercapacitors. On the other hand, supercapacitors have higher power densities and are ideal for handling short bursts of power demands that are observed in self-powered applications. Moreover, supercapacitors are also more power-efficient and offer higher operation lifetime in terms of charge–discharge cycles. However, they undergo leakage, which prevents their use for long term energy storage. While it is possible to implement a tiered energy storage mechanism, this leads to the tradeoff in the efficiency of the energy conditioning and power management circuitry, due to the increased overhead of energy storage management. Lastly, depending on their internal chemistry, the storage mediums are associated with unique characteristics. They differ with respect to parameters such as charging current requirements, self-discharge rates, ageing effects, temperature dependencies, etc. [9]. Thus, to achieve synergetic operation, high efficiency and robustness of the overall energy harvesting system, the design of power conditioning circuits have to be geared towards application-specific requirements, from both the energy transducers and storage media.

1.3.2 Power Management

Apart from the power conditioning systems, modern self-powered electronic devices require cross-layer power management to achieve efficient operation and long system runtime. From the system level, in order to effectively utilize the limited harvested energy, these devices are operated under various different power management techniques such as DVFS or dynamic power management. These techniques are highly application-dependent and utilize parameters such as processor workload, timing deadlines, data interdependencies, and so on, in order to determine optimal operation voltages and speeds. Hence, this requires the availability of unique voltage levels, which are different from the battery voltage, to ensure that the power and energy consumption is minimized.

From the circuit level, state-of-the-art self-powered embedded and portable systems are an integrated collection of numerous, highly sophisticated analog and digital modules. Depending upon its function and design, different modules such as the processor, radio transmitter and receivers, power amplifiers, etc., operate at different optimal supply voltages. Thus, from circuit function perspective, such a system requires multiple voltage levels delivered by corresponding power management systems.

As a result, advanced power management systems are critical for modern self-powered devices and can be classified as system level, circuit level and device level power management.

1.3.2.1 System Level Power Management

Power management is achieved at the highest level of abstraction through system level optimization techniques. These methods are algorithmic-based and dependent on the type of application being catered to. One of the most important system level algorithms for power management is dynamic power management (DPM). DPM is a design methodology that achieves energy-efficient operation by selectively turning off system components when they are idle and by operating them at peak performances when active. The fundamental premise of DPM is that most systems experience non-uniform workloads during their run time, which is valid for both systems operating in isolation and when inter-networked. Such power management schemes are widely employed in low duty cycle electronic circuits, such as RF transceivers and other communication circuits. These devices are operated in a *time-division multiple-access* mode, which is also known as a *burst mode*. In this mode, the system is powered only when data is transmitted and received in very small time slots. In order to maximize battery lifetime, DPM based power management algorithms have to ensure that the standby power of the computation and communication circuits is minimized. To solve such issues, several workload observation and prediction-based algorithms have been developed which are capable of predicting periods of inactivity, with a certain degree of confidence. Hence, by turning off system components, power consumption can be significantly reduced during these periods of inactivity.

While DPM based techniques are beneficial for systems that are inactive for a sufficiently long period of time, in certain applications, tasks are fine-grained and will have relatively short idle period. Such applications will not benefit from shutting down system components temporarily between different tasks, which are traditionally associated with additional energy overheads and delays. To overcome these drawbacks, several other system level power management techniques have been developed, with the most widely used being dynamic voltage/frequency scaling (DVFS). As illustrated in Fig. 1.2, with such a technique, a system is able to continuously monitor individual workloads, and then deliver the most suitable supply voltage and operating frequency accordingly to each module, and thus minimize dynamic power dissipation. Compared to DPM based techniques,

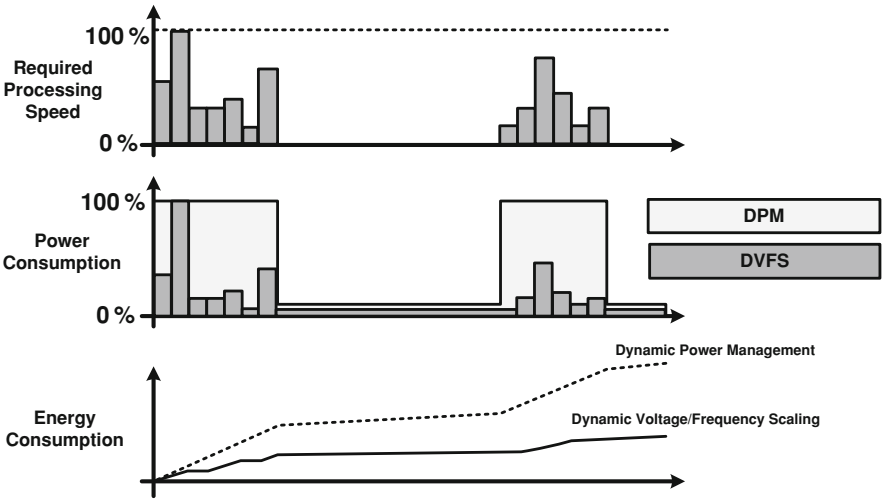

Fig. 1.2 DVFS vs. DPM system level power management schemes

a DVFS-based system completes all tasks on the critical path just within their timing deadlines, thereby eliminating any slack periods.

The fundamental operation of DVFS algorithms can be understood by classifying all tasks that are performed by computing systems as either computation-intensive, low speed or idle, depending on the workload. For computation-intensive tasks, short latency periods are critical, causing them to be executed at high frequencies. For low speed or idle tasks, only a fraction of throughput is required, as completing them ahead of their timing deadline leads to no discernible benefits. While reducing the operating frequency decreases dynamic power dissipation, it does not affect the total energy consumed, which is independent of the frequency to a first order approximation. Therefore, reducing the frequency alone does not improve operation lifetime, which is especially critical for portable and embedded applications. By reducing the supply voltage along with the frequency, energy savings can also be achieved along with power minimization. Similarly, reducing only the supply voltage of a system, while maintaining constant frequency, improves only the energy efficiency, but compromises the throughput. As a result, to achieve maximized power and energy savings, both clock frequency and supply voltage have to be dynamically varied in response to the instantaneous workload.

While DVFS and DPM techniques are the most widely used and fundamental system level power management techniques, other application-specific techniques also exist. For example, techniques such as vector quantization minimize the number of operations required to perform a given function. Cache delay and turning off cache lines can also be employed, in microprocessor based systems. Various other algorithms, from predictive policies, stochastic methods, workload sharing to clock gating, leakage reduction, adaptive body biasing and voltage scaling have all been derived from these fundamental system level power management algorithms.

1.3.2.2 Circuit Level Power Management

While system level power management techniques are employed to identify optimal operation conditions, they require a coordinated effort with hardware-enabling circuits to perform power sensing, power computing and power management. Power sensing involves the use of low power sensor circuits to determine various energy/power related parameters such as harvested voltages, stored battery voltage and current levels. This aids system level power management algorithms to ascertain optimal operation conditions. Hardware-based circuits are then used to perform power computing and subsequent power management, in order to determine the appropriate power delivery mechanisms to load applications. To achieve this, one of the most important circuit level power management modules are DC–DC converters. DC–DC converters are sophisticated closed loop power supplies. They convert an unregulated input DC voltage into an output voltage that is regulated at a desired reference value with high power efficiency, for varying line and output loading conditions. While traditional power converters are capable of delivering only fixed voltages, modern converters can deliver either a variable or multiple voltage levels. Hence, they are used as the hardware-enabling platforms for corresponding system level power management techniques such as DVFS. As a result, these circuits directly influence key factors such as the energy and power efficiency, operating lifetime, cost and size of self-powered microsystems.

As the energy harvested from the ambient environment is low, emerging applications have energy as their primary concern, instead of performance. A popular technique to achieve low power consumption for energy-constrained CMOS circuits is to operate them in the subthreshold or weak inversion region [22]. This is desirable for self-powered applications because it allows *minimum energy operation*, under low-performance situations. In this mode, circuits are powered with a supply voltage that is lower than the threshold voltage of a transistor, thereby considerably reducing the dynamic power. Moreover, subthreshold operation allows circuits to work at the theoretic *minimum energy point* (MEP), at which the total energy consumption is minimized [23]. Subthreshold operation has also been exploited for more advanced power management strategies such as *ultra dynamic voltage scaling* (UDVS) [24].

However, although operating in the subthreshold region considerably reduces the dynamic power consumption, it leads to a significant increase in the leakage power of CMOS circuits. Leakage power losses are critical for advanced semiconductor technologies, which have thinner silicon dioxide layers and lower threshold voltages [25]. Moreover, as numerous modules in self-powered devices typically operate in the sleep/idle mode, leakage power can be comparable or even dominate the total power consumption. Hence, circuit-based techniques are required to minimize the leakage power. One of such techniques is called adaptive body biasing [6, 26], which involves adaptively tuning the body bias voltage of transistors. During idle periods, the threshold voltage is increased so that leakage currents are minimized, while threshold voltages are decreased during active periods, in order to obtain the desired performance. Other circuit techniques also

exist, such as multi-threshold CMOS (MTCMOS) [27]. In this technique, low threshold voltage transistors are used to implement logic circuits. In contrast, high threshold voltage transistors are employed as power gating switches, in order to eliminate leakage currents.

Lastly, in self-powered applications, the aforementioned power management circuits are required to operate in a highly dynamic ambient environment. Depending on the varying environmental conditions, the voltages generated by energy harvesting can change significantly. This severely influences their performance and in the worst case, it can lead to circuit failure. Traditional power management circuits are designed and operated with fixed voltages. However, those methods do not suffice in emerging applications. Therefore, adaptive DC–DC converters with variable output and superior line regulation capability are highly expected. In addition, due to their impact at the system level, circuit level power management is highly critical.

1.3.2.3 Devices in Power Management Systems

At the device level, self-powered systems require energy transducers to convert energy from the ambient environment into useful electrical energy. Thus, understanding the characteristics of these devices is critical to obtain high efficiency, performance and robustness.

As discussed in Sect. 1.2.1, solar energy harvesting systems employ photovoltaic (PV) cells to convert light into electrical energy, through a process known as the photoelectric effect. However, although solar energy is one of the most plentiful energy sources, the energy conversion efficiencies of traditional PV cells are quite low. To overcome this drawback, material and device science research into improving the conversion efficiencies of PV cells has been developed, such as using semiconducting-polymer based photovoltaic devices and multi-junction solar cells [28, 29].

Another important device used in energy harvesting systems is piezoelectric materials, which are used to harvest vibration energy. A piezoelectric device is one that produces an electric charge when a mechanical stress is applied. Conversely, a mechanical deformation is produced when an electric field is applied. However, conventional piezoelectric energy harvesters have narrow operating bandwidths making them impractical when deployed in a real world environment with varying vibration spectra. This has led to research into improving the energy conversion efficiencies of these systems. A popular technique is resonance tuning, which can be performed by altering the physical properties of the vibrating device [30], active tuning by applying an electrical input to the piezoelectric material [31], by applying an axial compressive load [32], etc. Other material-based techniques also exist, such as developing non-uniform thickness piezoelectric cantilevers that can generate high power outputs, MEMS scale piezoelectric harvesters with improved power densities for on-chip implementation, and so on.

Lastly, a solid state device that is ideal for small-scale distributed power generation is the thermoelectric generator. These devices have a small form factor, are highly reliable and scalable, do not employ moving parts, making them attractive for ultra-low power portable applications. The drawbacks of existing TEGs are low output voltage, efficiency and large size. To overcome these drawbacks, numerous device level solutions have been explored. For example, polymer foil TEGs arranged in a coil structure allows for larger voltages to be generated in a smaller generator area [33]. Considerable research has also been conducted into developing thin-film thermoelectric devices. These materials are known for their extremely high heat fluxes, low thermal resistances and can generate significantly higher output voltages [34].

1.4 DC–DC Power Converters

As described in Sect. 1.3.2, the most important component in a circuit-based power management system are DC–DC converters. A DC–DC converter converts a DC input voltage to a regulated DC output voltage, with either a larger or a smaller magnitude, and either same or opposite polarity. Integrated DC–DC converters can broadly be classified into three categories: linear regulators, switch mode power converters and switched-capacitor power converters. Each of these converters regulates the output voltage, from an input voltage source. The output voltage is regulated with reference to a known reference voltage, with the aid of a closed loop feedback controller. DC–DC converters are key components in modern low power applications. They operate as the primary hardware-enabling platforms for several system level power management techniques, by delivering either multiple or variable supply voltages as the new control factor to optimize operation performance, power dissipation and energy efficiency. Hence, understanding certain key parameters involved in the design of DC–DC converters is necessary.

The most critical parameter in the design of DC–DC converter is the efficiency (η), which is defined as,

$$\eta = \frac{P_{\text{out}}}{P_{\text{in}}} \times 100\,\% = \frac{P_{\text{out}}}{P_{\text{loss}} + P_{\text{out}}} \times 100\,\%, \tag{1.1}$$

where P_{out} is the output power, P_{in} is the input power and P_{loss} is the power loss of the converter itself. Under ideal conditions, step-up or step-down voltage conversion takes place with no power loss, resulting in an efficiency of 100%. However, due to various power loss mechanisms in practical power converter designs, the actual power efficiency is lower than the ideal value. Efficiency is a critical parameter, especially for ultra low power applications that rely on energy harvesting mechanisms where the input power generated can be very low.

There are primarily two parameters measuring a DC–DC converter's regulation performance: line regulation and load regulation. Typically the output voltage V_{out}

of a DC–DC converter changes with a change in the input voltage V_{in}. Hence, one figure-of-merit for the steady state voltage regulation of a power converter is line regulation. This is the measure of the converter's ability to maintain the desired nominal output voltage, under varying input voltage conditions. It can be defined as the ratio of the output voltage change ΔV_{out} to a corresponding change in the input voltage ΔV_{in}.

$$\text{Line Regulation} = \left(\frac{\Delta V_{out}}{\Delta V_{in}}\right)\Bigg|_{I_{out}=\text{const.}} \left(\frac{\text{mV}}{\text{V}}\right). \tag{1.2}$$

Line regulation is an essential parameter, especially for energy harvesting based systems, where the generated input voltage can fluctuate considerably with varying environmental conditions.

Typically, the output voltage V_{out} of the converter decreases as the load current I_{out} increases, due to a varying load resistance. Load regulation is used to evaluate such a behavior. It represents the ability of the converter to maintain a constant output voltage under varying load conditions, over a certain range of load current. It is given by,

$$\text{Load Regulation} = \left(\frac{\Delta V_{out}}{\Delta I_{out}}\right)\Bigg|_{V_{in}=\text{const.}} \left(\frac{\text{mV}}{\text{A}}\right). \tag{1.3}$$

Another important parameter in modern DC–DC converters with variable outputs is their reference tracking speed. The parameter defines the rate at which the output of a power converter tracks the change in the reference voltage and is critical for DVFS-enabled systems. It is given by,

$$\text{Reference Tracking Speed} = \left(\frac{\Delta T}{\Delta V_{out}}\right)\Bigg|_{I_{out}=\text{const.}} \left(\frac{\text{s}}{\text{V}}\right), \tag{1.4}$$

where ΔT is the time required for the output voltage to settle within 95 % of the final targeted output voltage defined by V_{ref}. The reference tracking speed is defined for a constant load current value. Note that, with different design standards, the settling time ΔT varies with reference to the acceptable output voltage accuracy, which is normally chosen between 90 and 99 % of the ideal value.

Apart from these parameters, another critical requirement of state-of-the-art portable microsystems is system miniaturization. Many advanced applications such as biomedical implants and wireless sensor nodes are required to have a very small form factor. As mentioned earlier, the choice of the power supply has a critical impact on system volume, as it determines key parameters such as pin and pad requirements, PCB footprint, on-chip silicon area, etc. Hence, for these advanced applications, the ability to integrate the entire power supply on a single chip becomes highly attractive, leading to a completely monolithic solution.

Reconfiguration of power supplies is another highly attractive feature for energy harvesting systems. This is because modern converters that power such applications are expected to operate in a highly dynamic environment, consisting

of fluctuating input voltage levels, varying load power demands, and changing output voltage levels determined by power management algorithms. It is quite challenging to design a single power converter with a fixed topology and control scheme, which can operate with high efficiency under all these varying conditions. Reconfiguration enables the power converter to adaptively restructure its topology or control scheme, based on the instantaneous operating scenario. This results in a highly robust and power-efficient DC–DC converter design.

Lastly, noise characteristics of the DC–DC converters are critical. This is because many low power microsystems, such as wireless sensors, contain RF components. If the power converter has a sufficiently large noise component, this noise can be easily coupled into devices such as transceivers, power amplifiers, etc., which is highly undesirable. Typical sources of noise in power converters can be due to switching inductors that generate electromagnetic interference (EMI) noise, and switching noise in the output voltage. Hence, for noise-sensitive applications, a low noise power supply is highly desired.

Since power converters are critical for the power-efficient operation of self-powered devices, the remainder of this section discusses three major power converters designs, the linear regulator, the switch mode power converter and the switched-capacitor power converter.

1.4.1 Linear Regulators

Driven by perpetual improvements in efficiency and voltage regulation, modern power ICs have undergone several transitions and considerable development. Early power supply designs involved the application of linear regulator based solutions. Linear regulators are active linear analog circuits that are used to convert an unstable and noisy DC power source into a well-regulated power output. This is achieved through a simple and low cost design that is not associated with any magnetic components, making them very desirable for certain noise-sensitive applications.

Some popular linear regulator topologies include the standard linear regulator and the low-dropout (LDO) regulator, as illustrated in Fig. 1.3. The dropout voltage here refers to the minimum voltage drop required across the linear regulator, between the input and output voltages, to maintain valid output voltage regulation. The fundamental structure of a linear regulator consists of an error amplifier (EA) and a pass power transistor, which operates as a voltage-controlled current source. The EA continuously monitors the output voltage against a bandgap voltage reference. Based on the regulation error, the amount of current delivered to the load is controlled, in order to maintain the output voltage at the desired value. Irrespective of their advantages, the major drawback of linear regulators lies in their topological limitations. Only step-down voltage conversion can be achieved. In the meantime, the efficiency of a linear regulator is highly determined by the dropout voltage. High efficiency is achieved at low dropout voltage, but drops significantly for higher dropout values. Frequency compensation

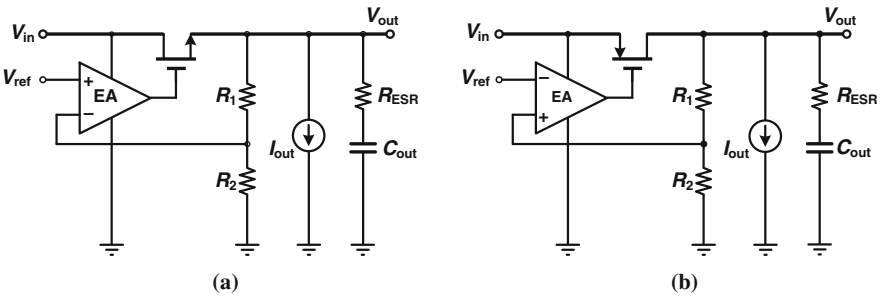

Fig. 1.3 **a** Standard linear regulator and **b** low-dropout (*LDO*) linear regulator

for such a circuit could be sophisticated and noise/process variation sensitive. Therefore, this type of regulator is not the most desirable hardware implementation for a self-powered environment, where the ability to operate over a large dynamic range of voltages is highly preferred.

1.4.2 Switch Mode Power Converters

A second type of power converter that is broadly employed in modern VLSI systems is switch mode power converters. Switch mode power converters consist of a power stage and a closed loop feedback controller to regulate the output voltage. Modern converters can also employ feed-forward controllers. These controllers ensure that the output voltage is highly regulated under varying input voltage conditions, which is typical to energy harvesting systems. The power stage employs switches along with an inductor-based temporary energy storage element. They convert one DC voltage level to another higher or lower voltage level. This is achieved by storing the input energy temporarily during the charge phase of the inductor and then releasing that energy to the output at a different voltage, during the discharge phase. Figure 1.4 illustrates the power stage implementations for the three most common switch mode converters, the buck, boost and the non-inverting buck-boost power converters. In order to regulate the output voltage to a desired reference voltage, the power stage is controlled by a feedback controller. The feedback controller determines the duty cycle of the power stage, in order to obtain the desired output with high accuracy, regardless of line, load or component variations. These converters are highly sophisticated, multi-mode power delivery modules, capable of operating at efficiencies of over 90 % for a wide range of power levels. The most traditional controller employs the pulse-width modulation (PWM) technique. This technique provides negative feedback to control the switching actions of the power stage. It requires the use of an error amplifier to determine the voltage regulation error, along with complex compensation circuitry to achieve system stability.

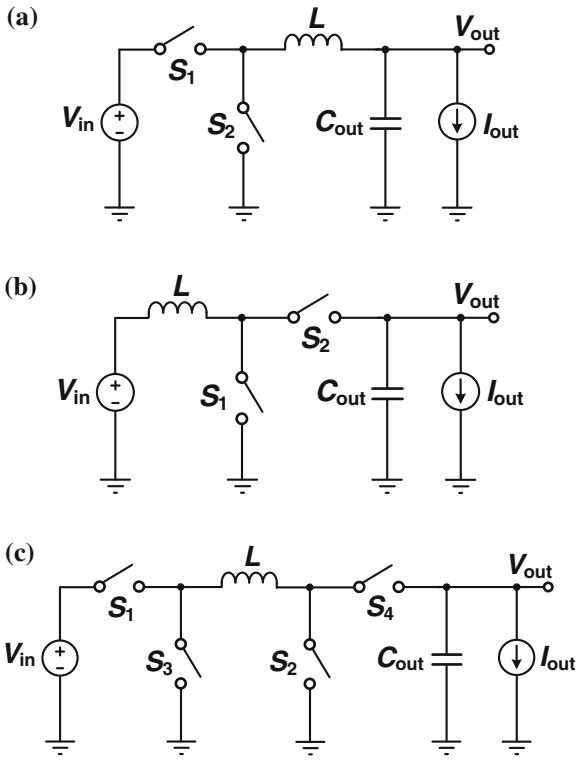

Fig. 1.4 Power stage topologies of switch mode power converters for **a** buck **b** boost and **c** non-inverting buck-boost voltage conversions

While traditional switch mode DC–DC converters generate fixed DC output voltages, state-of-the-art power converters are also capable of delivering variable output voltages, which are suitable for DVFS-based systems. However, the design of such an adaptive power supply is significantly more challenging than the traditional fixed-output counterparts. These converters should have fast transient response to minimize latencies and losses to ensure optimal and robust operation of load applications. The reference voltage tracking speed is required to be significantly enhanced from the state-of-the-art designs, in order to be able to suitably power DVFS applications. Stability issues of adaptive power converters is also considerably more challenging, as the locations of the poles and zeros of the closed loop system are non-stationary, as they are dependent on the output voltage and load current. Lastly, the operating point of the switch mode converter varies with the voltage levels and load currents, thereby affecting its speed, efficiency and power-transistor sizing. Thus, the desired adaptive power supply should be capable of maintaining high efficiency, while providing good line and load regulation over a wide range of voltage and load current levels.

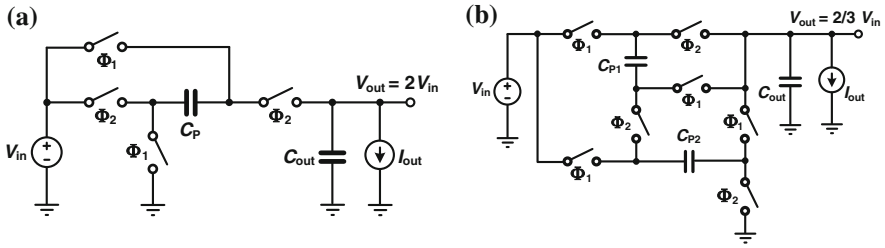

Fig. 1.5 **a** Voltage doubler charge pump and **b** a charge pump with CG = 2/3

1.4.3 Switched-Capacitor Power Converters

The third type of DC–DC converter is the switched-capacitor (SC) power converter. Similar to the switch mode power converter, a SC converter also consists of two major components, the power stage (also known as the charge pump), along with a closed loop feedback controller (and/or a feed-forward controller). The charge pump is an array of capacitors, which act as energy storage elements. An example of the voltage doubler and a charge pump topology with a conversion gain (CG) of 2/3 is illustrated in Fig. 1.5a and b respectively. The use of power switches and clock control signals leads to appropriate switching actions that cause charge storage on the pumping capacitors and then charge transference to the output load, with an ultimate goal to maintain a desired voltage value. The major advantage of SC power converters is their capability for monolithic integration at low power levels, since they employ capacitors as energy storage devices, instead of bulky, off-chip inductors.

One major drawback of traditional SC DC–DC converters is their ability to provide only a single CG, which is defined as the ratio of the output voltage to the input voltage of the converter. For example, as illustrated in Fig. 1.5a and b, the SC converters are capable of efficiently delivering supply voltages that are equal to only two times and two-thirds of the input voltage, respectively. If the output voltage deviates from this desired level, the efficiency of the SC converter drops. If the variation is large, the power loss becomes unacceptably high due to charge redistribution. Hence, to accommodate a large output voltage range and to be capable of powering DVFS-based applications, a SC power converter with a fixed CG does not suffice. To overcome this drawback, state-of-the-art SC power converter designs involve the use of reconfigurable power stages to supply variable output voltages. While such converters are capable of delivering multiple voltage levels, it is done so efficiently only at certain discrete levels, depending on the topology of the reconfigurable charge pump and its corresponding switching actions.

1.5 Discussion and Organization

The joint effort on system miniaturization and efficient power management has culminated into new frontiers in the areas of wireless sensing, implantable bio-engineering, homeland security, ubiquitous computing, and so on. As described earlier, in many of these emerging applications, renewable energy that is harvested by a variety of mechanisms and modalities such as thermal, vibration, and solar cells, has been successfully utilized, supplementing traditional batteries. However, in contrast to conventional electronic devices, these self-powered systems have certain critical operational requirements. Primarily, power supply circuits which interface high level power management algorithms to device level transducers and output load applications are highly desired to provide a multi-mode, reconfigurable system operation. This enables its robust design with high efficiency, fast load transient response, superior line regulation and low noise performance over a wide input and output voltage and power range.

Hence, choosing the appropriate power supply becomes paramount. As mentioned in Sect. 1.4.1, linear regulators are not preferred for such self-powered applications due to their limited operating voltage range and dropout voltages. With respect to switch mode and SC power converters, switch mode power converters require an inductor to efficiently transfer power over different output voltages, whereas SC converters use capacitors as the temporary energy storage elements. The inductor allows for efficient voltage conversion over a wide input and output voltage range, whereas the capacitor can only provide efficient conversion only for certain CGs. However, with continued transistor scaling in each generation of semiconductor processes, MOSFET devices have significantly reduced their turn-on resistance in the power path, while maintaining small sizes. In addition, with smaller transistor sizes needed to implement switches, more switches can be employed for a given silicon real-estate. This increase in switch count allows for more efficient CGs to be realized, leading to more supply voltages that can be delivered to the output efficiently. Secondly, state-of-the-art SC power converters employ capacitors that have a smaller footprint and are very cost-effective. Moreover, it is also feasible to fully integrate a SC power converter on-chip. This is highly desirable for self-powered applications such as implantable biomedical devices, which place considerable impact on low area and volume requirements. SC power converters are also preferred for noise-sensitive applications. This is because it does not involve the use of an inductor in its power stage, which can introduce considerable EMI noise. This noise can be easily coupled into the RF components of the self-powered system, which is undesirable. Lastly, portable devices operate in either sleep or standby modes, for majority of their operating time. During such periods of operation, the load power demand is low and the power dissipated by the controller circuit becomes comparable to the output power. Since this power consumption directly relates to the battery lifetime, it is very important to employ controller circuits with low quiescent current. The quiescent current in SC power converters is significantly lower, due to its simple controller

Hence, the remainder of this book focuses on the various issues related to the design of state-of-the-art SC power converters. Chapter 2 addresses on fundamental device level concepts in power converter designs, including a discussion on power diodes, MOSFETs, BJT, IGBT and thyristors. Chapter 3 introduces the premise behind fundamental charge pump topologies, their design principles and practical implementation issues. Chapter 4 focuses on various power loss mechanisms in charge pumps, in order to maximize the efficiency of SC power converters. In Chap. 5, various state-of-the-art reconfigurable SC power converters are introduced. This chapter will include an in-depth discussion on the design principles involved in reconfigurable charge pumps and corresponding control schemes for these converters. Interleaved SC power converter designs are then presented in Chap. 6. Through an interleaving regulation scheme, these power converters are capable of improving the output voltage ripples, inductor current ripples and the load regulation performance. Lastly, Chap. 7 presents the modeling and design of SC power converters in z-domain. By modeling the transfer function of the power stage, corresponding feedback controller and compensation circuits can be designed to further enhance the performance and accuracy of voltage regulation.

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Chapter 2
Power Semiconductor Devices

2.1 Introduction

Power semiconductor devices are one of the core constituent elements of state-of-the-art power electronic applications. They are employed in a plethora of applications ranging from DC–DC converters, rectifiers, inverters, AC–AC converters, and so on. Modern semiconductor devices are designed to operate accurately and robustly over a large range of operating conditions, while striving to achieve the desired balance between their breakdown voltages, turn-on resistance and switching characteristics. Therefore, they are optimized with respect to physical structure, doping profiles, fabrication and packaging techniques, which jointly define their steady state and dynamic operating performance. As a result, each power semiconductor device exhibits a unique set of operating characteristics. Understanding their device level fundamentals therefore has critical implications on design of efficient, reliable, cost-effective, power IC systems. This chapter focuses on the review of various power semiconductor devices in modern power electronics.

2.2 Power Semiconductor Devices

Power semiconductor devices can be generally classified into two major categories, which are two-terminal passive and three-terminal active devices.

Passive power semiconductor devices are generally diodes, whose operation is dependent on the external circuit that the device is connected to. Two types of two-terminal passive devices are widely used in power electronic applications. The first is the minority charge carrier based power diode, while the second type is the Schottky diode, which is a majority charge carrier device [1].

The second class of power semiconductor devices is active devices. These devices traditionally employ three terminals and their operation is not only

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dependent on the external circuit, but also on separate control signals that drive the power device. Different types of three-terminal power devices exist. The most widely used power device, especially for low power applications, are power MOSFETs. These are majority charge carrier devices, which are known for their high input impedance, fast switching characteristics and low power losses. Apart from these majority charge carrier devices, minority charge carrier based three-terminal devices are also employed, especially for high power electronic applications. These are the power bipolar junction transistors (BJTs), insulated gate bipolar transistor (IGBTs) and thyristors. Hence, the remainder of this section will discuss each of these devices, with respect to their physical structure, steady state operation and switching characteristics.

2.2.1 Power Diodes

Power diodes were the first type of power semiconductor device ever developed, in order to provide an uncontrolled rectification of power. Hence, they are employed in applications that require unidirectional flow of current, such as battery charging, AC and DC power supplies and feedback and freewheeling functions in power converters. Figure 2.1 illustrates a typical diffused power diode, along with its standard electrical symbol, a typical distribution of the active impurity concentration along a cross-section and its *I–V* characteristics. It can be observed that a typical power diode consists of a lightly-doped n-type region (n^-) and a more heavily-doped p-type region (p). This forms a *p-n* junction that is capable of withstanding a large reverse breakdown voltage. The device also contains heavily doped p^+ and n^+ layers, which provides a low contact resistance at the metal–semiconductor interface. Hence, this results in a $p^+pn^-n^+$ structure for the power diode.

The static operation of the power diode is similar to that of a traditional *p-n* junction diode [2]. In the forward-biased condition, holes are injected across the junction, and become minority carriers in the n^- region. The injected minority carriers lower the effective resistivity of the n^- region through conductivity modulation. An increase in the applied positive voltage at the anode terminal leads to greater minority carrier injection, thereby resulting in a further decrease in resistivity. Hence, as seen from the *I–V* characteristic curves in Fig. 2.1c, an exponential increase in diode forward current is observed, with an increase in the forward voltage. In the reverse bias condition, the diode conducts a small leakage current, due to the flow of minority carriers. The leakage current increases gradually with voltage, until a threshold value is reached, called the breakdown voltage. Beyond this voltage value, the device undergoes avalanche breakdown. Under this condition, the reverse current increases rapidly and the diode can be damaged by heat, due to the large power dissipation at the junction.

An alternate structure for the power diode, for applications where fast switching characteristics are desired, over the capability to handle very high power levels, is the epitaxial power diode. Its structure and doping profile is illustrated in Fig. 2.2.

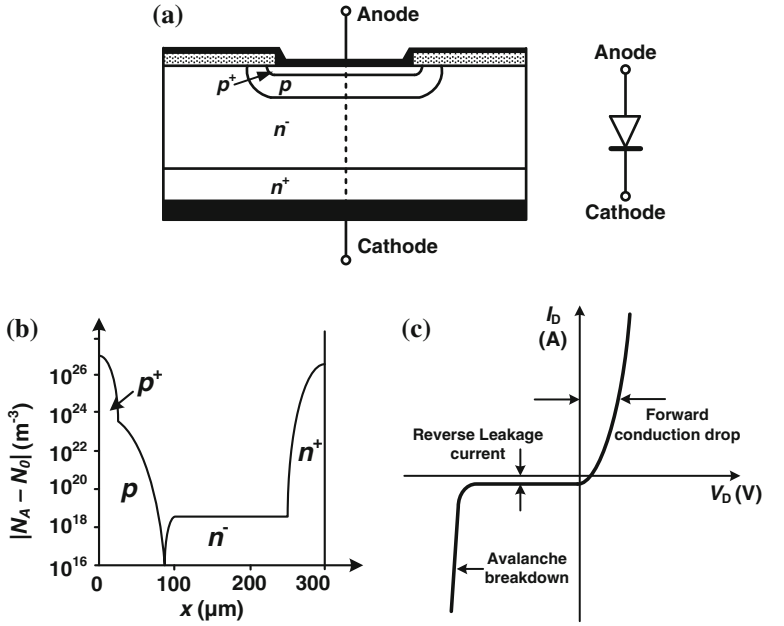

Fig. 2.1 **a** The structure of a p^+pn^-n power diode, **b** its doping profile and **c** *I*–*V* characteristics

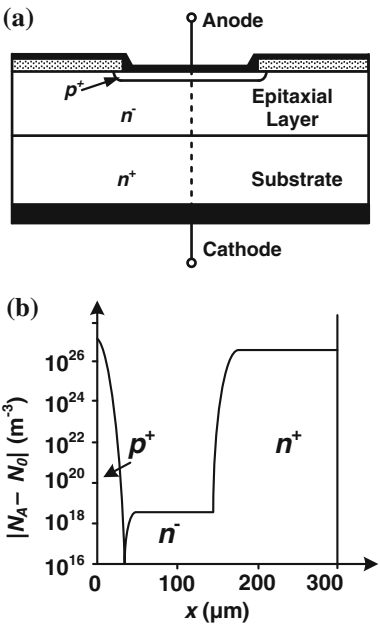

Fig. 2.2 **a** Structure of an epitaxial diode and **b** its doping profile

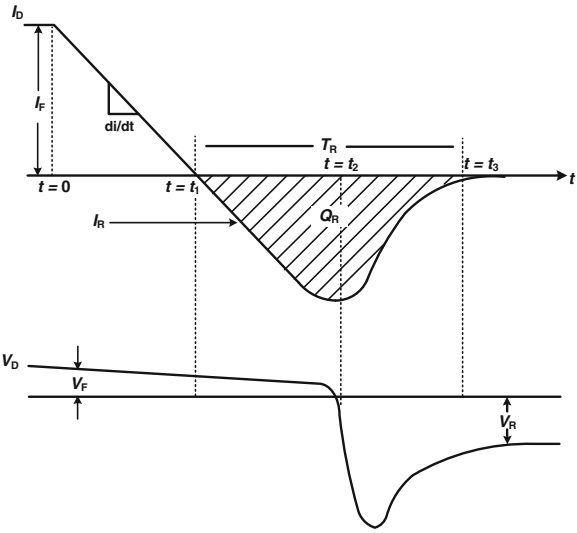

Fig. 2.3 Turn-off switching characteristics of a power diode

The power diode consists of a heavily doped n^+ substrate over which a lightly doped n^- epitaxial layer is deposited. A p^+ surface layer is then diffused onto the n^- layer, in order to form the p-n junction. During static operation, the I–V curves of the epitaxial diode are similar to Fig. 2.1c.

While the I–V characteristics of the power diode accurately represent its operation during equilibrium, during transient operation, considerable differences in device operation are observed. This is illustrated in Fig. 2.3, which shows the turn-off characteristics of the epitaxial diode [3]. Initially, at time $t = 0$, the diode operates in the forward biased condition and is saturated with minority charge carriers. Hence, the voltage across the diode is the forward conduction drop. Then, the diode is switched from the on state to the off state. However, the presence of minority charge carriers at the p-n^- junction maintains the diode in the forward-biased condition and will turn off only after this charge is completely removed. This can be achieved by either applying a reverse voltage to the diode terminals, or through charge recombination. As observed in Fig. 2.3, applying a negative voltage to the anode terminal changes the direction of current flow. At time $t = t_1$, the diode current becomes negative. This initiates the removal of minority charge carriers from the p-n^- junction. The total charge stored in the depletion region is illustrated in the negative portion of the diode current waveform, and is known as the recovered charge Q_R. At the time interval $t = t_2$, the minority charge carriers in the p-n^- region are removed and the diode junction becomes reverse-biased. Hence, the diode becomes capable of blocking a negative voltage. The remainder of the recovered charge, from t_2 to t_3, charges the depletion region capacitor, to the negative off-state voltage. After t_3, the diode blocks the entire applied reverse voltage. Therefore, the total time duration from t_1 to t_3 is known as the reverse recovery time, T_R. This is a critical parameter as it directly influences the

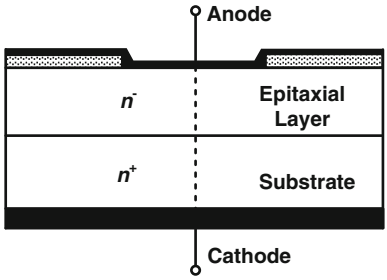

Fig. 2.4 Structure of a Schottky power diode

maximum operating frequency of power electronic applications and determines the switching power losses in diode-based switch mode power supplies.

Another type of power diode employed in power electronic applications is the Schottky diode. The Schottky diode is employed when a very low forward voltage drop is desired and a high blocking potential is not necessary. These diodes are made with a metal–semiconductor junction. As a result, they are majority carrier devices, where the diffusion of minority charges is negligible. The structure of the diode is illustrated in Fig. 2.4. The semiconductor adopts an n-type material, due to higher mobility of electrons over holes. The semiconductor at the anode terminal is lightly doped to form a rectifying contact, and is of the order of $N_D = 10^{14}$–10^{16} cm^{-3} for silicon. At the cathode end, the doping level of the n-type material is very high, to form a non-rectifying ohmic contact between the metal and n^+ semiconductor. The flow of electrons into the metal creates a region in the n^- semiconductor, adjacent to the metal–semiconductor interface that is depleted of majority charge carriers, thereby forming a depletion region. Unlike a traditional *p-n* junction diode, where the depletion region is formed based on the difference in the doping concentrations, the depletion region in the Schottky diode is dependent only on the work function of the metal and semiconductor materials. Hence, during forward-biased condition, electrons flow from the n-type semiconductor into the metal, similar to a traditional *p-n* junction diode. However, for a Schottky diode, the flow of current is due to the injection of majority charge carriers from the n-type material into the metal. These charge carriers drift in response to the applied electric field. As a result, the need to accumulate or remove excess minority charges is eliminated, thereby avoiding the forward and reverse recovery phenomena. Hence, the time constants associated with the switching actions of the diode are limited only by the times required to charge and discharge the depletion region capacitor at the metal–semiconductor interface. As a result, very fast switching speed can be achieved.

However, one of the major drawbacks of Schottky diodes occurs during the revere-biased condition. The diode suffers from much larger leakage current than traditional diodes. Leakage currents increase with temperature and can cause thermal instability. This limits the maximum applicable reverse voltage, which is considerably lower than the actual voltage rating.

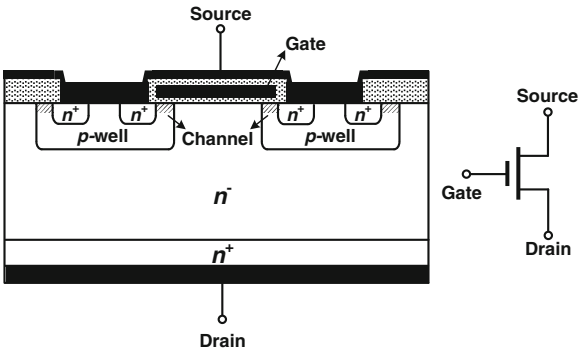

Fig. 2.5 Physical structure of a power MOSFET with its symbol

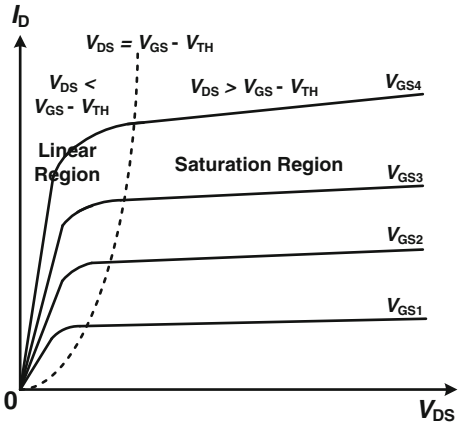

Fig. 2.6 *I–V* characteristics of the power MOSFET

2.2.2 Power MOSFET Transistors

One most widely used semiconductor device today is the metal-oxide semiconductor field effect transistor (MOSFET). Due to features such as being a voltage-controlled device, having high input impedance and being capable of switching at high speeds, the MOSFET has revolutionized the IC industry. For power supply applications, the power MOSFET is widely employed, which has characteristics similar to that of a traditional MOSFET. The cross-section of the device is illustrated in Fig. 2.5, which shows an enhancement-type n-channel power MOSFET. This structure is known as the vertical double-diffusion MOSFET (DMOS) transistor, due to the presence of source and drain contacts on opposite sides of the die and since two diffusions are required to fabricate the p-wells and the n^+ sources. As seen from Fig. 2.5, the transistor is fabricated on an n^+ substrate, which is traditionally a single crystal wafer that provides the required physical support to the device. An n^- epitaxial layer is then grown on top of the n^+ substrate. The size of this layer depends on the maximum blocking voltage required, when the transistor

is turned off. A power MOSFET usually consists of multiple parallel-connected cells. Hence, this requires the diffusion of p-wells and n^+ regions along the surface of the wafer. The p–wells form the body terminal of the MOSFET and are all internally connected to the source, through source metal contacts.

The operation of the power MOSFET can be explained with the aid of the I–V characteristics curves, illustrated in Fig. 2.6. When the potential at the gate terminal is less than the threshold voltage, the MOSFET remains off. Under this condition, both the p-n^+ and the p-n^- regions are reverse-biased. Any applied drain-to-source voltage V_{DS} appears across the p-n^- region. When a sufficiently large gate-to-source voltage, V_{GS}, is applied, a channel is formed at the surface of the p–region, underneath the gate terminal. This channel conducts current, leading to the flow of electrons from the n^- region, through the channel, into the n^+ source, and out of the external source contacts. As illustrated in Fig. 2.6, when the power MOSFET is turned on, it can operate in two different regions, similar to the traditional MOSFET. It operates in the saturation region when $V_{DS} > V_{GS} - V_{TH}$ and $V_{GS} > V_{TH}$, and operates in the linear region when $V_{DS} < V_{GS} - V_{TH}$ and $V_{GS} > V_{TH}$.

One of the major differences between the traditional and the power MOSFET is the presence of a body diode, which is in parallel with the channel. The body diode is present due to the p-n^- junction between the p-type base and the n^-- epitaxial layer. It can be turned on when a negative voltage is applied across the gate-to-source terminal. While the body diode is capable of conducting the full rated current of the power MOSFET, it is not optimized with respect to its switching speed. As a result, when the body diode has to be turned off, it undergoes a reverse recovery process. The resulting reverse current flowing through the MOSFET generates heat due to its turn-on resistance. Moreover, the collapsing electric field at the p-n junction of the body diode leads to a large voltage across the diode, which jointly raises the risk of heat damage on the transistor. To overcome this drawback, many modern power MOSFETs are designed with fast recovery body diodes. These body diodes are characterized by their soft reverse recovery process that requires smaller reverse recovery current [4].

The overall structure of a power MOSFET is thus illustrated in Fig. 2.7. It depicts the parasitic capacitances along with the body diodes. The parasitic capacitances for the power MOSFET are critical since it affects the switching characteristics directly. From Fig. 2.7, it can be observed that C_{GS} is the gate-to-source capacitance. It is created due to the overlap of the source and the channel regions by the poly-silicon gate and is independent of the applied voltage. C_{GD} is the gate-to-drain capacitance and consists of the capacitance due to the overlap between the poly-silicon gate and the n^- silicon underneath and the capacitance due to the depletion region immediately below the gate terminal. Lastly, C_{DS} is the drain-to-source capacitance and is associated with the body diode. It varies inversely with the square root of the drain-to-source voltage.

A power MOSFET is a majority carrier device, and hence minority charge carriers do not influence the switching speeds. The switching characteristics of such a device is determined based on the time duration required to charge and discharge the parasitic capacitances.

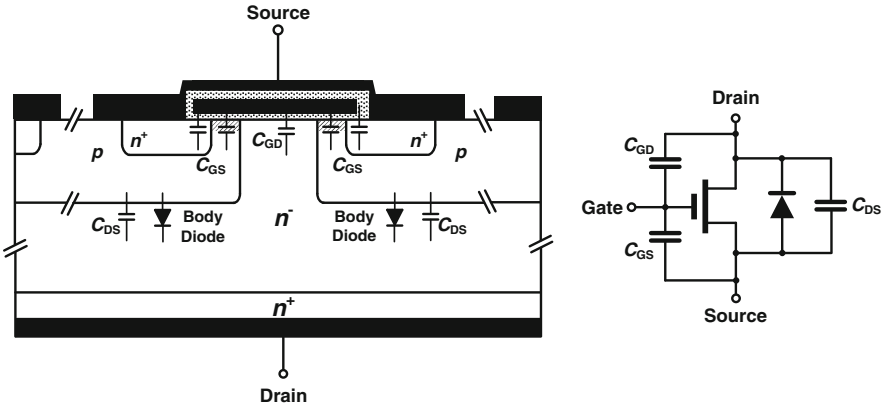

Fig. 2.7 Structure and symbol of a power MOSFET including parasitic capacitors and body diodes

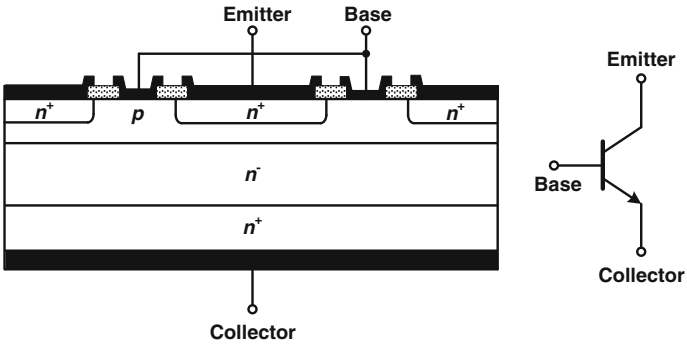

Fig. 2.8 Structure of a power BJT transistor with its symbol

2.2.3 Power Bipolar Junction Transistors

A power bipolar junction transistor (BJT) is a three-terminal, two-junction, self-controlled device. Its physical structure is illustrated in Fig. 2.8. It consists of the emitter, the base and the collector terminals. However, unlike a traditional BJT, the flow of current is vertical through the silicon wafer. Moreover, the collector region consists of a heavily doped n^+ region along with a lightly doped n^- region, which is inserted to achieve a sufficient breakdown voltage. A power BJT operates in the on-state (saturation) when both the p-n^+ base-emitter junction and the p-n^- base–collector regions are forward-biased. Under this condition, both the p and the n^- regions contain a significant amount of minority charge carriers, and thus have a low turn-on resistance. On the other hand, the transistor operates in the off-state,

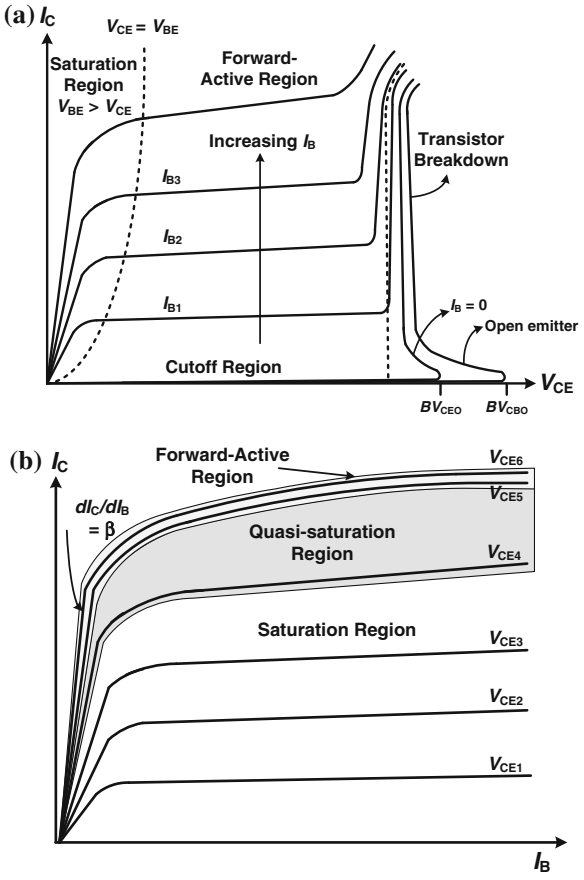

Fig. 2.9 Static characteristics of the power BJT **a** I_C vs. V_{CE} and **b** I_C vs. I_B

also known as cut-off, when both the base-emitter and the base–collector regions are reverse-biased. The third region of operation for the power BJT is the well-known forward-active region, where the base-emitter region is forward-biased, while the base–collector region is reverse-biased. In the active region, the collector current of the BJT is proportional to the base minority charge current. Lastly, the transistor can also operate in the quasi-saturation region. In this region of operation, the base current is not large enough to saturate the device. As a result, the minority charge carriers present in the n^- region is not sufficient to increase the conductivity of this region. Hence, the transistor has a high turn-on resistance.

Figure 2.9 illustrates the static characteristics of the power BJT. Figure 2.9a illustrates the collector current I_C with respect to the collector-emitter voltage V_{CE}, for different values of base current I_B. The different regions of operation are also highlighted. As discussed earlier, it can be observed that for a given value of I_c, the transistor will function as a switch, by operating in the saturation region, only for a sufficiently large base current I_B. Figure 2.9a also illustrates the breakdown

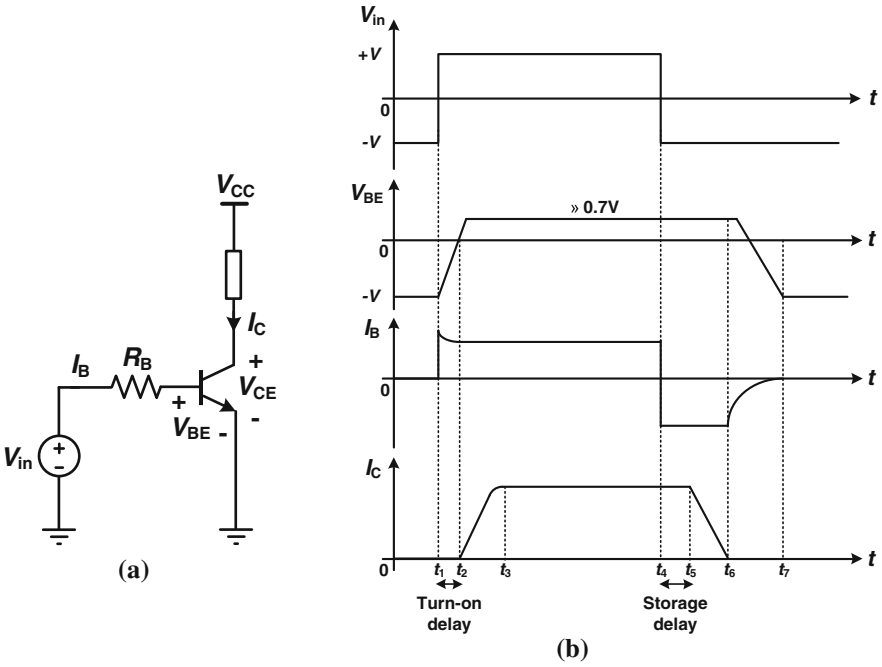

Fig. 2.10 **a** Circuit schematic to demonstrate BJT switching characteristics and **b** its switching waveforms

voltages for the transistor. Firstly, when the transistor operates in the forward-active region, the base–collector *p-n* junction is reverse-biased. Hence, if a sufficiently large voltage is applied to this reverse-biased junction, it will undergo avalanche breakdown. The voltage at which this occurs is the breakdown voltage BV_{CBO}, which is defined when the emitter is open-circuited, or for a large negative base current. The breakdown voltage BV_{CEO} is the collector-emitter breakdown voltage. As illustrated in Fig. 2.9a, this breakdown voltage is smaller than BV_{CBO}, and is measured when the base current is zero. For majority of applications, the collector-emitter voltage V_{CE} should not exceed BV_{CEO} during the off-state. Figure 2.9b illustrates the collector current I_C as a function of the base current I_B, for different V_{CE} voltages. From this figure, it can be observed that in the saturation region I_C remains approximately constant with respect to I_B and is dependent only on V_{CE}. In the forward-active region, I_C increases linearly with I_B, and is defined by the slope dI_C/dI_B, which is also called the forward current gain β. β decreases at high values of the collector current, due to the difficulty in saturating the transistor.

In power electronics, the BJT is usually employed as a switch, and has to function between the saturation and the cutoff regions. Hence, it is critical to understand its switching characteristics, which is illustrated in Fig. 2.10. Figure 2.10a illustrates the circuit set-up to demonstrate the switching characteristics of a BJT. $V_{in}(t)$ is the varying supply voltage, which is used to control the

base current I_B, while V_{CC} is the power supply and R_L is the loading resistor. As illustrated in Fig. 2.10b, at the instant $t = 0$, $V_{in}(t) = -V$, due to which the transistor operates in the cutoff region. I_B and I_C are both zero, and the entire input voltage appears across the base-emitter junction. At $t = t_1$, $V_{in}(t) = +V$, which starts the turn-on process of the BJT. The input power supply provides a base current to the BJT, which starts to charge the depletion region capacitance of the base-emitter junction. This causes V_{BE} to rise from $-V$ to zero, at t_2. The time duration $\Delta t = t_2 - t_1$ is known as the *turn-on delay period*. After t_2, the base-emitter junction becomes forward-biased, causing minority charge carriers to be injected into the base. I_C thus increases proportionally. At t_3, the base–collector region becomes forward-biased. The transistor operates in the saturation region.

To describe the turn-off characteristics of the power BJT, at t_4, the voltage $V_{in}(t) = -V$. Similar to the *p-n* junction diode, the BJT does not turn off immediately due to the presence of minority charge carriers at the base-emitter junction. However, a negative base current of $-(V - V_{BE})/R_B$ is present, which actively discharges the minority charge carriers, along with recombination. At t_5, all excess minority charge carriers, which are required to saturate the BJT, are removed. Hence, the time duration $\Delta t = t_5 - t_4$ is known as the *storage time*. At t_5, the transistor begins to operate in the forward active mode. The presence of the negative base current continues to remove minority charge carriers from the base. As a result, I_C decreases and eventually reaches zero, allowing the base-emitter junction to be reverse-biased at t_6. The time duration $\Delta t = t_6 - t_5$ is known as the *turn-off time* of the BJT. The base-emitter region eventually becomes fully discharged, thereby completely turning off the device at t_7.

2.2.4 Insulated Gate Bipolar Transistors

Insulated gate bipolar transistors (IGBTs) were introduced in the mid-1980s, and are extremely popular in high power electronics applications, with a power rating ranging from a few kWs to several MWs. They have replaced power BJTs as the preferred semiconductor device in the high power range, and are used mainly in applications such as DC/AC drives and power supply modules. An IGBT is essentially a hybrid MOS-gated bipolar transistor. It combines the advantages of both a MOSFET and a BJT. It is a voltage-controlled, high input impedance device, similar to a MOSFET, but has a much lower turn-on voltage drop, especially at high voltage ratings. Moreover, unlike a BJT, its switching time durations are considerably shorter [5].

The structure of an IGBT is illustrated in Fig. 2.11. It can be observed that its construction is very similar to that of a power MOSFET, except with a p^+ layer that is fabricated at the collector instead of the n^+ drain layer. The operation of this device is as follows. When a positive voltage is applied at the gate terminal, with respect to the emitter, an n-channel is induced in the *p*-region. This leads to the flow of a drain current in the effective NMOS transistor, thereby forward biasing

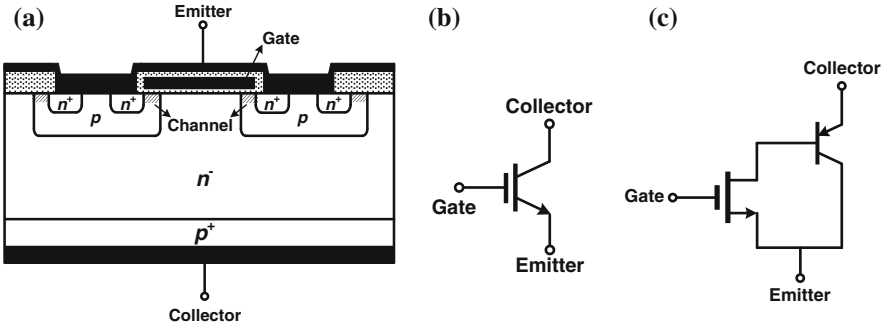

Fig. 2.11 **a** Physical structure, **b** symbol, and **c** equivalent circuit of an IGBT

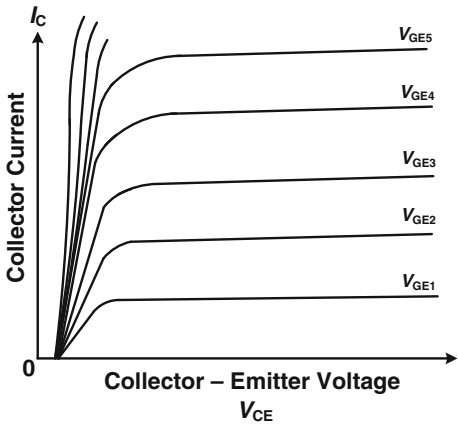

Fig. 2.12 I-V characteristics of an IGBT

the emitter–base junction and turning on the PNP transistor. This causes minority charge carriers to be injected from the p^+-collector region into the n^- epitaxial layer. As a result, the resistivity of the n^- region decreases considerably due to conductivity modulation, which leads to a significant reduction in the conduction loss of the IGBT. In order to turn off the IGBT, a zero or negative voltage is applied to the gate terminal. This prevents the formation of the channel in the *p*–region. As a result, the PNP transistor of the IGBT is turned off. The *I*–*V* characteristic curves of the IGBT is illustrated in Fig. 2.12, from which it can be observed that the characteristics resemble that of a power BJT. Moreover, the device does not experience any secondary breakdown characteristics, making it highly preferable for high power, high temperature applications.

As described above, one of the key advantages of the IGBT is that its n^- epitaxial layer undergoes conductivity modulation, which significantly reduces the voltage drop and conduction losses when turned on. However, this phenomenon also leads to one big limitation—increased switching time durations. When the IGBT has to be turned off, the potential at the gate terminal is reduced to zero or a

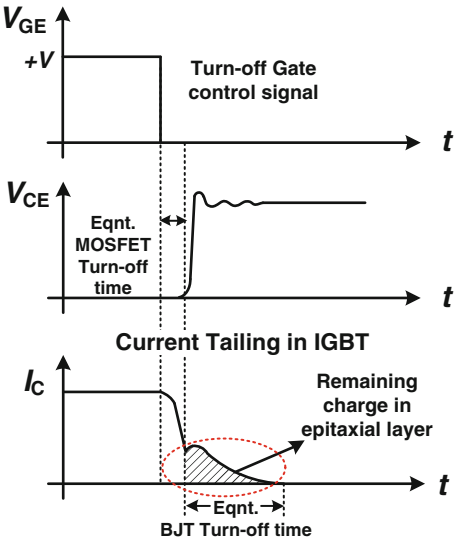

Fig. 2.13 Turn-off switching characteristics of the IGBT

negative value. While this turns off the effective MOSFET transistor quickly, the PNP transistor will continue to stay on as long as minority charge carriers exist in its base terminal. From Fig. 2.11, it can be observed that this base terminal is the n^- epitaxial layer, which is not accessible externally. Hence, the turn-off speeds of the IGBT cannot be improved through the use of external gate drive circuitry. The presence of minority charge carriers stored in the base leads to the generation of a characteristic tail in the current waveform of the IGBT [6], which is illustrated in Fig. 2.13. It can be observed that the collector current initially drops rapidly, when the gate voltage goes to zero. This is because the effective MOSFET turns off, thereby ceasing the flow of electrons. However, the remainder of the holes in the epitaxial layer is removed only through electron–hole recombination, hence leading to the current tailing effect. This tail leads to significant switching losses in the IGBT, and thus necessitates the use of longer dead-times in modern power supplies.

2.2.5 Thyristors

The last power semiconductor device discussed in this chapter is the thyristor. It features a family of devices, including silicon controlled rectifiers (SCRs), gate turn-off thyristor (GTO), the MOS-controlled thyristor (MCT) and integrated gate-commutated thyristor (IGCT). Of all power semiconductor devices, the SCR is known to handle the largest amount of power, with voltage and current ratings of the order of several thousands of volts and amperes, respectively. Hence, these devices are traditionally employed in applications such as DC transmission lines.

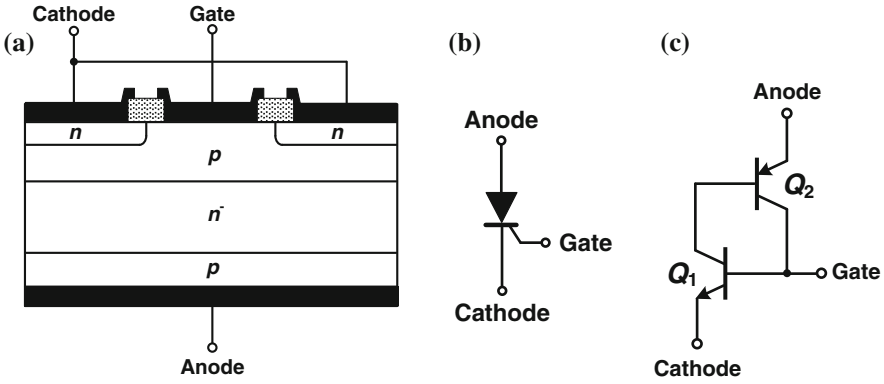

Fig. 2.14 **a** Physical structure, **b** symbol, and **c** equivalent circuit of a SCR

Figure 2.14 illustrates the structure, the schematic symbol and the equivalent circuit of a SCR. The device is a three-junction PNPN type device, which can be represented as two bipolar junction transistors connected through a regenerative feedback. The transistor Q_1 is formed by the n, p, and n^- regions, while the second transistor Q_2 is formed by the p, n^- and p layers. The SCR is known for its symmetric voltage blocking nature, due to its ability to block voltages in both the forward and reverse directions. This is because one of the p-n^- junctions is always reverse-biased, causing a depletion region to be formed in the n^- layer. The SCR can conduct current only when a positive voltage is applied to the anode terminal, relative to the cathode terminal. However, the device starts to conduct only when a positive gate current is supplied. This current causes the transistor Q_1 to turn on. Since Q_1 and Q_2 are connected in a regenerative feedback manner, the collector current of Q_1 provides the necessary base current to Q_2, thereby turning on Q_2. Hence, a positive feedback mechanism is created, causing minority charge carriers to be injected into all four semiconductor layers. As a result, due to conductivity modulation, the turn-on resistance of the device is lowered considerably and the device is latched to the on-state. When I_G is greater than the *latching current*, the current flowing through the SCR becomes independent of I_G. It behaves similarly to a conventional p-n junction diode and with the current varying exponentially with V_A. In order to turn off the SCR, a reverse current can to be applied at the anode or a negative anode-to-cathode voltage will force the device into the off-state.

The I–V characteristics of the SCR are illustrated in Fig. 2.15. It can be observed that for forward-biased condition at zero gate current, the device will initially conduct a leakage current. If the anode voltage V_A is increased to a sufficiently large voltage level, the device starts to conduct. This is the breakover voltage of the SCR. If a base current is applied to the device, due to the regenerative feedback mechanisms, the forward breakover voltage is reduced. Eventually, at a sufficiently large base current I_{G3} in Fig. 2.15, the SCR behaves like a traditional p-n junction

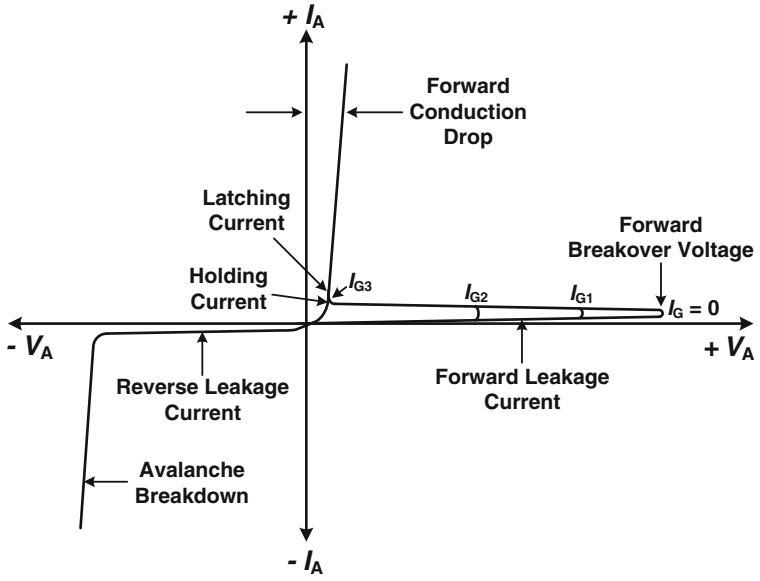

Fig. 2.15 Static *I-V* curves of a SCR

diode, with the forward blocking region removed. The device will be turned on successfully if a minimum gate current, called the latching current, is maintained. During conduction, if the gate current is zero and the anode current falls below a critical limit, called the holding current, the device reverts to the forward blocking state. When a negative voltage is applied to the anode terminal, the p-n^- junction of the device becomes reverse-biased and the *I–V* curves behave similarly to the traditional diodes.

The switching characteristics of the SCR are similar to those of the epitaxial diode, illustrated in Fig. 2.3. During the turn-off transition, a negative anode voltage reverses the direction of current flow in the SCR. However, the inner p-n^- junction continues to be forward biased as long as minority charge carriers continue to exist in this junction. These charge carriers are removed with the aid of the negative current and through charge recombination. As a result, a minimum turn-off time is always required before a positive voltage can be applied again at the anode. If a positive voltage is applied before this, the presence of minority charge carriers could retrigger the SCR, without the need for an external gate current. However, this is not desired in traditional switching operations.

One of the major limitations of SCRs is the inability of the device shutdown through gate control. To overcome this drawback, the gate turn-off thyristor (GTO) was developed, which can be turned on by the application of a gate current pulse and turned off by a negative gate current pulse. The GTO is capable of being turned off by a negative current pulse, by diverting the collector current of the effective PNP transistor. This prevents the positive feedback effect between the

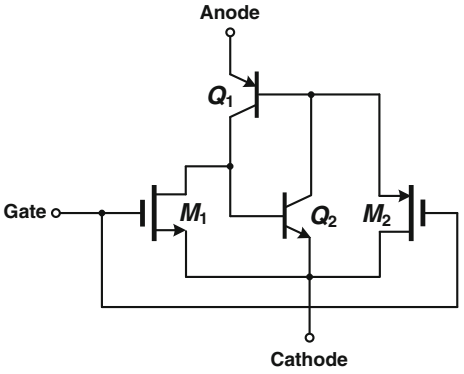

Fig. 2.16 Equivalent circuit of a MCT

two BJTs. However, the GTO cannot be turned off under all operating conditions, as it is dependent on its turn-off current gain. This is defined as the ratio of the anode current, when the device is turned on and conducting, to the negative gate current required to turn off the device. As a result, a negative current of the order of several hundreds of amperes would be required to turn off a GTO, which can typically conduct several thousands of amperes of current when operating in the on state.

Lastly, the third type of thyristor which attempts to provide gate control on the switching process is the MOS-controlled thyristor (MCT) [7]. As the name suggests, the MCT is a hybrid device that can be turned on or off by applying a voltage pulse at the gate terminal of the device. The operation of the MCT can be explained with the aid of Fig. 2.16, which illustrates its equivalent circuit. The MCT is turned on by applying a negative pulse at the gate terminal, relative to the anode. This negative voltage turns on the PMOS transistor M_2, which provides the necessary base current to the NPN transistor Q_1. Once Q_1 is turned on, the regenerative action between Q_1 and Q_2 causes the MCT to conduct current. In order to turn off the MCT, a positive voltage is applied to the gate terminal, with respect to the anode. This turns on the MOSFET M_1, which interferes with the positive feedback mechanism between the two BJTs. As a result, the MCT is turned off.

2.3 Conclusions

This chapter introduces certain fundamental semiconductor devices that are employed in modern power electronic applications, from ultra low power portable devices to extremely high power systems. The various types of devices that are discussed can be generally classified into passive and active devices. Passive devices are traditionally two-terminal devices such as the p-n^--n diode and the Schottky diode, whose operation is dependent solely on the circuit operating

conditions. On the other hand, the second class of power semiconductor devices is active devices such as MOSFETs, BJTs, IGBTs and thyristors. These devices include a third terminal which is used to control device operation, apart from external circuit conditions. In order to achieve the desired steady state and transient switching operations, each of these devices is optimized with respect to their physical design and fabrication. Hence, the chapter provides a brief overview of these power semiconductor device principles. With a thorough understanding of these underlying concepts, reliable and high-performance SC power converters can be designed.

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Chapter 3
Fundamental Charge Pump Topologies and Design Principles

Switched-capacitor (SC) DC–DC converters are a class of power converters that are used to convert one voltage level to another, through the use of switches and capacitors. They consist of two parts, a power stage, which is also known as a charge pump, and a feedback/feed-forward controller that regulates the output to the desired voltage value. In general, a charge pump employs pumping capacitors as the temporary energy storage medium. To achieve the desired power conversion, the capacitors are initially energized from the input power source, during their charge period. The stored energy is then transferred to the output, during the discharge period. This is implemented with the aid of the controller, which appropriately turns on the power switches for one or more phases in a clock period, to obtain the desired charge pump topology. Hence, each switching period comprises of n separate non-overlapping clock phases. In each phase, the charge pump is configured as a network of capacitors and switches and by correctly switching between these phases, the required voltage conversion is obtained.

Since charge pumps handle the power transfer operations, they are critical for the efficiency, robustness and operation performance of SC DC–DC converters. Thus, a fundamental understanding of charge pumps is essential. To facilitate this, this chapter will focus on various charge pump topologies, their design principles and practical implementation issues. The chapter will begin by introducing the concept of charge transfer between capacitors. To characterize the performance of charge pumps, critical parameters are investigated. Elementary charge pumps then are introduced, followed by a thorough discussion on more advanced topologies and their corresponding operation principles. Lastly, following the theoretical analysis, practical issues in the design and implementation of integrated charge pump designs are investigated.

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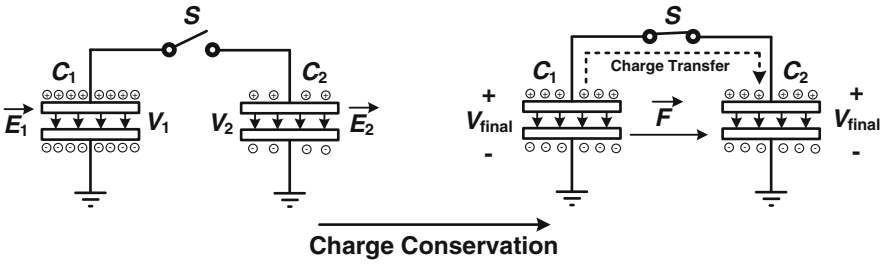

Fig. 3.1 Charge conservation between two capacitors

3.1 Principle of Charge Transfer

This section discusses the principle of charge transfer between capacitors, which is the most fundamental concept in the operation of charge pumps. To understand it, it is important to understand the concept of charge distribution. Consider two capacitors C_1 and C_2, which are initially charged to voltages V_1 and V_2 respectively, as illustrated in Fig. 3.1. This generates an electric field E_i between the capacitor plates, which is related to the potential difference V_i by

$$\overrightarrow{E_\mathrm{i}} \cdot d_\mathrm{i} = V_\mathrm{i} \,(\mathrm{i} = 1, 2), \tag{3.1}$$

where d_i is the distance between the plates of the capacitor C_i. Let the two capacitors be then connected in parallel, by turning on the switch S. The potential difference between the two capacitors forces charge redistribution. To understand this, let W be the work done on the stored charges, due to the voltage difference between the two plates. Its value is given by

$$\frac{W}{q} = (V_1 - V_2). \tag{3.2}$$

This work is done by an electrostatic force F, which redistributes charges between the two capacitor plates. From *Gauss' Law* [1], the expression for the work done can be written as

$$W = -\int \frac{\vec{E}}{q} \cdot \vec{ds} = -\int \vec{F} \cdot \vec{ds}, \tag{3.3}$$

where F is the electrostatic force exerted on the charge along a path ds. For the scenario shown in Fig. 3.1, assuming $V_1 > V_2$, the electrostatic force redistributes charge from capacitor C_1 to C_2. By substituting Eqs. 3.3 into 3.2, we get

$$(V_1 - V_2) = \frac{W}{q} = -\frac{1}{q}\int \vec{F} \cdot \vec{ds}. \tag{3.4}$$

Hence, from Eq. 3.4, it can be seen that, as long as a potential difference exists between the two capacitors, an electrostatic force continues acting upon the stored charges. This force redistributes the stored charges until the voltage of both capacitor plates are equal. Once charge redistribution is complete, each capacitor is charged to a voltage V_{final}, which can be determined based on the principle of conservation of charge. From this law, it is known that when two charged capacitors are connected together, the total charge on the parallel combination is equal to the sum of the original charges on the capacitors. The total original charge Q_{total} on the two capacitors is given as

$$Q_{\text{total}} = C_1 V_1 + C_2 V_2. \tag{3.5}$$

After the charge is re-distributed, the resulting voltage V_{final} across each capacitor is given as

$$\begin{aligned} V_{\text{final}} &= \frac{Q_{\text{total}}}{C_1 + C_2} = \frac{C_1 V_1 + C_2 V_2}{C_1 + C_2} \\ &= \left(\frac{C_1}{C_1 + C_2}\right) V_1 + \left(\frac{C_2}{C_1 + C_2}\right) V_2. \end{aligned} \tag{3.6}$$

The principle of charge distribution can be employed to analyze the operation of a charge pump. Figure 3.2a illustrates a basic voltage replicator charge pump, whose ideal voltage at steady state should be equal to the input voltage supply. In this charge pump, C_1 is the pumping capacitor, while C_2 is the output capacitor, which is initially charged to zero. The operation of the charge pump is as follows. During the first charge cycle, S_1 is on and S_2 is off, causing C_1 to be charged to V_{in}. During the discharge cycle, when C_1 and C_2 are connected in parallel, charge redistribution takes place. Ideally, V_{out} is charged up to a voltage V'_{out} which can be calculated from Eq. 3.6 as

$$V'_{\text{out}} = \left(\frac{C_1}{C_1 + C_2}\right) V_{\text{in}}. \tag{3.7}$$

If $C_1 = C_2$, $V'_{\text{out}} = V_{\text{in}}/2$. In the second charge transfer cycle, during the charge phase, C_1 charges up to V_{in}. During the discharge phase, charge redistribution takes place once again, resulting in V_{out} being charged to a higher voltage level V''_{out} given by

$$V''_{\text{out}} = \left(\frac{C_1}{C_1 + C_2}\right) V_{\text{in}} + \left(\frac{C_2}{C_1 + C_2}\right) \cdot V'_{\text{out}}. \tag{3.8}$$

For equal values of capacitances, $V''_{\text{out}} = V_{\text{in}}/2 + V_{\text{in}}/4$. During the third charge transfer phase, V_{out} is charged up to a voltage level given by $V_{\text{in}}/2 + V_{\text{in}}/4 + V_{\text{in}}/8$. Thus, in such a continuous manner, V_{out} approaches the input voltage V_{in}, as illustrated in the switching waveform in Fig. 3.2b.

From the above analysis, it can be observed that during each switching cycle, the charge pump undergoes a charge phase and a discharge phase. This concept is

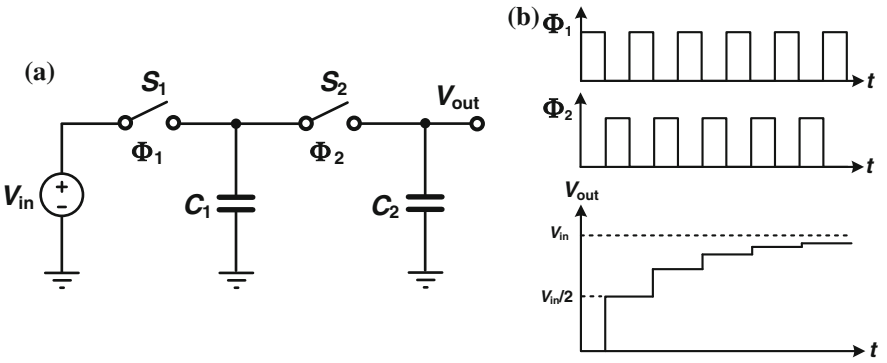

Fig. 3.2 **a** Circuit schematic, and **b** output voltage waveforms for a SC votlage replicator

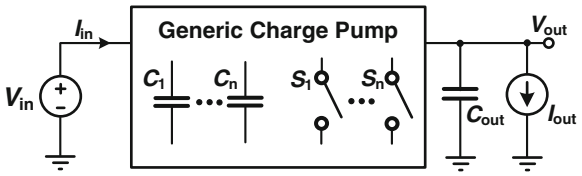

Fig. 3.3 Generic charge pump

inherent to all charge pump designs. While the voltage replicator charge pump is capable of charging up only to V_{in}, advanced SC converters can employ several charge pump stages to achieve different topologies, allowing them to generate a wide range of output voltages, both higher and lower than the input supply, with either the same or opposite polarity.

3.2 Charge Pump Parameters

An understanding of certain fundamental parameters in charge pumps is necessary before various topologies can be investigated. To aid this discussion, consider a generic charge pump, illustrated in Fig. 3.3. V_{in} is the input voltage of the charge pump, while the output voltage is V_{out} and supplies a load current I_{out}. The charge pump employs pumping capacitors C_1 to C_{n} along with switches S_1 to S_{n} to achieve the desired voltage conversion.

The most critical parameter in the design of charge pumps is its efficiency (η), which is defined as

$$\eta = \frac{P_{\text{out}}}{P_{\text{in}}} \times 100\,\% = \frac{P_{\text{out}}}{P_{\text{loss}} + P_{\text{out}}} \times 100\,\%, \tag{3.9}$$

where P_{out} is the output power, P_{in} is the input power and P_{loss} is the power loss of the charge pump itself. Under ideal conditions, voltage conversion takes place with no power loss, resulting in an efficiency of 100 %. However, due to various power loss mechanisms in practical power converter designs, the actual efficiency is lower than the ideal value.

A second critical parameter in defining charge pumps is the conversion gain (CG). It is defined as the ratio of the output voltage to the input supply voltage, as given by

$$\mathrm{CG} = \frac{V_{out}}{V_{in}}. \tag{3.10}$$

The CG of a SC DC–DC converter is dependent on the topology of the charge pump and also the duty ratio of the clock signals employed.

To measure the voltage regulation performance, two parameters are line and load regulation [2]. Line regulation is the measure of the SC power converter's ability to maintain the desired nominal output voltage, under varying input voltage conditions. It is defined as the ratio of the output voltage change ΔV_{out} to a corresponding change in the input voltage ΔV_{in}, for a constant load current I_{out}.

$$\text{Line Regulation} = \left(\frac{\Delta V_{out}}{\Delta V_{in}}\right)\Bigg|_{I_{out}=\text{const.}} \left(\frac{\text{mV}}{\text{V}}\right). \tag{3.11}$$

As I_{out} increases, typically the output voltage V_{out} decreases. This is because the output capacitor C_{out} delivers the required load current until the charge pump responds to the change in output power demand. To evaluate such a regulation behavior, load regulation is defined and is the ability of the charge pump to maintain a constant output voltage under varying load conditions, over a certain range of load current. It is given by

$$\text{Load Regulation} = \left(\frac{\Delta V_{out}}{\Delta I_{out}}\right)\Bigg|_{V_{in}=\text{const.}} \left(\frac{\text{mV}}{\text{A}}\right). \tag{3.12}$$

Another important parameter in charge pumps is the output voltage ripple, which is defined at steady state for a constant load current. It value is dependent on the value of the output capacitor C_{out}, its equivalent series resistance (ESR) and the switching frequency f_s. Typically, the ripple is expected to be less than a few tens of millivolts. A large ripple voltage impacts the operation performance and robustness of load applications and is of critical concern in noise sensitive modules such as RF communication and signal processing circuits.

3.3 Fundamental Charge Pump Topologies and Operations

In order to obtain the required CG in the charge pump, power switches are appropriately controlled in order to obtain several capacitor configurations. These configurations form different charge pump topologies, which are used to provide

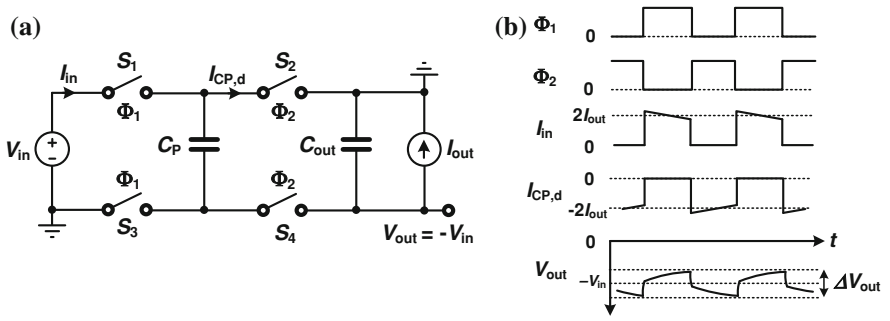

Fig. 3.4 **a** Circuit schematic, and **b** voltage and current waveforms for a voltage inverter

different voltage levels. Hence, this section introduces several fundamental topologies, along with their operation schemes.

3.3.1 Voltage Inverter

The first charge pump topology to be discussed is the voltage inverter, which provides a CG of -1. The circuit of the voltage inverter and corresponding waveforms are illustrated in Fig. 3.4. The operation of the voltage inverter is as follows. In the charge phase, the clock signal $\Phi_1 = 1$ which causes the switches S_1 and S_3 to turn-on, while S_2 and S_4 are turned off. This connects the pumping capacitor C_P to the input, thereby charging it to V_{in}. The average value of the input current over the switching period is equal to the load current I_{out}. However, its initial value is dependent on the voltage across C_P, the ESR of the pumping capacitor and the turn-on resistance of the power switches S_1 and S_3. As illustrated in Fig. 3.4b, due to the discontinuous nature of the charge current, its initial value is greater than $2I_{out}$ and decays as the voltage across the pumping capacitor approaches V_{in}. In the discharge phase, $\Phi_2 = 1$, which causes the switches S_2 and S_4 to be on, while S_1 and S_3 are turned off. The pumping capacitor is disconnected from the input and connected to the output capacitor C_{out} and the load. The voltage stored in C_P is inverted and used to charge C_{out} and provide the required load current.

Similar to all power converters, the voltage inverter undergoes a start-up process initially, after which the steady state is reached and the output voltage of $-V_{in}$ is obtained. Under this condition, the amount of charge transferred from C_P to C_{out} is dependent on the switching frequency and the load current.

Furthermore, from Fig. 3.4, it can be observed that the output consists of a ripple voltage along with the nominal DC value. Typically, the output ripple in a SC power converter is attributed to the impulse-like charge transfer operation discussed in Sect. 3.1. During the charge phase, C_{out} supplies the load current, while during the discharge phase it is supplied by the charge pump. Hence, these charge and discharge

actions lead to the generation of ripples in the output voltage. For integrated charge pumps, conventionally, the ripple voltage can be analyzed by considering its behavior in the *slow switching limit* (SSL) operation [3]. In this operating mode, the RC delays, due to the switches, capacitors, and their ESR, are small compared to the switching period. Thus, the output voltage ripple is dependent on the switching frequency f_s, C_{out} and load current I_{out}. The maximum peak-to-peak voltage ripple for the voltage inverter supplying a current source load can be determined as follows. From Fig. 3.4b, it can be observed that when the charge pump transits from the charge phase to the discharge phase, a step change of $-2I_{out}$ is observed in the pumping capacitor discharge current $I_{CP,d}$. This creates a step change in V_{out} equal to $2I_{out} \times \mathrm{ESR}_{Cout}$, where ESR_{Cout} is the ESR of the output capacitor. After the initial step change, C_{out} is then charged by the charge pump. As the first order approximation, this voltage is equal to $I_{out}/(2\, f_s \cdot C_P)$. As a result, the peak-to-peak output ripple voltage ΔV_{out} for the voltage inverter is given by

$$\Delta V_{out} = 2I_{out} \cdot \mathrm{ESR}_{Cout} + \frac{I_{out}}{2f_s \cdot C_{out}}. \tag{3.13}$$

During the charge phase, when C_P is connected to V_{in}, the ripple waveform reverses its direction. The current $I_{CP,d}$ increases to zero at the instant when phase Φ_1 occurs, after which C_{out} is discharged by the load current I_{out}.

3.3.2 Voltage Doubler

While the voltage inverter provides a negative CG, many charge pumps accomplish positive CGs. One widely used example is the voltage doubler, as illustrated in Fig. 3.5. During the charge phase when $\Phi_1 = 1$, the operation of the doubler is identical to the voltage inverter. The pumping capacitor C_P is connected to the input supply, thereby charging it to the voltage level V_{in}. However, during the discharge phase when $\Phi_2 = 1$, the input voltage is connected in series with C_P. This enables the voltage doubling operation to be realized. However, one major difference of the voltage doubler, when compared to the voltage inverter, is that the input current waveform has an average value of $2I_{out}$. This is because V_{in} is connected to C_P during the charge phase and to the load during the discharge phase.

From Fig. 3.5b, it can be observed that the output current of the voltage doubler is discontinuous and similar to that of the voltage inverter. As a result, the peak-to-peak output ripple voltage ΔV_{out} for the voltage doubler is also given by

$$\Delta V_{out} = 2I_{out} \cdot \mathrm{ESR}_{Cout} + \frac{I_{out}}{2f_s \cdot C_{out}}. \tag{3.14}$$

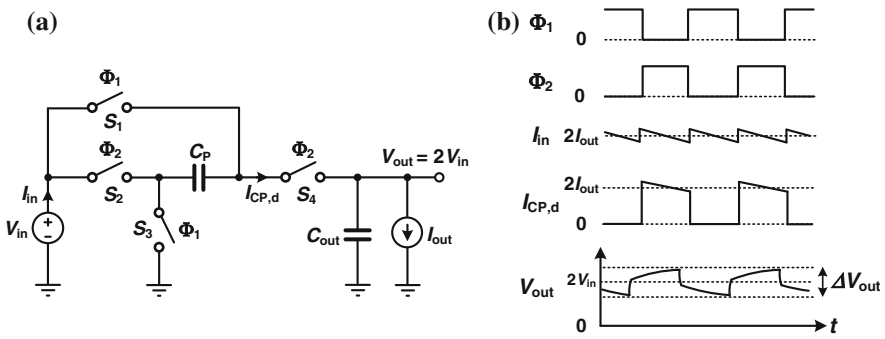

Fig. 3.5 **a** Circuit schematic, and **b** voltage and current waveforms of a voltage doubler

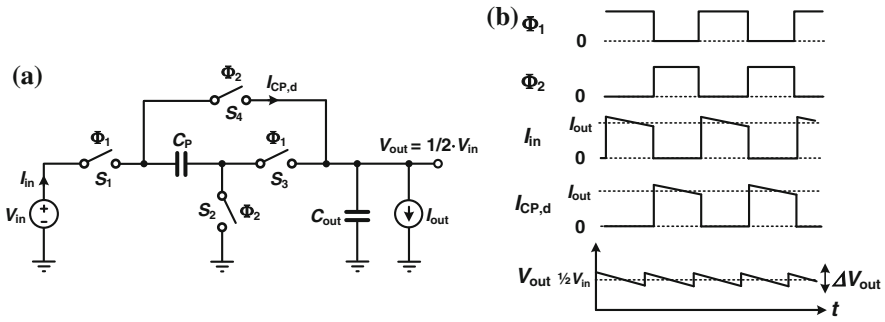

Fig. 3.6 **a** Circuit schematic, and **b** voltage and current waveforms of a charge pump with CG = ½

3.3.3 Step-Down Charge Pump

While the voltage doubler in Sect. 3.3.2 achieves a higher voltage at the output in comparison to the input voltage, some charge pumps are also capable of generating output voltages that are lower than the input power supply. An example is the charge pump with a CG = 1/2, whose circuit diagram and voltage and current waveforms are illustrated in Fig. 3.6. Its operation is described as follows. During the charge phase when $\Phi_1 = 1$, the switches S_1 and S_3 are turned on, while S_2 and S_4 are turned off. As a result, the pumping capacitor C_P is connected in series with the output capacitor. During the discharge phase when $\Phi_2 = 1$, S_2 and S_4 are turned on, while S_1 and S_3 are turned off. The energy stored in C_P is delivered to the output. From the charge pump operation, it can be observed that the two capacitors are connected in series during the charge phase, and then discharged in parallel. Hence, for a 50 % duty ratio clock signal, an output voltage equal to $1/2V_{in}$ is obtained.

One of the major advantages of this charge pump, when compared to the previous two topologies, is that charge is delivered to the output during both the charge and discharge phases. As a result, the contribution of the ripple component $2I_{out} \cdot ESR_{Cout}$ to the total output ripple voltage, is eliminated. Thus, the ripple voltage performance of the charge pump is significantly enhanced and is ideally given by

$$\Delta V_{out} = \frac{I_{out}}{2f_s \cdot C_{out}}. \tag{3.15}$$

3.4 Practical Charge Pump Circuits

In order to achieve various CGs, Sect. 3.3 discussed several charge pump topologies and their corresponding operation principles. Each of the charge pumps employs ideal switches and capacitors. However, for their practical circuit realizations, charge pumps employ on- or off-chip capacitors and power semiconductor devices for implementation. These components are associated with various non-idealities such as turn-on resistances, parasitic capacitances and inductances, leakage currents, and so on. Therefore, this section discusses several practical circuit implementations of the charge pump topologies discussed in Sect. 3.3, along with operation and design principles.

3.4.1 Dickson Charge Pumps

3.4.1.1 Diode-Based Implementation

One of the most well-known charge pump topologies is the Dickson charge pump [4]. Its contribution to modern charge pump designs has been remarkable and has triggered many innovations in this field. The earliest circuit implementation of the Dickson charge pump employs diodes as switches, as illustrated in Fig. 3.7. The charge pump employs two clocks, Φ_1 and Φ_2, which are anti-phase and with a voltage amplitude of V_Φ. The diodes operate as self-timed switches and are characterized by a forward bias voltage V_D. C_s is the stray parasitic capacitance present at each node. The charge pump operates by pumping charge along the diode chain, causing the capacitors C to be successively charged and discharged during each clock cycle. For example, when the clock $\Phi_1 = 0$ and $\Phi_2 = 1$, the diode D_1 conducts until the voltage at node 1 becomes equal to $V_{in} - V_D$. When the clock $\Phi_1 = 1$, the voltage at node 1 increases to $V_{in} + (V_\Phi - V_D)$. This causes the diode D_2 to conduct until the voltage at node 2 becomes equal to $V_{in} + (V_\Phi - V_D) - V_D$. Then, when $\Phi_1 = 0$ and $\Phi_2 = 1$ again, the voltage at node 2 becomes equal to $V_{in} + 2(V_\Phi - V_D)$. At the output of the nth stage, the voltage is

$$V_{out} = V_{in} + N \cdot (V_\Phi - V_D) - V_D. \tag{3.16}$$

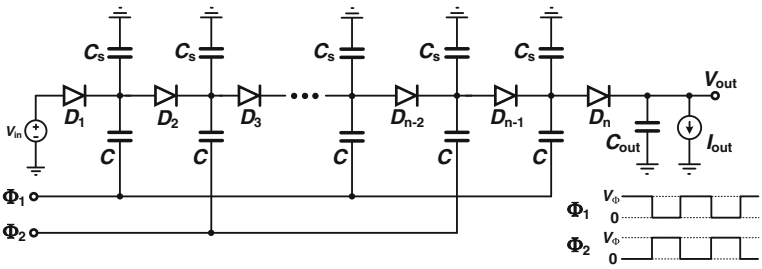

Fig. 3.7 Circuit schematic of the Dickson charge pump

From Eq. 3.16, it can be observed that for $N = 1$ and $V_\Phi = V_{in}$, the output voltage of the Dickson charge pump is approximately equal to twice the input voltage. Hence, it can be used to implement a voltage doubler. Furthermore, cascading more stages allows for higher CGs to be realized.

While Eq. 3.16 accounts for the diode voltage drop, the effect of stray parasitic capacitances on V_{out} is not addressed. Stray capacitances reduce the amount of charge transferred from each stage to the next, by a factor equal to $C/(C + C_S)$. As a result, the actual output voltage is given as

$$V_{out} = V_{in} + N \cdot \left(\left(\frac{C}{C + C_s} \right) V_\Phi - V_D \right) - V_D. \tag{3.17}$$

Equations 3.16 and 3.17 are valid when no load is connected to the output of the charge pump. However, when the charge pump has to deliver a load current I_{out}, the output voltage is reduced by an amount that is inversely proportional to the switching frequency, f_s, and is given by

$$V_{out} = V_{in} + N \cdot \left(\left(\frac{C}{C + C_S} \right) V_\Phi - V_D - \frac{I_{out}}{(C + C_S) \cdot f_s} \right) - V_D. \tag{3.18}$$

Based on the operation of the Dickson charge pump, it can be observed that when $\Phi_1 = 1$, charge is delivered to the output capacitor C_{out}, while during the phase $\Phi_2 = 1$, C_{out} delivers the required current to the load. This leads to a voltage ripple at the output and for a resistive load R_{out}, it is given by

$$\Delta V_{out} = \frac{I_{out}}{f_s \cdot C_{out}} = \frac{V_{out}}{f_s \cdot R_{out} \cdot C_{out}}. \tag{3.19}$$

3.4.1.2 MOSFET-Based Dickson Charge Pump

The main advantage of the diode-based Dickson charge pump is that additional switch control signals are not required. However, the main drawback is the

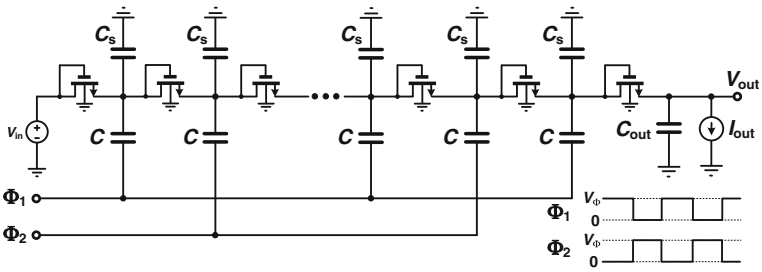

Fig. 3.8 MOSFET-based Dickson charge pump

reduction in V_{out} due to the voltage drop V_D. In addition, in many semiconductor processes, isolated diodes are not available. To overcome these issues, a MOSFET transistor based implementation for the Dickson charge pump is illustrated in Fig. 3.8, in which diode-connected NMOS transistors replace isolated diodes. Hence, the diode forward voltage drop V_D is replaced by the NMOS threshold voltage, V_{TN}, in Eq. 3.18. While the MOSFET-based topology of the Dickson charge pump solves issues related to silicon integration, the advent of sub-micron fabrication technologies introduces further challenges and constraints. In modern technologies, transistor threshold voltages have not decreased commensurately with the reduction of the maximum supply voltage levels. Moreover, from Fig. 3.8, it can be observed that the substrate terminals of each NMOS transistors are connected to ground, while the voltage at the source terminal varies at each stage. Hence, due to the body effect, the threshold voltages of MOS transistors are not constant [5]. For the Dickson charge pump illustrated in Fig. 3.8, the voltage gained at the nth stage is given by

$$V_n - V_{n-1} = \frac{CV_\Phi}{(C + C_s)} - V_{TN}[V_{SB}(n)]. \tag{3.20}$$

Here V_{TN} is the threshold voltage of the NMOS transistor, which is dependent on the source to body voltage V_{SB}. It can be observed from Eq. 3.20 that the voltage gained at each stage decreases, due to the increase in the threshold voltage. As a result, the output voltage becomes lower than the value obtained by the diode-based charge pump. The output voltage is not a linear function of the number of stages and its efficiency decreases as the number of stage increases. Hence, considerable research effort is still required in order to develop novel strategies to overcome this loss.

3.4.1.3 Dickson Charge Pump with Bootstrap Gate Control

Although conceptually simple, implementing a switch using a MOSFET is challenging. This is because typically the voltages at the drain and source terminals of diode-connected NMOS transistors are higher than the supply voltage. In some cases, the voltage generated at the next stage is used to control the MOSFET in the

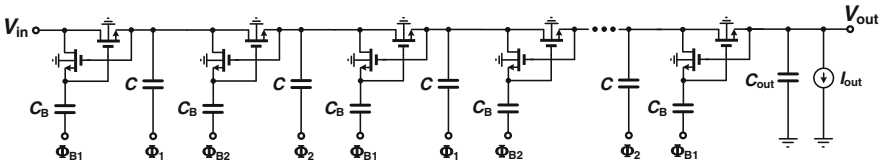

Fig. 3.9 Dickson charge pump with bootstrap control

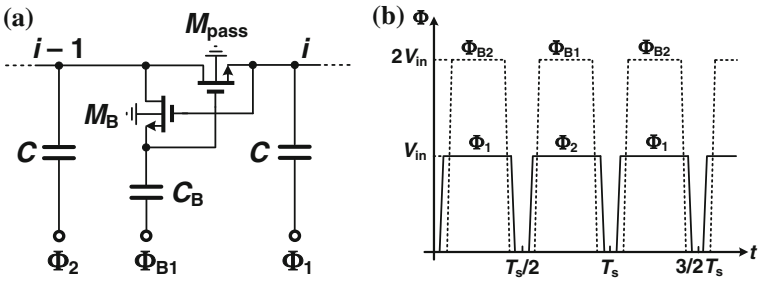

Fig. 3.10 **a** Single stage of the Dickson charge pump with boostrap gate control, and **b** corresponding timing diagram

previous stage. However, this introduces certain challenges at start-up, when the voltage at the next stage is lower than the previous stage. The most prominent solution developed so far is shown in Fig. 3.9, which is the Dickson charge pump with bootstrap gate control. It employs a bootstrap circuit in order to provide the necessary gate control signals to drive its switches. The bootstrap circuit is realized by adding a supporting capacitor C_B and MOS transistor M_B to each stage. This circuit operates in conjunction with the pass transistors M_{pass} and pumping capacitor C, in order to generate the necessary output voltage. The operation of this topology can be described with the aid of Fig. 3.10, which illustrates a single stage of the charge pump and its corresponding timing diagram.

During the first half period, charge transfer does not occur since the clock signal $\Phi_{B1} = 0$, causing the transistor M_{pass} to be turned off. From Fig. 3.10b, during this period, the clock signal $\Phi_1 = 1$. This causes the bootstrap transistor M_B to be turned on, since its V_{GS} voltage is equal to $2V_{in}$. The capacitor C_B is thus charged up to a voltage equal to $V_{i\_1} = (i - 1)V_{in} - (i - 2)\cdot\Delta V$, where ΔV is the voltage transferred from one stage to the next, when M_{pass} is turned on. During the next half period, the clock signal $\Phi_1 = 0$, while $\Phi_2 = 1$. It can be observed from the timing diagram that during this phase, the clock signal $\Phi_{B1} = 1$. Due to the charge injected into C_B during the previous phase, the gate voltage of M_{pass} is boosted up significantly, causing it to be turned on. This enables charge transfer from node $i - 1$ to i.

While this charge pump solves one of the major challenges associated with the gate drivability of the power switches, one drawback does exist. This circuit

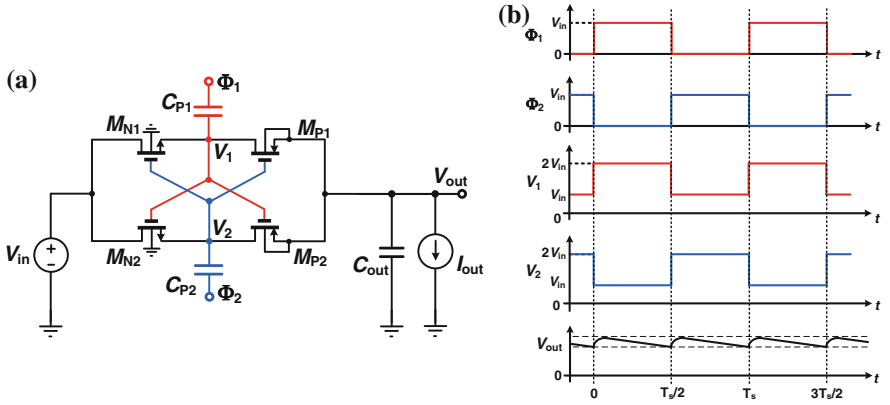

Fig. 3.11 **a** Schematic diagram of the cross-coupled voltage doubler, and **b** its timing diagram

requires a 4-phase clock signal, with two of the phases requiring the doubled voltage swing, when compared to the traditional clocking scheme used in traditional Dickson charge pumps.

3.4.2 Cross-Coupled Voltage Doubler

Among all the CGs provided by charge pumps for various advanced applications, the most widely used is the voltage doubler. Many voltage doubler solutions have been developed, but face several drawbacks. One of the most straightforward techniques to implement such a circuit was discussed in Sect. 3.3. In this implementation, an amplitude of $2V_{in}$ or higher is required as the gate drive signals for the power switches. This significantly increases switching power losses in the charge pump. Moreover, the voltage drop across each power switch is equal to one V_{DS}, which is typically 150 mV or less, when turned on. This results in a voltage drop of $2V_{DS}$ in both the charge and discharge paths, which contributes to considerable conduction loss in the charge pump. To overcome these drawbacks, the cross-coupled voltage doubler is developed and is considered as one of the most efficient topologies for low-voltage applications. In this charge pump, the gate drive signal for each power transistor is internally generated. Therefore, the amplitude of the clock signals is always V_{in}. Secondly, in both the charge and discharge paths only a single power transistor is turned on. As a result, the total voltage drop is equal to a single V_{DS} instead of $2V_{DS}$, thereby reducing the conduction power loss.

The schematic of the cross-coupled voltage doubler is illustrated in Fig. 3.11a, and its operation can be explained with regard to the timing diagram in Fig. 3.11b. In the steady state, the voltages across the two pumping capacitors C_{P1} and C_{P2} are almost equal to the input voltage V_{in}. As shown in Fig. 3.11b, when $\Phi_1 = 1$ and $\Phi_2 = 0$, the voltage of V_1 is equal to $2V_{in}$ and the voltage of V_2 is V_{in}. As a result,

the NMOS transistor M_{N2} controlled by V_1 and the PMOS transistor M_{P1} controlled by V_2 are turned on, while M_{N1} and M_{P2} are turned off. The pumping capacitor C_{P2} is connected to the input voltage and charged to V_{in}. Meanwhile, C_{P1} is connected in parallel with the output capacitor C_{out}, and the charge stored at C_{P1} is transferred to the output. Eventually, the voltage across C_{P2} will be V_{in} and the voltage across C_{P1} will be $V_{out} - V_{in}$. Similarly, when $\Phi_1 = 0$ and $\Phi_2 = 1$, the switches M_{N1} and M_{P2} are turned on and M_{N2} and M_{P1} are turned off. C_{P1} is connected to the input supply and charged to V_{in}. C_{P2} is connected to C_{out} and discharged. At the end, the voltage across C_{P1} will be V_{in} and the voltage across C_{P2} will be $V_{out} - V_{in}$.

In the steady state, the total net charge difference on the two pumping capacitors C_{P1} and C_{P2} should be equal to the charge consumed by the output load in one switching cycle. This is represented as

$$(C_{P1} + C_{P2})[V_{in} - (V_{out} - V_{in})] = \frac{V_{out}}{R_{out}} T_s, \tag{3.21}$$

where T_s is the switching period of the voltage doubler. If $C_{P1} = C_{P2} = C_P$, then,

$$\frac{V_{out}}{V_{in}} = \frac{2}{1 + {}^{T_s}/_{2R_{out}C_P}}. \tag{3.22}$$

If $T_s << 2R_{out}C_P$, then $V_{out} \approx 2V_{in}$. Hence, a CG of 2 is achieved. From Eq. 3.22, it can be observed that a higher switching frequency and lower output load allows the use of smaller capacitors for the same output voltage ripple. It is also shown that a higher switching frequency, lower output load and larger pumping capacitors lead to a higher output voltage.

3.5 Design Issues in Integrated Charge Pumps

Advancements in semiconductor fabrication technologies have led to the development of several advanced charge pumps, involving monolithic implementations. Such designs employ integrated switches and capacitors and are highly beneficial for ultra-low power applications, such as wireless sensor nodes and implantable devices. This is because integrated charge pumps rely fully on on-chip components. As a result, the number of off-chip pins and pads are significantly reduced, thereby decreasing the PCB footprint and system volume. Hence, such charge pumps are attractive for portable applications that place considerable emphasis on small form factor. Moreover, an integrated implementation allows for the realization of sophisticated feedback/feed-forward controllers, which can considerably enhance operation performance and system robustness. However, the implementation of integrated charge pumps introduces certain critical issues that have to be considered. Thus, this section discusses these factors and their influence on modern charge pump designs.

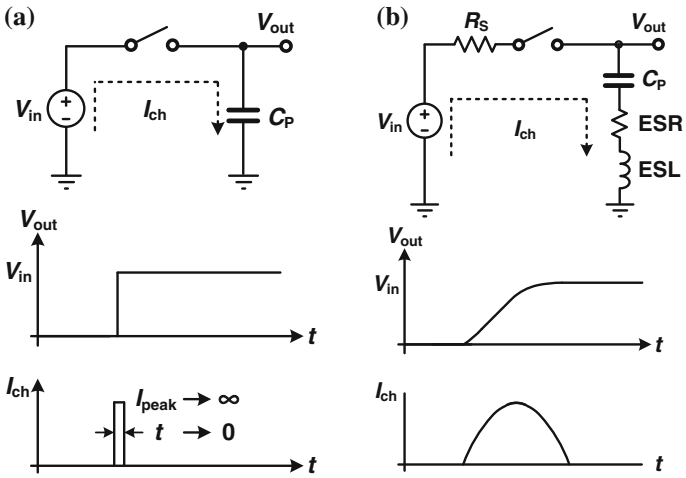

Fig. 3.12 Charging of an **a** ideal, and **b** practical capacitor

3.5.1 Practical Capacitor Implementations

The first issue in practical charge pump designs is related to the charging characteristics of capacitors. Typically, if an ideal capacitor is charged from an input voltage source, it charges instantaneously, resulting in an impulse current, as shown in Fig. 3.12a. However, all capacitors have an equivalent series resistance (ESR) and an equivalent series inductance (ESL). These parasitic components limit the peak charge current, resulting in an increased charge time of the capacitor. Moreover, MOS switches are also associated with a turn-on resistance, which further limit the charging current. The charging characteristics of a practical capacitor are shown in Fig. 3.12b.

In addition, all integrated capacitor implementations are associated with stray parasitic capacitances, which degrade the efficiency of the charge pump, as discussed in Sect. 3.4. Depending on the fabrication process being used, integrated capacitors can be constructed in different ways. For example, Fig. 3.13 depicts three types of linear capacitors that are available in CMOS processes, the poly-diffusion capacitor, the double-polysilicon capacitor and the metal-polysilicon capacitor. Traditionally, a relatively thin oxide layer is deposited between the two conducting plates, leading to a large capacitance implementation. However, it can be observed that a parasitic stray capacitance exists between each plate and the substrate. Typically, the bottom-plate parasitic capacitance C_s can be approximately 10–20 % of the actual capacitance, as shown in Fig. 3.14. The presence of C_s has adverse effects on the steady state output voltage level of the charge pump, along with its efficiency. As a result, most integrated charge pump designs employ topologies in which the voltage swings at the bottom plates of the capacitors are not high.

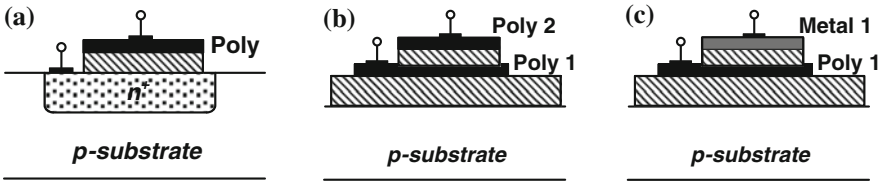

Fig. 3.13 Structures for **a** poly-diffusion, **b** double-polysilicon, and **c** metal-polysilicon capacitances

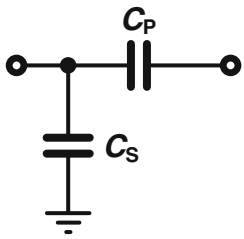

Fig. 3.14 Circuit schematic of a monolithic capacitor with its parasitic component

3.5.2 MOSFET Transistors as Switches

As discussed in Sect. 3.4, practical charge pumps employ power semiconductor devices to implement switches. For integrated charge pump designs, MOSFET transistors are commonly used. Figure 3.15 illustrates the switching behavior of a MOSFET transistor M_N. Let the initial voltage across the capacitor be zero. V_g is the gate control signal for the NMOS transistor, with an amplitude equal to V_Φ. Thus, to charge C_P, let $V_g = V_\Phi$ at time $t = t_0$. This causes M_N to turn-on, thereby charging C_P until V_{out} approaches V_{in}. For $V_\Phi \gg V_{in}$, M_N will operate in the triode region, with an effective turn-on resistance given by

$$R_{on} = \frac{1}{\mu_n C_{ox}\left(\frac{W}{L}\right)_N (V_\Phi - V_{out} - V_{TH})}. \tag{3.23}$$

Similarly, the pumping capacitor C_P can be discharged from a voltage V_{in} to zero, as illustrated in Fig. 3.16. To achieve this, at time $t = t_0$, V_g equals V_Φ to turn-on M_N. However, in this scenario, since C_P is initially charged to V_{in}, M_N will operate in the saturation region. As a result, the discharge current is limited by the V_{GS} voltage of the transistor and is given by

$$I_{dch} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_N (V_{in} - V_{TH})^2. \tag{3.24}$$

This current causes the output capacitor C_P to discharge. When V_{out} discharges below $V_{in} - V_{TH}$, M_N operates in the triode region, eventually discharging C_P to zero volts.

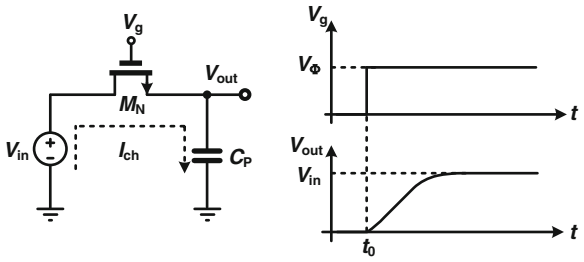

Fig. 3.15 NMOS transistor during charge operation

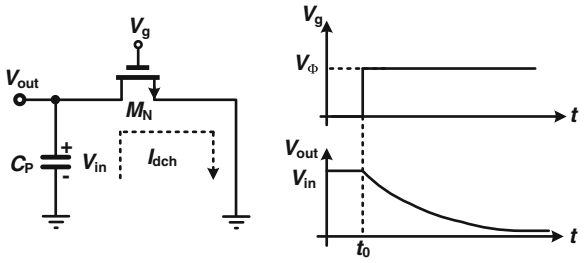

Fig. 3.16 NMOS transistor during discharge operation

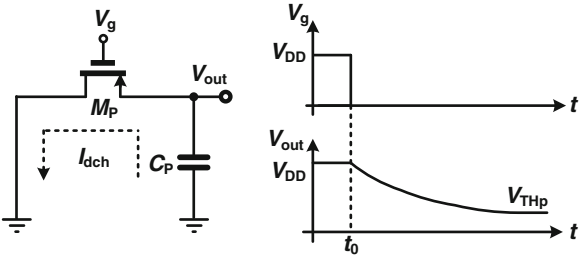

Fig. 3.17 PMOS transistor during discharge operation

From the above discussion, it can be observed that an NMOS transistor can be employed to both charge and discharge capacitors effectively. However, in the above discussion, it was assumed that $V_\Phi \gg V_{in}$. When $V_\Phi = V_{in}$, during the charge phase M_N will operate in the saturation region. However, as V_{out} approaches V_{in}, the gate to source voltage V_{gs} of M_N approaches the threshold voltage V_{TH} of the NMOS transistor. When $V_{out} = V_{in} - V_{TH}$, the transistor enters the sub-threshold region. As a result, M_N is not capable of charging the pumping capacitor to the full input voltage V_{in}. Hence, NMOS transistors can provide effective switching for charge pumps only when the upper bound voltage of V_{in} is limited to $V_\Phi - V_{TH}$.

The inability of NMOS transistor to charge capacitors to large voltages can be overcome by replacing them with PMOS transistors. From Fig. 3.17, it can be observed that the overdrive voltage for the PMOS switch M_P is $V_{out} - V_{TH}$. As a result, for large output voltages, sufficient overdrive voltage exists, thereby allowing

V_{out} to faithfully track V_{in}. However, while PMOS transistors can effectively operate as switches for charging capacitors, they face a similar issue during the discharging process. As seen from Fig. 3.17, as V_{out} discharges from a voltage V_{in}, the overdrive voltage of M_P reduces. Eventually, when $V_{out} = V_{THp}$, the overdrive voltage becomes zero, preventing further discharge of V_{out}. To overcome both of these drawbacks, a parallel connection of both NMOS and PMOS power transistors can be employed. The PMOS transistor can effectively charge the capacitors in the charge pump, while the NMOS transistors are effective during its discharge.

3.6 Conclusions

This chapter introduces fundamental topologies and operation principles in the design of charge pumps. A charge pump consists of a network of switches and capacitors, which are controlled to achieve the desired voltage conversion and power regulation. A thorough understanding of the theoretical and practical concepts of charge pump design is essential for the development of robust, area- and power-efficient SC DC–DC converters.

The chapter first introduced the concept of charge transfer, which is the primary mechanism for energy and power conversion in charge pumps. The chapter then covers various critical parameters in charge pump designs. Following this, various fundamental topologies such as the voltage inverter, the voltage doubler and the charge pump with CG = 1/2 are introduced. Practical circuit designs of these charge pumps are then discussed, with primary focus on a few well-known topologies. At last, practical implementation issues in integrated charge pump designs are investigated. The principle of employing on-chip capacitors and power switches are addressed.

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Chapter 4
Power Loss in Switched-Capacitor Power Converters: Causes and Analysis

The design of modern switched-capacitor (SC) power converters entails the generation of highly precise and efficient power supply modules, which can operate over a large range of input and output voltage levels and load power demands. The development of a highly efficient power supply should thus involve an in-depth investigation on the various power loss mechanisms in the power stage, gate drive buffers and controller. This is especially critical for the SC power converters designed for self-powered microsystems, wherein the losses should be reasonable compared to the energy harvested and load power demands.

In general, the efficiency (η) of a SC power converter can be defined as

$$\eta = \frac{P_{\text{out}}}{P_{\text{out}} + P_{\text{loss}}} \times 100\,\%, \tag{4.1}$$

where P_{out} is the output load power and P_{loss} represents the total internal power loss caused by the SC power converter itself. P_{loss} is comprised of the power losses due to the power stage, the gate drive buffer circuits and the feedback/feed-forward controller. When P_{loss} is minimized, maximum efficiency can be achieved. Among these, the power dissipated by the gate drive circuits and the controller is usually much lower than the power losses incurred by the power stage. This is due to advancements in modern semiconductor technologies, which enable the development of integrated controllers that operate at very low power. Gate drive buffers can also be designed with much smaller transistor sizes than their corresponding power switches. Hence, this chapter focuses on various power loss mechanisms in the power stage, since understanding these mechanisms is essential to maximize its efficiency. Typically, these losses can be classified as conduction loss, switching loss, redistribution loss and reversion loss. A detailed study of each power loss mechanism and their inter-relationships enables the efficiency optimization of modern SC power converters.

D. Ma and R. Bondade, *Reconfigurable Switched-Capacitor Power Converters*,
DOI: 10.1007/978-1-4614-4187-8_4,

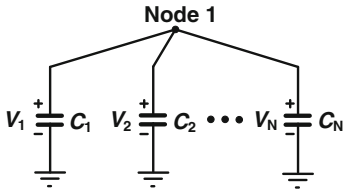

Fig. 4.1 KQL for charge transfer in a system of capacitors

4.1 Redistribution Power Loss

Redistribution loss occurs due to the fact that energy is lost when two capacitors with different voltages are connected together. To quantify the lost energy, we start with Kirchhoff's current law (KCL), which states that "*At any point in an electrical circuit where charge density is not changing in time, the sum of currents flowing towards that point is equal to the sum of currents flowing away from that point*". This law can be applied to a system of capacitors, as follows. Consider currents $I_1(t)$, $I_2(t)\ldots$ $I_N(t)$, flowing into a certain node. From KCL,

$$I_1(t) + I_2(t) + \ldots + I_N(t) = 0. \tag{4.2}$$

Integrating Eq. (4.2) leads to

$$\int_{t_1}^{t_2} (I_1(t) + I_2(t) + \ldots + I_N(t)) \cdot dt = 0 \tag{4.3}$$

Equation (4.3) can be applied to a system of capacitors that are connected to a single node, and can be stated as "*In a system of capacitors, the sum of all charges leaving a node in any instance of charge transfer is equal to zero*". This law is called as Kirchhoff's charge law (KQL) [1]. Equation (4.3) can be rewritten as

$$[Q_1(t_N) + Q_2(t_N) + \ldots + Q_n(t_N)] - [Q_1(t_{N-1}) + Q_2(t_{N-1}) + \ldots + Q_n(t_{N-1})] = 0. \tag{4.4}$$

To understand how this leads to power loss, consider Fig. 4.1, which applies KQL to a system of capacitors, C_1, $C_2\ldots C_N$, which are connected together at node 1.

Prior to charge transfer at $t = t_0$, let the voltage across each of the capacitors be $V_1(t_0)$, $V_2(t_0)$ … $V_N(t_0)$. At $t = t_1$, charge redistribution takes place. The voltages across the capacitors change to $V_1(t_1)$, $V_2(t_1)$ … $V_N(t_1)$. According to KQL,

$$C_1V_1(t_0) + C_2V_2(t_0) + \ldots + C_NV_N(t_0) = C_1V_1(t_1) + C_2V_2(t_1) + \ldots + C_NV_N(t_1). \tag{4.5}$$

A simplified version of this scenario can be described with two capacitors C_1 and C_2. The capacitors, which are initially charged to the voltages V_1 and V_2, are connected in parallel. After charge redistribution, let the capacitor voltages be V_{final}. According to Eq. (4.5), V_{final} is given by

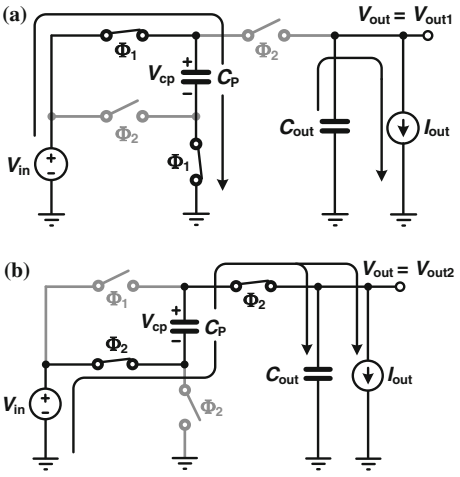

Fig. 4.2 Charge redistribution during (**a**) the charge phase and (**b**) the discharge phase in a SC voltage doubler

$$V_{\text{final}} = \frac{C_1 V_1 + C_2 V_2}{C_1 + C_2}. \tag{4.6}$$

Thus, the energy loss due to charge redistribution is

$$E_{\text{loss}} = \frac{1}{2} C_1 V_1^2 + \frac{1}{2} C_2 V_2^2 - \frac{1}{2}(C_1 + C_2) V_{\text{final}}^2. \tag{4.7}$$

Minimizing the power loss due to charge redistribution is highly critical in practical charge pump designs. This is due to the presence of a load current, which constantly draws charge from the output filter capacitor C_{out}. This causes a continuous change in the output voltage level, thereby leading to charge redistribution between the pumping capacitors and C_{out}, during each clock cycle. This operation scenario is demonstrated for a traditional voltage doubler, from which the impact of charge redistribution can be further appreciated.

In a SC voltage doubler, during the charge phase when $\Phi_1 = 1$ and $\Phi_2 = 0$, the pumping capacitor C_P is charged to the input voltage V_{in}, as illustrated in Fig. 4.2a. During the discharge phase when $\Phi_2 = 1$ and $\Phi_1 = 0$, as illustrated in Fig. 4.2b, V_{in} is connected to the bottom plate of C_P. As a result, the effective voltage at the top plate of C_P is equal to $2V_{\text{in}}$. However, V_{out} is lower than $2V_{\text{in}}$ since the output capacitor C_{out} is constantly discharged by the load current I_{out}. Hence, this voltage difference between $2V_{\text{in}}$ and V_{out} causes charge redistribution from C_P to C_{out}, leading to a redistribution power loss. To determine the power loss, let the output voltage before and after charge redistribution be V_{out1} and V_{out2}, respectively. Applying KQL at the output node gives

$$C_P V_{\text{in}} + C_{\text{out}} V_{\text{out1}} = C_P (V_{\text{out2}} - V_{\text{in}}) + C_{\text{out}} V_{\text{out2}}. \tag{4.8}$$

Note that V_{out} is taken as a constant while calculating the output voltage of the converter because $(V_{\text{out2}} - V_{\text{out1}})$ is negligible compared to its nominal value.

However, in calculating the redistribution loss, it becomes important. Once C_{out} is charged to V_{out2}, it is then discharged to V_{out1} by the load current I_{out} over one switching period. Hence, if $C_{out} \gg C_P$, the two voltages are related as

$$C_{out}(V_{out2} - V_{out1}) = I_{out}T_s. \tag{4.9}$$

Solving for V_{out2} and V_{out1} from Eqs. (4.8) and (4.9) gives

$$\begin{aligned} V_{out2} &= 2V_{in} - \frac{I_{out}}{C_P f_s}, \\ V_{out1} &= 2V_{in} - \frac{I_{out}}{C_P f_s} - \frac{I_{out}}{C_{out} f_s}. \end{aligned} \tag{4.10}$$

Thus, the redistribution loss is given by

$$P_{loss} = \frac{1}{2} f_s \left[C_P V_{in}^2 + C_{out} V_{out1}^2 - C_P (V_{out2} - V_{out1})^2 - C_{out} V_{out2}^2 \right]. \tag{4.11}$$

Hence, from Eq. (4.11), it can be observed that the redistribution power loss for a SC voltage doubler is dependent on the values of the C_P, C_{out} and f_s.

4.2 Conduction Power Loss

In SC power converters, the power switch is a fundamental device that is used to establish the necessary connections between the input power source, pumping capacitors and the output load. In the ideal scenario, these power switches are desired to operate with zero turn-on resistance. However, all practical switches are associated with an internal turn-on resistance. Due to the flow of current, the turn-on resistance leads to a conduction power loss in the SC power converter. Another source of conduction loss is the parasitic equivalent series resistance (ESR) of the pumping capacitors. Together, the conduction loss in the charge path of the typical SC power converter is given by

$$P_{loss} = \left(\sum_{i=1}^{p} ESR_{C_P} + \sum_{j=1}^{m} R_{on} \right) \cdot f_s \int_{nT}^{nT+DT} i \cdot dt, \tag{4.12}$$

where D is the duty ratio and i is the instantaneous current through the switches in the charging path. R_{on} is the turn-on resistance of the power switches, while ESR_{Cp} is the equivalent series resistance of the pumping capacitor. Using a similar method, the conduction loss can be calculated in the discharge path. By adding both the charge and discharge path conduction loss, the total conduction loss of the system can be determined.

Equation (4.12) provides the conduction power loss for a general switch implementation. However, as discussed in Chap. 2, modern power supply designs

can employ different switch implementations. A widely used switch implementation for SC power converters is the MOSFET transistor, for which the total conduction loss can be determined. When turned on, these transistors are operated in the linear region where the current–voltage relationship is given by [2]

$$I_{\mathrm{D}} \approx \mu C_{\mathrm{ox}} \frac{W}{L}(V_{\mathrm{GS}} - V_{\mathrm{TH}})V_{\mathrm{DS}}, \tag{4.13}$$

where I_{D} is the drain current, μ is the mobility of the majority charge carriers (electrons for NMOS and holes for PMOS transistors), C_{ox} is the gate-oxide capacitance, W and L are the width and length of the transistor, respectively, V_{TH} is the threshold voltage, V_{GS} is the gate to source voltage and V_{DS} is the drain to source voltage of the transistor. This equation implies a linear relationship between V_{DS} and I_{D}. This indicates that the path from the drain to the source can be modeled by a resistor, whose resistance is controlled by V_{GS}. The resistance is calculated to be

$$R_{\mathrm{on}} = \frac{1}{\mu C_{\mathrm{ox}} \frac{W}{L}(V_{\mathrm{GS}} - V_{\mathrm{TH}})}. \tag{4.14}$$

A flow of current through the transistor thus leads to conduction loss, due to R_{on}. Thus, for example, the conduction loss in the charge path of a traditional SC voltage doubler is given by

$$P_{\mathrm{loss}} = \left(ESR_{C_{\mathrm{P}}} + \frac{1}{\mu C_{\mathrm{ox}}} \sum_{i}^{i=1,2} \frac{1}{\frac{W_i}{L_i}(V_{\mathrm{GS}} - V_{\mathrm{TH}})} \right) \cdot f_s \int_{nT}^{nT+DT} i \cdot dt, \tag{4.15}$$

If the drain current I_{D} and switch sizes are assumed to be constant and for a low ESR pumping capacitor, the conduction loss can be expressed as

$$P_{\mathrm{loss}} = \frac{I_{\mathrm{D}}^2 D}{\mu C_{\mathrm{ox}} \frac{W}{L}(V_{\mathrm{GS}} - V_{\mathrm{TH}})}. \tag{4.16}$$

From Eq. (4.16), it can be observed that the conduction loss in MOSFET switches can be minimized by increasing the width of the transistors. However, this has a conflicting effect on the switching power loss of the transistor, which will be discussed next.

4.3 Switching Power Loss

As discussed in Sect. 4.2, one technique to minimize conduction losses in SC power converters with MOSFET switches is to increase the width of the power transistor, which effectively reduces the turn-on resistance R_{on}. However, this design strategy has an adverse effect on the switching power loss of the charge pump.

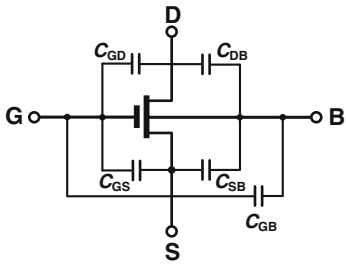

Fig. 4.3 Parasitic capacitances in a MOSFET transistor

For a MOSFET transistor, switching power loss is incurred due to the charge and discharge mechanisms of the parasitic capacitances. As illustrated in Fig. 4.3, MOSFETs are associated with various parasitic capacitances [3]. Of these, the gate-to-source parasitic capacitance C_{GS} dominates the switching behavior of the transistor and contributes significantly to this power loss component. The switching power loss due to C_{GS} is given by

$$P_{\text{loss,C}_{GS}} = f_s \sum_i C_{GS,i} \cdot V_{GS,i}^2 = f_s C_{ox} \sum_i W_i L_i \cdot V_{GS,i}^2, \tag{4.17}$$

where $C_{GS,i}$ and $V_{GS,i}$ are the gate-source capacitance and voltage swing at the gate of the power transistor i. From Eq. (4.17), it can be seen that the switching power loss for a MOS transistor is directly proportional to the width and length of the transistor. A larger width leads to a higher gate-source capacitance and more parasitics. Hence, from the perspective of switching power loss, it is not desirable to choose a very large size for the power transistor.

Thus, the size of the power switch is critical in optimizing the efficiency of the SC power converter. From the above discussion, it is observed that the conduction power loss and the switching power loss have opposing trends with respect to the size of the power switch. As a result, there exists an optimal size W_{opt} for each switch in the SC power converter, which can minimize the total power loss. This is determined when the condition, $\partial P_{tot}/\partial W_i = 0$, is satisfied. The value of W_{opt} is highly determined by parameters such as the configuration of the charge and discharge paths, the input and output voltages, the load current and the switching frequency. Thus, by carefully designing and optimizing the size of the power switches, it is possible to minimize the sum of the switching and conduction losses in a SC power converter.

4.4 Reversion Power Loss

The fourth type of power loss in SC power converters is reversion loss. This type of loss occurs when shorting a node at a higher potential to a second node at a lower voltage. This leads to a reversion current, which is opposite to that of the original power flow. Hence, it is similar to redistribution power loss, but with a

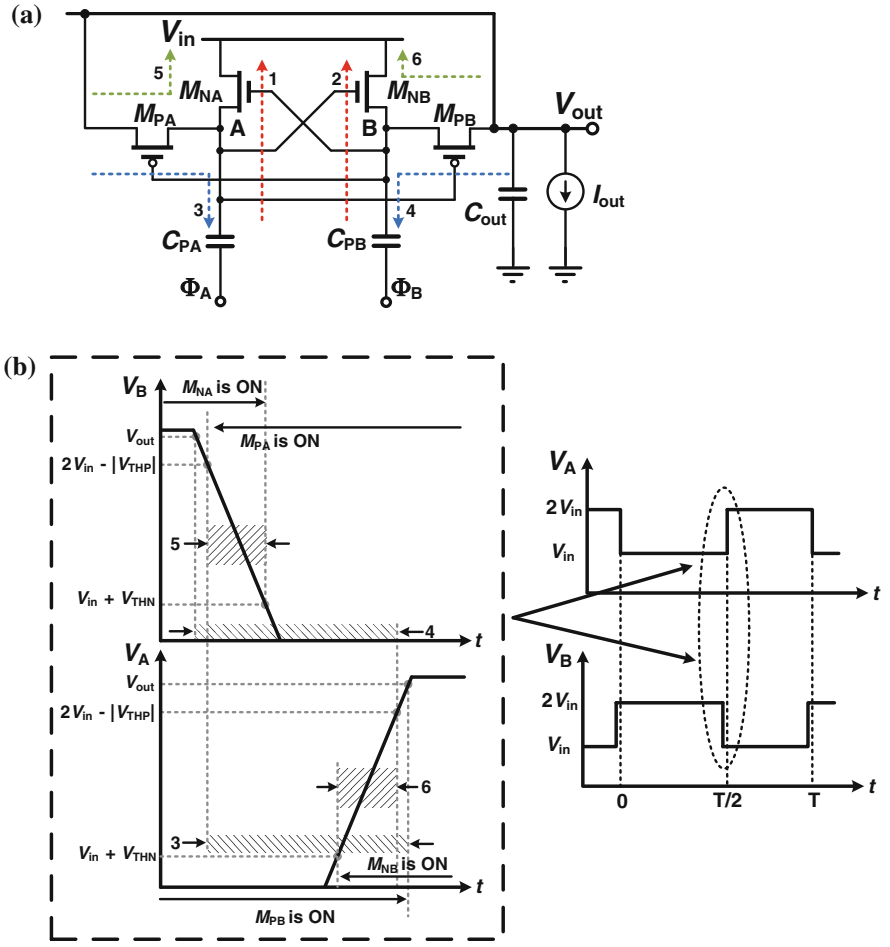

Fig. 4.4 **a** Reversion shoot-through current generation in cross-coupled voltage doubler and **b** its switching waveforms

reverse current flow. An example is demonstrated for a conventional cross-coupled voltage doubler, in Fig. 4.4. It can be observed that when Φ_A and Φ_B are both low, voltages V_A and V_B are equal to the input voltage V_{in}. This causes the PMOS transistors M_{PA} and M_{PB} to be turned on, while the NMOS power switches M_{NA} and M_{NB} are both turned off. As shown in Fig. 4.4a, reverse shoot-through currents 3 and 4 are generated, which flow from V_{out} through M_{PA} and M_{PB} and back to C_{PA} and C_{PB}. This leads to the degradation of the efficiency of the charge pump. The reversion power loss due to the shoot-through current can be determined by applying KQL to the charge pump,

$$V_{in}C_{PA} + V_{out}C_{out} + V_{in}C_{PB} = V_{out2}(C_{PA} + C_{out} + C_{PB}), \tag{4.18}$$

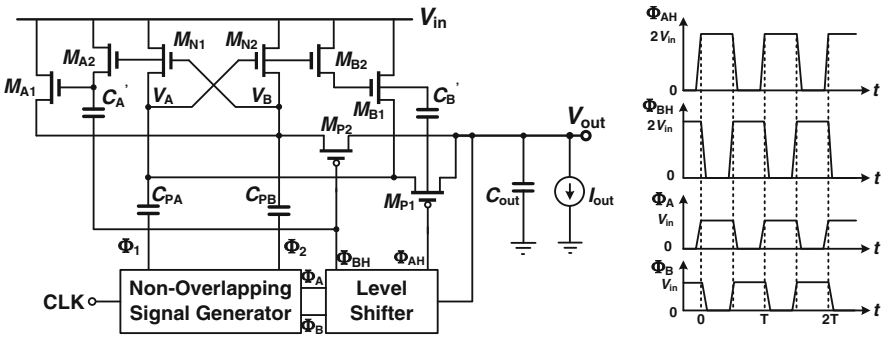

Fig. 4.5 Cross-coupled voltage doubler with gate-drive enhancement

where V_{out2} is the voltage across the pumping and output capacitors after charge redistribution. If $C_{PA} = C_{PB} = C_P$, then the total reversion power loss can be expressed as

$$P_{loss} = f_s C_P V_{in}^2 + \frac{1}{2} f_s C_{out} V_{out}^2 - \frac{1}{2} f_s (2C_P + C_{out}) V_{out2}^2. \tag{4.19}$$

From Eqs. (4.18) and (4.19), it can be shown that the reversion loss due to this shoot-through current is equal to

$$P_{loss} = f_s \frac{C_P C_{out}}{2C_P + C_{out}} (V_{out} - V_{in})^2, \tag{4.20}$$

where $V_{out} \approx 2V_{in}$. Thus, $V_{out} - V_{in} \approx V_{in}$, which causes this reversion loss component to be much larger than the redistribution loss in Eq. (4.12). Figure 4.4b also indicates that in the shaded region 5 and region 6, the reverse shoot-through current leaks from V_{out} through M_{PA} and M_{NA} (M_{PB} and M_{NB}) to the input supply, during the simultaneous conduction. This leads to a large reversion power loss, which has to be minimized in order to obtain high efficiency.

In summary, power losses in the power stage of a SC converter can occur through four major mechanisms: conduction loss, switching loss, redistribution loss and reversion loss. Significant research effort has been invested in order to minimize these power loss components, thereby obtaining state-of-the-art power supplies for advanced self-powered microsystems.

4.5 Practical Case Studies

While Sects. 4.1–4.4 focused on different causes of power loss in SC power converters, this section will investigate various power loss mechanisms that are observed in practical SC power converter designs. The discussion will use cross-coupled SC power converters and voltage doublers as examples.

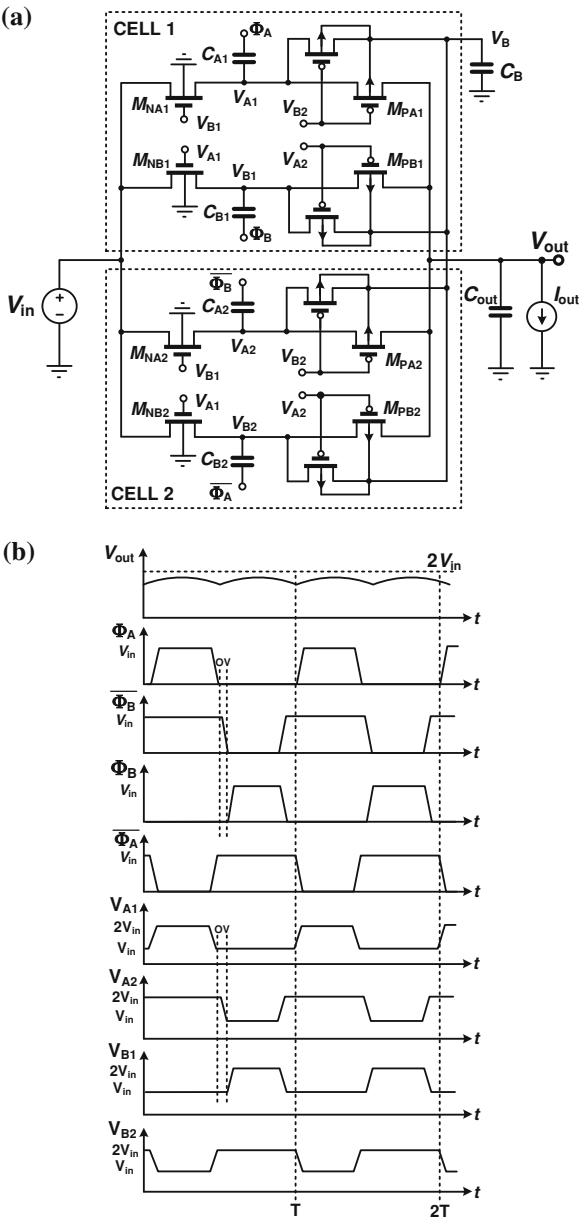

Fig. 4.6 **a** Complementary cross-coupled voltage doubler and **b** timing diagram with non-overlapping control signals

To improve the efficiency of the cross-coupled voltage doubler, a few new charge pump topologies have been proposed. A cross-coupled voltage doubler is presented in [4] and shown in Fig. 4.5, is an enhanced version of the traditional cross-coupled voltage doubler. In the traditional cross-coupled voltage doubler

illustrated in Fig. 4.4a, the transistors M_{PA} and M_{PB} are driven by control signals V_B and V_A, respectively. Both these signals swing between V_{in} and $2V_{in}$. From the expression for conduction loss in Eq. (4.16), it can be observed that the conduction loss in the PMOS transistor pair can be reduced with higher gate overdrive voltages. Hence, in [4], a new pair of gate control signals Φ_{AH} and Φ_{BH} is employed. These signals swing between 0 and $2V_{in}$, by using a level shifter, thereby reducing the conduction loss considerably.

However, the major drawback with this design is the resulting increase in the switching power loss. From Eq. (4.17), it can be observed that an increase in the V_{GS} voltage swing leads to a considerable increase in the switching loss of the PMOS transistor pair. Moreover, no additional circuit design techniques were applied to minimize reversion loss. Lastly, in order to drive the PMOS power transistors, two additional buffers and level shifters are required, leading to an increase in silicon area and power consumption.

To reduce reversion loss, a charge pump topology is proposed in [5] and depicted in Fig. 4.6. It consists of two identical cross-coupled voltage doubler cells that are connected in parallel between V_{in} and V_{out}. All NMOS switches are controlled by the clock signals Φ_A and Φ_B, while the PMOS switches are managed by their complementary clock counterparts Φ'_A and Φ'_B. To reduce reversion loss, the operation of the charge pump is as follows. As shown in the timing diagram in Fig. 4.6b, it can be observed that a non-overlapping period exists between the charge and discharge phases in each sub-cell. In this period, both the clocks Φ_A and Φ_B are low.

As a result, V_{A1} and V_{B1} are equal to V_{in}, while V_{A2} and V_{B2} are charged to $2V_{in}$. Hence, all the power switches are effectively turned off. Since a reverse current path does not exist, charge cannot be transferred from V_{A2} and V_{B2} (from C_{A2} and C_{B2}) back to V_{in}, or from C_{out} back to V_{A1} and V_{B1} (C_{A1} and C_{B1}). Reversion loss is thus substantially reduced. Nevertheless, this loss still exists during simultaneous transitions.

4.6 Conclusions

Minimizing the power loss in the charge pump of a SC power converter is essential to maximize its efficiency. Hence, this chapter discusses the four major power loss components, which are the conduction loss, switching loss, redistribution loss and reversion loss. A detailed study of each power loss component and their interdependencies enables the efficiency optimization of modern SC power converters. Following the discussion of each of these power loss components, the chapter further discusses power loss mechanisms in practical SC power converters, with emphasis on various cross-coupled voltage doubler topologies.

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Chapter 5
Reconfigurable Switched-Capacitor Power Converters

The proliferation of self-powered devices and implantable biomedical microsystems has led to the growth of highly-efficient, multi-mode power supply designs. SC power converters are invaluable to such applications since they enable robust operation at ultra-low-power levels, enhance the operation lifetime and achieve monolithic implementation, thereby reducing the size, cost and PCB footprint of the overall system.

However, certain new challenges are introduced in such a power system due to the unique operation environment and design specifications. To understand this, first consider the expression for the efficiency of a SC power converter. If all the power losses, such as redistribution loss, conduction loss and switching loss in the power stage, buffer and controller are neglected, the efficiency is given by

$$\eta = \frac{V_{\text{out}}}{\text{CG} \cdot V_{\text{in}}}, \tag{5.1}$$

where V_{in} and V_{out} are the input and output voltages, respectively and CG is the conversion gain of the SC power converter. As described in Chap. 1, modern self-powered systems scavenge energy from the ambient environment, through sources such as solar, vibration energy, heat, etc. The power generated through these energy harvesting mechanisms is quite low and the voltage levels can fluctuate largely due to the varying intensity and availability of the energy sources. Hence, even for a fixed V_{out}, the efficiency can change considerably due to the fluctuating input voltage level, as observed from Eq. (5.1).

In addition, in order to effectively utilize the limited harvested energy, self-powered devices are operated under various power management techniques, such as DVFS. This requires the adaptive variation of V_{out} with respect to the instantaneous operating conditions, such as the system workload. However, one of the major drawbacks with traditional SC power converters is their ability to provide only a constant CG. If V_{out} deviates from this desired level, due to a change in the reference voltage, the efficiency of a SC converter drops. If the

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variation is large, the power loss becomes unacceptably high due to charge redistribution. Hence, to accommodate a large input and output voltage range and to be capable of powering DVFS-based applications, a SC converter with a fixed CG is insufficient and impractical. To overcome this drawback, state-of-the-art SC power converter designs involve the use of integrated, reconfigurable power stages to supply a variable output voltage, for varying input voltage levels. Based on the instantaneous operating conditions, these modern SC converters are capable of undergoing dynamic reconfiguration into the optimal power stage topology. This minimizes their power losses and provides enhanced power regulation.

Accordingly, this chapter discusses various reconfigurable SC power converter designs. Each power converter is discussed in detail, with regards to system architecture, control schemes, power stage reconfiguration mechanisms and design strategies.

5.1 Topologies and Optimization Strategies

To begin the discussion on reconfigurable SC power converters, this section presents key design principles involving reconfigurable charge pump topologies and control strategies. In order to accommodate variable input and output voltages, a SC converter's power stage must be reconfigurable with variable CGs to achieve high efficiency. Few research efforts have been reported on this subject. Although the prior arts in [1–3] can provide multiple CGs, similar to traditional SC doublers, they suffer from high output voltage ripples, a large input in-rush current and slow transient response. For example, the power regulation scheme of the reconfigurable SC power converter in [1] is illustrated in Fig. 5.1, using a CG of 3/2 as an example. It can be observed that the converter operates in two phases. During the phase $\Phi_1 = 1$, the pumping capacitors C_{P1} and C_{P2} are connected in series across V_{in}. If C_{P1} and C_{P2} are identical, each capacitor is pre-charged to $V_{in}/2$. During the phase $\Phi_2 = 1$, C_{P1} and C_{P2} are connected in parallel between V_{in} and V_{out}. The output capacitor C_{out} is charged to $3/2V_{in}$ ($=V_{in} + V_{in}/2$). However, some of the drawbacks associated with this design are: (1) the separation of the charge and discharge paths leads to large current and voltage ripple problems, and (2) the capacitor C_{P3} remains idle during the entire operation. To overcome these issues, a generic multi-gain step-up/down SC power converter is presented, along with a systematic study on the charge pump topology and an interleaving regulation scheme for closed loop operation.

Figure 5.2 illustrates the operation of the interleaving regulation scheme, which is used to overcome the drawbacks of large output voltage ripple and in-rush current. In this scheme, the charge pump is regulated in three different phases, which are controlled by clock signals Φ_1, Φ_2 and Φ_3, with a phase difference of 120^o. The interleaving regulation scheme can be described for a CG of 3/2. During phase $\Phi_1 = 1$, the charge pump follows the same operation as described in Fig. 5.1, wherein C_{P1} and C_{P2} are connected in series and pre-charged to $V_{in}/2$.

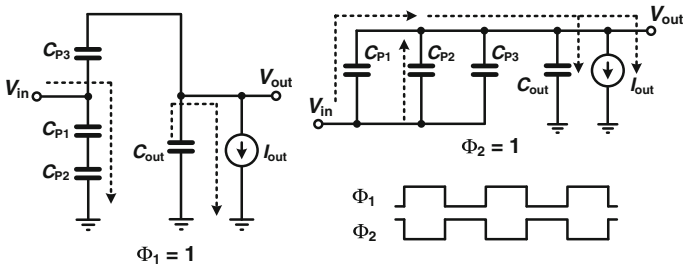


Fig. 5.1 Power regulation scheme to provide a CG of 3/2 [1]

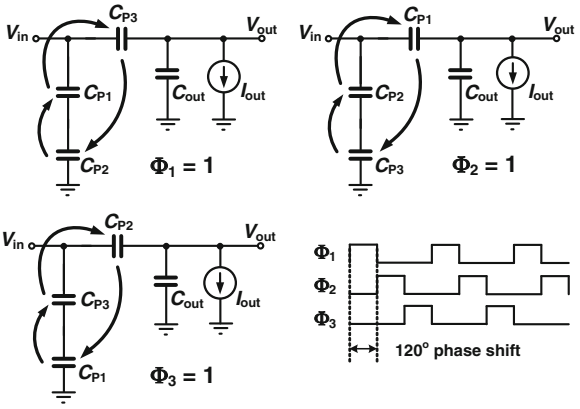


Fig. 5.2 Interleaving regulation scheme for the multi-gain SC power converter

However, during phase $\Phi_2 = 1$, instead of keeping C_{P3} idle, the charge pump undergoes dynamic reconfiguration. The pumping capacitor C_{P1} is connected between V_{out} and V_{in} and delivers charge to C_{out}, while C_{P2} and C_{P3} are pre-charged to $V_{in}/2$. Similarly in phase $\Phi_3 = 1$, C_{P2} delivers charge to C_{out} while C_{P1} and C_{P3} are pre-charged to $V_{in}/2$. Hence, the output voltage V_{out} is regulated at $3/2V_{in}$. Moreover, there always exist two pre-charged capacitors that are capable of immediate power delivery to the output during any clock phase. This continuous pre-charge operation leads to continuous input charge current and thus low in-rush current ripple. Meanwhile, the presence of the third pumping capacitor that powers C_{out} during each clock phase leads to a continuous output discharge current. This reduces the output voltage ripple and ensures a fast load transient response.

As shown in Fig. 5.3, a reconfigurable power stage design is proposed to facilitate the interleaving regulation mechanism. In general, the circuit consists of a switch-capacitor array. Each of the capacitors in the array is associated with six switches, which can flexibly connect either of the plates of the capacitor to V_{in}, V_{out} or another capacitor. For example, the top plate of C_{P1} can be connected to V_{in} by S_{11}, to V_{out} by S_{12}, or to the bottom plate of C_{PN} by S_{16}. Meanwhile, the bottom plate of C_{P1} can be connected to V_{in} by S_{13}, to V_{out} by S_{14}, to the top plate of C_{P2} by S_{26}, or to ground by S_{15}.

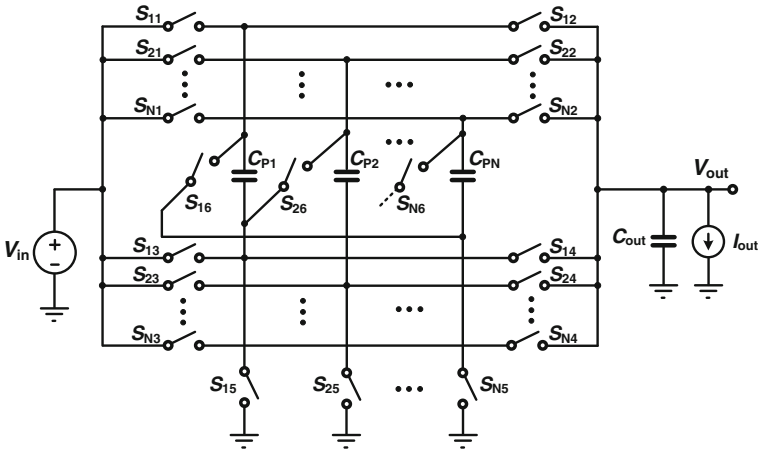


Fig. 5.3 Generic architecture of the multi-gain reconfigurable SC power converter

In general, with N pumping capacitors and $6N$ switches, the converter can achieve $4N - 5$ different CGs, with the options of 1 to N interleaving phases. For step-up conversions, the CG can be represented as i/j, where j = 1, 2… N, and $i = j, j + 1 \ldots N$. For step-down voltage conversions, the CG can be represented as i/j, where $j = 1, 2 \ldots N$, and $i = 1, 2 \ldots j$. In practical implementations, in order to reduce the number of switches, this generic architecture can be simplified to satisfy application requirements. For example, if only step-down conversions are needed, the switches S_{i3} can be eliminated, where $i = 1, 2 \ldots N$. The SC power converter then offers $2N - 2$ step-down CGs with N capacitors and $5N$ switches. Similarly, the switches S_{i4} can be removed for if only step-up conversions are required. In this case, the charge pump can provide $2N - 3$ CGs with N capacitors and 5 N switches, where $i = 1, 2 \ldots N$. Compared to the prior arts, this architecture achieves more CG options.

To address the major design strategies and optimization issues, Fig. 5.4 demonstrates the detailed reconfiguration mechanism of the SC power converter. As an example, the power stage is designed to have $N = 3$ pumping capacitors. However, the system design methodology is generic to charge pumps with any number of capacitors. As discussed earlier, with three pumping capacitors, the SC power converter can achieve 7 CGs (1/3, 1/2, 2/3, 1, 3/2, 2 and 3).

To optimize the design of the SC power converter, the charge and discharge behavior of the pumping capacitors have to be analyzed, since it directly affects the regulation performance. If the capacitance of each pumping capacitor in Fig. 5.4 is equal to C_P, then as depicted in Fig. 5.5, C_P is charged and discharged exponentially from V_H to V_L during the charge time t_c and discharge time t_d, respectively. The net charge (ΔQ) that is delivered to the load I_{out} is given as

$$\Delta Q = C_P(V_H - V_L) = C_P \Delta V_{CP} = \alpha I_{out} T_s, \tag{5.2}$$

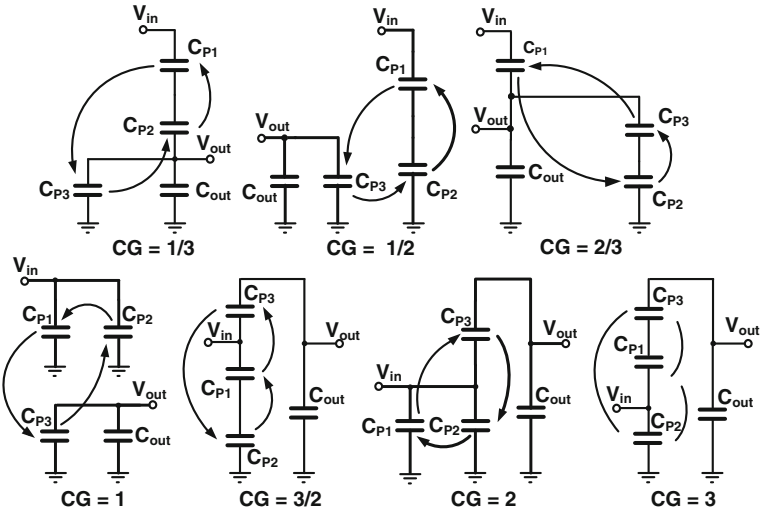


Fig. 5.4 Different CG configurations of the reconfigurable SC power converter

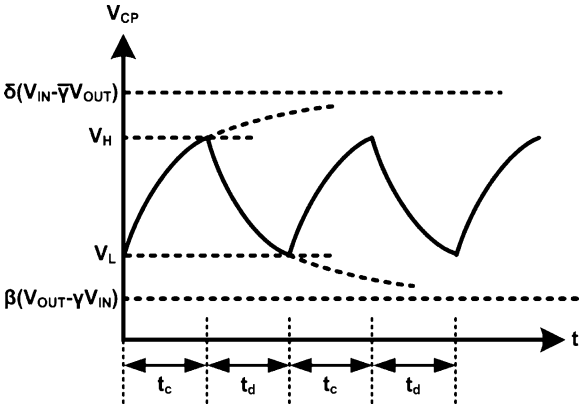


Fig. 5.5 Typical voltage waveform observed across one pumping capacitor C_P

where α is the capacitor charge multiplier vector of the corresponding CG and T_s is the switching cycle. The boundary voltages V_H and V_L are given as

$$V_L = V_H - [V_H - \beta(V_{out} - \gamma V_{in})]\left(1 - e^{-t_d/\tau_d}\right) \text{ and} \tag{5.3}$$

$$V_H = V_L + [\delta(V_{in} - \zeta V_{out}) - V_L]\left(1 - e^{-t_c/\tau_c}\right), \tag{5.4}$$

where $t_c = D{\cdot}T_s$ and $t_d = (1 - D){\cdot}T_s$ and D is its duty ratio. τ_c and τ_d represent the respective charge and discharge time constants, which are determined by the equivalent path resistance and capacitance. The parameters β, γ, δ, and ζ are circuit

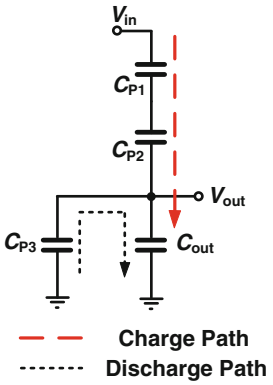


Fig. 5.6 Power stage configuration for CG of 1/3

related coefficients that are determined by the CG configurations. For example, consider the CG of 1/3, which is illustrated in Fig. 5.6. During the charge phase, if $t_c \gg \tau_c$, then the capacitors C_{P1} and C_{P2} on the charge path are each charged to a voltage of V_H given by

$$V_H = \frac{V_{in} - V_{out}}{2}. \tag{5.5}$$

From Eq. (5.4), this voltage is defined as

$$V_H = V_L + [\delta(V_{in} - \zeta V_{out}) - V_L] = \delta(V_{in} - \zeta V_{out}). \tag{5.6}$$

Based on the structure of the power stage at a CG of 1/3, the two conditions are satisfied when $\delta = 1/2$ and $\zeta = 1$. Similarly, during the discharge phase, if $t_d \gg \tau_d$, then C_{P3} discharges until the voltage $V_L = V_{out}$. From Eq. (5.3), this voltage is defined as

$$V_L = V_H - [V_H - \beta(V_{out} - \gamma V_{in})] = \beta(V_{out} - \gamma V_{in}). \tag{5.7}$$

The voltage V_L in Eq. (5.7) is equal to V_{out} when β= 1 and $\gamma = 0$. To determine the remaining parameters, a transistor-based implementation of generic architecture of Fig. 5.3 has been designed, and is illustrated in Fig. 5.7.

To achieve CG = 1/3, 3 pumping capacitors and a 3-phase interleaving regulation are employed. For instance, as depicted in Fig. 5.7a, during the phase $\Phi_1 = 1$, the capacitor C_{P1} is connected to V_{out} by the transistors M_{P12}, M_{N12} and M_{N15}, and delivers charge to the output V_{out}. Meanwhile, C_{P2} and C_{P3} are charged between V_{in} and V_{out}, through a charge path formed with the transistors M_{P21}, M_{P36}, M_{N36}, M_{P34} and M_{N34}. In the next phase $\Phi_2 = 1$ as shown in Fig. 5.7b, the capacitors are reconfigured. C_{P2} is connected to V_{out}, while C_{P1} and C_{P3} are charged between V_{in} and V_{out}. Lastly, as illustrated in Fig. 5.7c during phase $\Phi_3 = 1$, similar reconfiguration takes place. Capacitor C_{P1} and C_{P2} are charged by connected them between V_{in} and V_{out}, while C_{P3} is discharged to V_{out}. As a result, each capacitor is charged between V_{in} and V_{out} for 2/3 of a switching cycle. Hence, the duty ratio D is 2/3. In addition, the total output charge Q_{out} is defined as

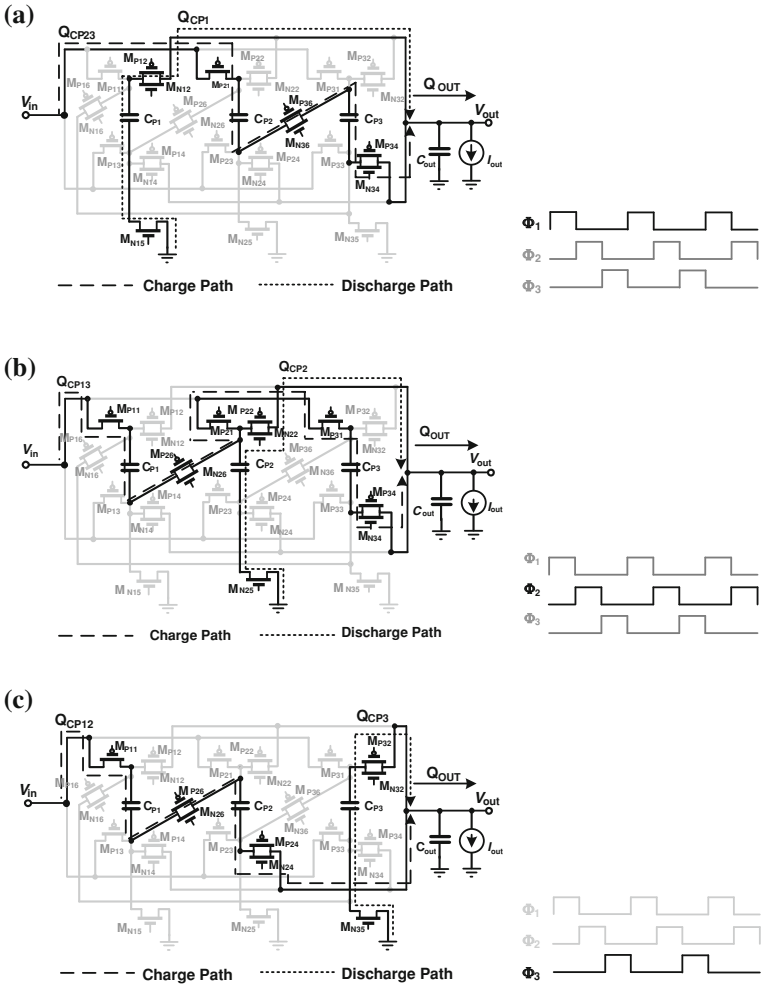


Fig. 5.7 Circuit schematic of the multi-gain charge pump with CG = 1/3, during different operation phases

$$Q_{\text{out}} = Q_{\text{CP1}} + Q_{\text{CP23}}, \tag{5.8}$$

where,

$$Q_{\text{CP1}} = \Delta Q, \quad \text{and} \quad Q_{\text{CP2,CP3}} = \frac{1}{2} C_{\text{P}} \Delta V_{\text{CP}}.$$

As a result, the parameter α is given by

$$\alpha = \frac{\Delta Q}{Q_{\text{OUT}}} = \frac{C_{\text{P}} \Delta V_{\text{CP}}}{C_{\text{P}} \Delta V_{\text{CP}} + \frac{1}{2} C_{\text{P}} \Delta V_{\text{CP}}} = \frac{2}{3}. \tag{5.9}$$

Table 5.1 CG configuration parameters

CG	1/3	1/2	2/3	1	3/2	2	3
α	2/3	1/2	1/3	1	1	1	1
β	1	1	½	1	1	1	1/2
γ	0	0	0	0	1	1	1
ζ	1	1	1	0	0	0	0
δ	1/2	1	1	1	1/2	1	1
D	2/3	2/3	1/3	2/3	2/3	2/3	1/3

The values of the parameters α, β, γ, δ, ζ and D for the remaining CG configurations are illustrated in Table 5.1.

To optimize the power stage design of the reconfigurable SC power converter, the power losses have to be identified. The output voltage of the converter can be expressed as

$$V_{\text{out}} = \frac{\beta\gamma + \delta}{\beta + \delta\zeta} V_{\text{in}} - \frac{\alpha I_{\text{out}} t_{\text{d}}}{(\beta + \delta\zeta) C_{\text{P}}} \left(\frac{1}{1 - e^{-t_{\text{d}}/\tau_{\text{d}}}} + \frac{1}{1 - e^{-t_{\text{c}}/\tau_{\text{c}}}} - 1 \right). \tag{5.10}$$

Hence, the redistribution power loss due to the deviation of V_{out} from its nominal value is

$$P_{\text{D}} = \frac{\alpha I_{\text{out}}^2 t_{\text{d}}}{(\beta + \delta\zeta) C_{\text{P}}} \left(\frac{1}{1 - e^{-t_{\text{d}}/\tau_{\text{d}}}} + \frac{1}{1 - e^{-t_{\text{c}}/\tau_{\text{c}}}} - 1 \right). \tag{5.11}$$

Another major power loss component is the switching loss P_{sw} of the power transistors. It is dependent on the sizes of the power transistors and the quiescent current of the operating circuit. It is given by

$$P_{\text{sw}} = \sigma f_{\text{S}} C_{\text{ox}} \sum_{\text{j}=1}^{6N} L_{\text{j}} W_{\text{j}} V_{\text{GS(j)}}^2. \tag{5.12}$$

Here, C_{ox} is the gate oxide capacitance. L_{j} and W_{j} represent the length and width of the power transistor j, respectively. V_{GS} is the gate-to-source voltage of the transistor, σ is the fabrication process related coefficient and N is the number of the pumping capacitors in the power stage. To reduce the parasitic capacitance and thus the switching loss, the length of each power transistor is chosen as the minimum value L_{min}. Thus, the total loss in the power stage can be expressed as

$$P_{\text{loss}} = \frac{\alpha I_{\text{out}}^2 t_{\text{d}}}{(\beta + \delta\zeta) C_{\text{P}}} \left(\frac{1}{1 - e^{-t_{\text{d}}/\tau_{\text{d}}}} + \frac{1}{1 - e^{-t_{\text{c}}/\tau_{\text{c}}}} - 1 \right) + \sigma f_{\text{s}} C_{\text{ox}} L_{\text{min}} \sum_{\text{j}=1}^{6N} W_{\text{j}} V_{\text{GS(j)}}^2. \tag{5.13}$$

Note that τ_{c} and τ_{d} are dependent on the turn-on resistance of the charge/discharge path R_{on}, which is given by,,

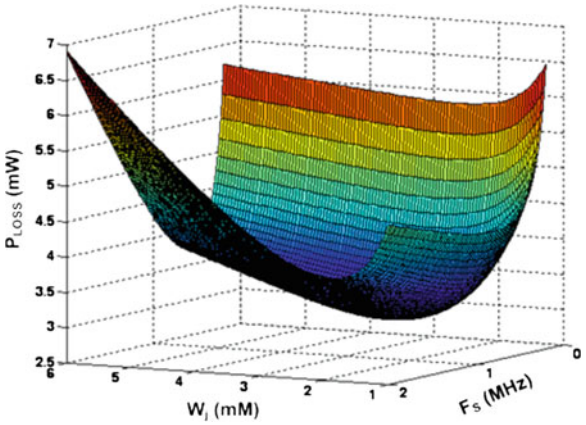


Fig. 5.8 Plot of power loss P_{loss} versus W_{j} and f_{S} for CG = 3/2

$$R_{\text{on}} = \sum_{\text{j}=1}^{m} \frac{L_{\min}}{\mu_{\text{eff}} C_{\text{ox}} W_{\text{j}} \left(V_{\text{GS(j)}} - V_{\text{TH}}\right)}. \tag{5.14}$$

In Eq. (5.14), m is the total number of the power transistors in the charge/discharge path. Equations (5.13) and (5.14) reveal that the total power loss in the power stage is highly dependent on the values of f_{s} and W_{j}. Hence, in order to minimize the power consumption and maximize the efficiency, f_{s} and W_{j} should be optimized based on the lowest P_{loss}. This is illustrated in Fig. 5.8.

However, the power loss plot in Fig. 5.8 only represents the case when CG = 3/2. When the value of CG changes, the circuit has to be reconfigured accordingly, resulting in different turn-on resistances. If the initial optimal values for parameters W_{j} and f_{s} remain unchanged, the power loss would increase and the efficiency would drop. Hence, for the reconfigurable SC power converter, the parameters such as f_{s} and W_{j} should also be adjusted with reference to the CG value.

Figure 5.9 shows a design example for a 3-pumping capacitor SC power converter. With 7 different CG values, the operation of the converter is divided into 7 regions. The parameters of f_{s} and W_{j} are optimized within each region individually.

In conclusion, this section discusses a topology and reconfiguration control scheme for an integrated step-up SC power converter. While the circuit implementation employs 3 pumping capacitor to provide 7 CGs, it is generic to a charge pump with N pumping capacitors. Moreover, as the charge pump employs an interleaving regulation scheme with multiple-phase gain reconfiguration, it aids in reducing the input current ripple, output voltage ripple and improves the system bandwidth. It allows the converter to flexibly provide either step-up or step-down voltage conversion.

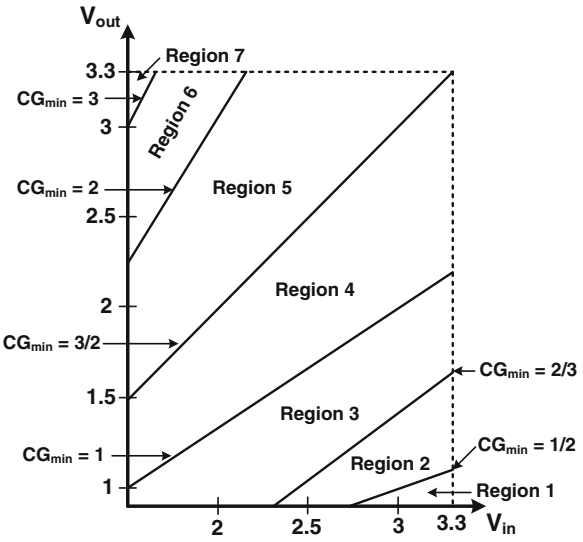


Fig. 5.9 Optimal operating regions based on the CGs

5.2 Signal Flow Graph Modeling

Reconfigurable SC power converters are capable of operating under multiple CG topologies. This enables the power supply to operate over fluctuating input voltages and be capable of supplying multiple output voltage levels for DVS-based applications. However, the use of a highly reconfigurable power stage significantly increases the number of power components, such as the pumping capacitors and power switches, along with the complexity of the controller. This introduces considerable challenges during the topology and efficiency optimization of SC power converters.

To overcome this design hurdle, this section introduces a systematic design approach to model and derive reconfigurable SC power converters. With the assistance of a signal flow graph (SFG) model, the reconfiguration algorithm can be optimized to achieve multiple desired voltage CGs, with highly-efficient energy delivery and minimized number of power components. The developed SFG model also allows small-signal analysis to be conducted at different reconfiguration scenarios.

5.2.1 SFG Modeling and Design Approach

SFG techniques have been applied to switch mode power converter designs to analyze and evaluate both large-signal and small-signal characteristics as well as stability conditions. In this section, a SFG is developed for SC power converters.

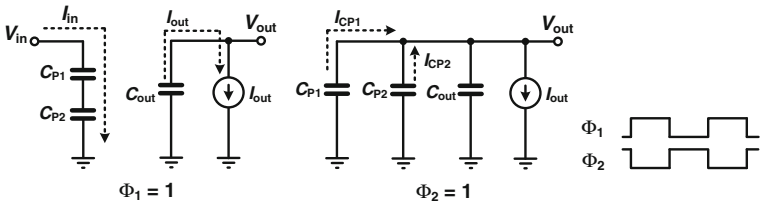


Fig. 5.10 Pumping capacitor configurations to obtain CG = 3/2

The SFG modeling is implemented under the following assumptions: (1) all power switches are assumed to be ideal; (2) passive components (pumping and output filtering capacitors) are assumed to be linear and time-invariant; (3) equivalent series resistance (ESR) of capacitors is neglected.

The first step of the SFG modeling is to define every node in the graph. In general, from the discussion on charge pump topologies in Sect. 5.1, it is known that in order to achieve $2N + 1$ CGs in a SC power converter, N pumping capacitors C_{P1}, C_{P2}, …, C_{PN} are needed. Thus, there will be $2N + 4$ nodes in the SFG, which are the input voltage and current (V_{in} and I_{in}) nodes, output voltage and current (V_{out} and I_{out} nodes, where I_{out} = current flowing into the output filtering capacitor + load current), voltage across and current flowing through each pumping capacitor (V_{CPi} and I_{CPi} ($i = 1, 2\ldots N$)). For example, if we choose $N = 2$ to achieve 5 CGs, the SFG then includes 8 nodes.

In order to model this charge pump using a SFG, the first step is to create the correct connections between the nodes. These connections in general represent different charge/discharge paths in the SC power converter, which will provide the different CGs. For example, of the 5 CGs that can be delivered by the charge pump, let us consider the capacitor configurations for which CG = 3/2. To regulate V_{out} appropriately, the two pumping capacitors C_{P1} and C_{P2} have to be connected in series between V_{in} and ground during the charge phase $\Phi_1 = 1$, as illustrated in Fig. 5.10. During the discharge phase $\Phi_2 = 1$, the pumping capacitors are connected in parallel between V_{in} and V_{out}. Using the SFG approach, it is now possible to construct a power stage employing the fewest number of power devices.

The SFGs for both these phases can be obtained as shown in Fig. 5.11. The transmittance for each branch (established connection) can then be found by applying both Kirchhoff's current law (KCL) and Kirchhoff's voltage law (KVL). During the phase $\Phi_1 = 1$, the KCL/KVL equations are given as

$$\begin{cases} V_{in} = V_{CP1} + V_{CP2} \\ I_{in} = I_{CP1} = I_{CP2}. \end{cases} \tag{5.15}$$

The voltage and current relationship at each node can be expressed as given by

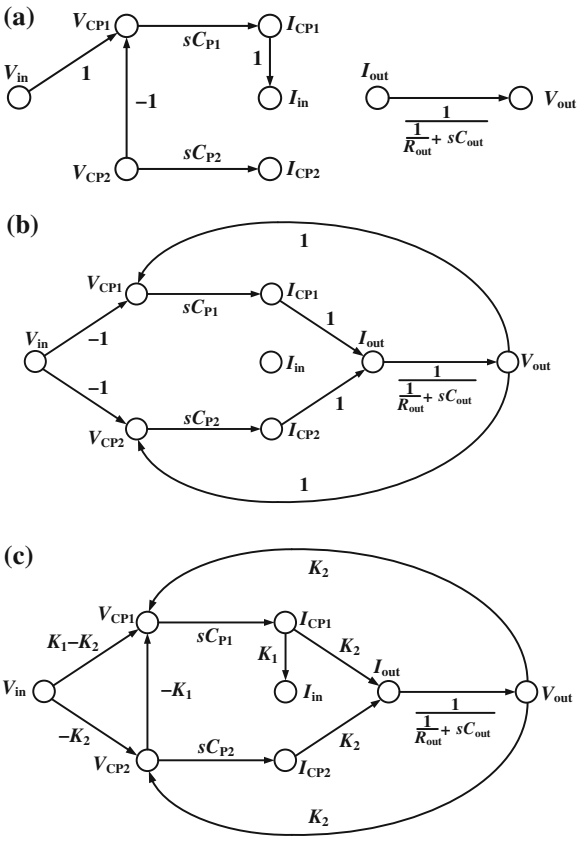


Fig. 5.11 SFGs for the (**a**) charge phase Φ_1 and (**b**) discharge phase Φ_2, and (**c**) the combined SFG by using phase multiplexing functions

$$\begin{cases} I_{CP1} = s \cdot C_{CP1} \cdot V_{CP1} \\ I_{CP2} = s \cdot C_{CP2} \cdot V_{CP2} \\ I_{out} = (1/R_{out} + s \cdot C_{out}) \cdot V_{out}. \end{cases} \tag{5.16}$$

Combining Eqs. (5.15) and (5.16), the complete signal flow graph for the charge phase SFG_{CH} can be derived as shown in Fig. 5.11a. Similarly, during phase $\Phi_2 = 1$, the KCL/KVL equations can be expressed as

$$\begin{cases} V_{out} = V_{CP1} + V_{in} \\ V_{out} = V_{CP2} + V_{in} \\ I_{out} = I_{CP1} + I_{CP2}. \end{cases} \tag{5.17}$$

The discharge phase SFG_{DCH} is obtained as in Fig. 5.11b. A closer look at the two SFGs reveals that certain branches appear in both graphs, while others only exist only in one. In order to merge SFG_{CH} and SFG_{DCH} into a combined SFG, two phase multiplexing functions are defined as

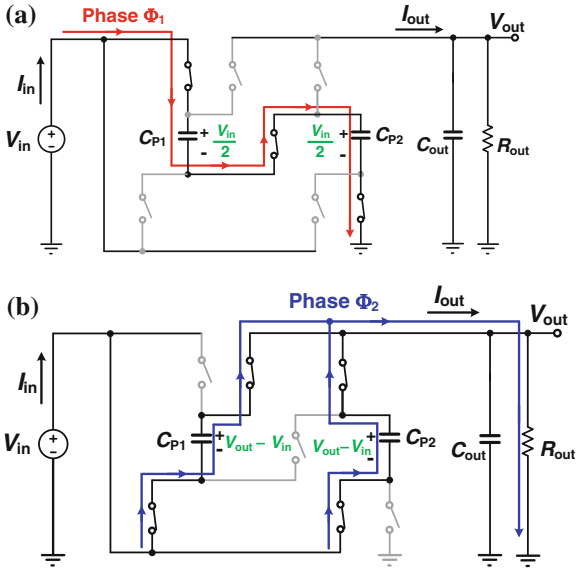


Fig. 5.12 Power stage configuration during (**a**) charge phase Φ_1 and (**b**) discharge phase Φ_2

$$K_1 = \begin{cases} 1 & \text{at phase } \Phi_1 \\ 0 & \text{not at phase } \Phi_1 \end{cases} \quad \text{and} \quad K_2 = \begin{cases} 1 & \text{at phase } \Phi_1 \\ 0 & \text{not at phase } \Phi_2 \end{cases} \tag{5.18}$$

The combined SFG_{COMB} can thus be mathematically written as

$$SFG_{\text{COMB}} = K_1 \cdot SFG_{\text{CH}} + K_2 \cdot SFG_{\text{DCH}} \tag{5.19}$$

Thus, Fig. 5.11c illustrates the combined SFG.

Based on the combined SFG shown in Fig. 5.11c, the corresponding SC power stage can be developed. As illustrated in Fig. 5.12a, during the charge phase Φ_1, the two pumping capacitors are charged up to V_{in}. Assume that C_{P1} and C_{P2} have the same capacitance, then, at the end of the charge phase the two capacitors will be charged to a voltage $V_{\text{in}}/2$. During the discharge phase Φ_2, two parallel paths are created as shown in Fig. 5.12b, which transfer the charges stored on C_{P1} and C_{P2} to the output V_{out}. At the end of phase Φ_2, the voltages across both the pumping capacitors will be $V_{\text{out}} - V_{\text{in}}$. When the converter reaches steady state, the difference between total charges on the two pumping capacitors should be equal to the charge delivered to the load. This is expressed as

$$(C_{\text{P1}} + C_{\text{P2}}) \cdot \left[\frac{V_{\text{in}}}{2} - (V_{\text{out}} - V_{\text{in}})\right] = \frac{V_{\text{out}}}{R_{\text{out}}} \cdot T_{\text{s}}, \tag{5.20}$$

where R_{out} is the equivalent load resistance and T_{s} is the switching cycle of the converter. Let $C_{\text{P1}} = C_{\text{P2}} = C_{\text{P}}$, then Eq. (5.20) is transformed to

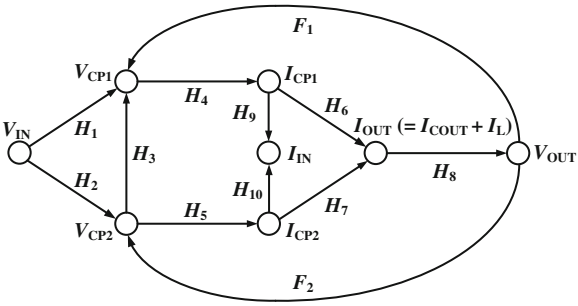


Fig. 5.13 SFG of the SC power converter with five CGs

$$V_{\text{out}} = \frac{3V_{\text{in}}}{2 + \frac{2T_s}{R_{\text{out}} \cdot C_P}}. \tag{5.21}$$

From Eq. (5.21), if $T_s/R_{\text{out}} \cdot C_P \ll 1$, then $V_{\text{out}} \approx 3/2\ V_{\text{in}}$. Hence, a SC power stage that achieves a CG of 3/2 is developed. Since the combined SFG merges any overlapping connections in SFG_{CH} and the SFG_{DCH}, all redundant switches are removed, leading to a minimum number of power switches. In addition, the SFG ensures that every connection between any two nodes is the shortest, with no unnecessary detours. Therefore, the power stage derived from this approach represents the most efficient powering path for each particular CG topology.

Following the same procedure, the SFGs and the corresponding power stages for CGs of 1/2, 2/3, 1 and 2 can be obtained. Combining these SFGs, the complete signal flow graph for the SC power converter can thus be derived, as illustrated in Fig. 5.13. The detailed branch transmittances $H_{1\sim10}$ and $F_{1,2}$ are summarized in Table 5.2. Accordingly, the reconfigurable power stage can be developed in Fig. 5.14. It includes 2 pumping capacitors C_{P1} and C_{P2}, and 11 power switches $S_{1\sim11}$. By taking different charge/discharge paths, 5 different CGs can be implemented. Comparing to the state-of-the-art designs, the developed structure can effectively achieve a wide voltage conversion range, with fewer power components. Note that no more than four power switches are turned on and off simultaneously at any switching instants. Thus, both conduction and switching power loss are significantly reduced.

5.2.2 Small-Signal Modeling and Analysis

The small-signal model for the developed SC converter shown in Fig. 5.14 can be derived from the SFG in Fig. 5.13. This is achieved by imposing small-signal perturbations onto the DC voltage and current at each node as given by

Table 5.2 Branch transmittances in the SFG

CG	1/2	2/3	1	3/2	2
$\mathbf{H}_1$	K_1	K_1	K_1	$K_1 - K_2$	$K_1 - K_2$
$\mathbf{H}_2$	K_1	K_1	K_1	$-K_2$	$K_1 - K_2$
$\mathbf{H}_3$	0	$-K_2$	0	$-K_1$	0
$\mathbf{H}_4$	sC_{P1}	sC_{P1}	sC_{P1}	sC_{P1}	sC_{P1}
$\mathbf{H}_5$	sC_{P2}	sC_{P2}	sC_{P2}	sC_{P2}	sC_{P2}
$\mathbf{H}_6$	1	1	K_2	K_2	K_2
$\mathbf{H}_7$	1	1	K_2	K_2	K_2
$\mathbf{H}_8$	$R_{out}/(1+sR_{out}C_{out})$	$R_{out}/(1+sR_{out}C_{out})$	$R_{out}/(1+sR_{out}C_{out})$	$R_{out}/(1+sR_{out}C_{out})$	$R_{out}/(1+sR_{out}C_{out})$
$\mathbf{H}_9$	K_1	K_1	K_1	K_1	K_1
$\mathbf{H}_{10}$	K_1	K_1	K_1	0	K_1
$\mathbf{F}_1$	$-K_1 + K_2$	$-K_1 + K_2$	K_2	K_2	K_2
$\mathbf{F}_2$	$-K_1 + K_2$	$-K_1$	K_2	K_2	K_2

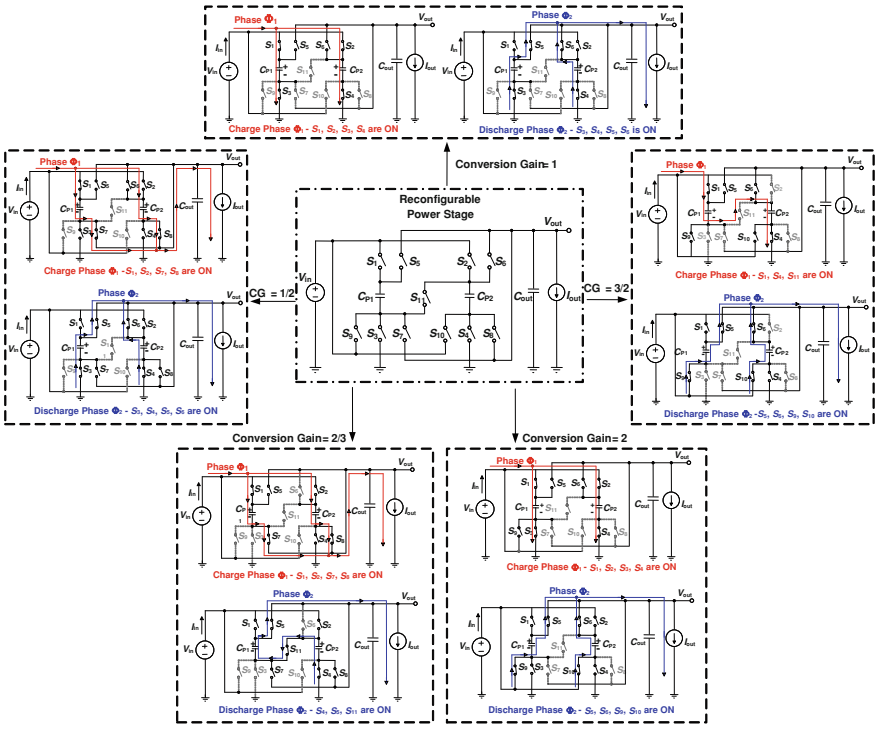


Fig. 5.14 Illustration of the step-up/down reconfigurable SC power converter with five CGs

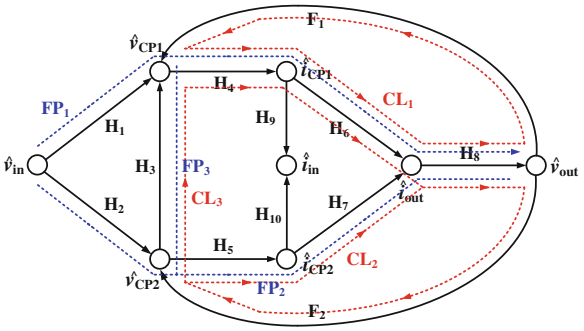


Fig. 5.15 Small-signal SFG

$$\begin{cases} V_{\text{in}}(t) = V_{\text{in}} + \hat{v}_{\text{in}}(t) \\ V_{\text{CP1}}(t) = V_{\text{CP1}} + \hat{v}_{\text{CP1}}(t) \\ V_{\text{CP2}}(t) = V_{\text{CP2}} + \hat{v}_{\text{CP2}}(t) \\ V_{\text{out}}(t) = V_{\text{out}} + \hat{v}_{\text{out}}(t) \end{cases} \text{and} \quad \begin{cases} I_{\text{in}}(t) = I_{\text{in}} + \hat{i}_{\text{IN}}(t) \\ I_{\text{CP1}}(t) = I_{\text{CP1}} + \hat{i}_{\text{CP1}}(t) \\ I_{\text{CP2}}(t) = I_{\text{CP2}} + \hat{i}_{\text{CP2}}(t) \\ I_{\text{out}}(t) = I_{\text{out}} + \hat{i}_{\text{out}}(t) \end{cases}. \tag{5.22}$$

By substituting Eq. (5.22) into each state node, the small-signal SFG can be derived as shown in Fig. 5.15, with the same branch transmittances tabulated in Table 5.2.

In order to demonstrate the application and effectiveness of the developed SFG, the transfer function and input/output impedance of the converter are derived. To find the gain between any two nodes in a given SFG, *Mason's Gain Formula* [4] is employed. This formula requires all the forward and closed loops between the two interested nodes to be identified, in order to calculate the transfer function between these two nodes. For the small-signal SFG shown in Fig. 5.15, three forward paths exist between $\hat{v}_{\text{in}}$ and $\hat{v}_{\text{out}}$ They are **FP$_1$**: $\hat{v}_{\text{in}} \rightarrow \hat{v}_{\text{CP1}} \rightarrow \hat{i}_{\text{CP1}} \rightarrow \hat{i}_{\text{out}}$, **FP$_2$**: $\hat{v}_{\text{in}} \rightarrow \hat{v}_{\text{CP2}} \rightarrow \hat{i}_{\text{CP2}} \rightarrow \hat{i}_{\text{out}} \rightarrow \hat{v}_{\text{out}}$ and **FP$_3$**: $\hat{v}_{\text{in}} \rightarrow \hat{v}_{\text{CP2}} \rightarrow \hat{v}_{\text{CP1}} \rightarrow \hat{i}_{\text{CP1}} \rightarrow \hat{i}_{\text{out}} \rightarrow \hat{v}_{\text{out}}$. Their path transmittances are $FP_1 = H_1 \cdot H_4 \cdot H_6 \cdot H_8, FP_2 = H_2 \cdot H_5 \cdot H_7 \cdot H_8$ and $FP_3 = H_2 \cdot H_3 \cdot H_4 \cdot H_6 \cdot H_8$, respectively. In addition, three closed loops are formed between $\hat{v}_{\text{in}}$ and $\hat{v}_{\text{out}}$. They are **CL$_1$**: $\hat{v}_{\text{CP1}} \rightarrow \hat{i}_{\text{CP1}} \rightarrow \hat{i}_{\text{out}} \rightarrow \hat{v}_{\text{out}} \rightarrow \hat{v}_{\text{CP1}}$, **CL$_2$**: $\hat{v}_{\text{CP2}} \rightarrow \hat{i}_{\text{CP2}} \rightarrow \hat{i}_{\text{out}} \rightarrow \hat{v}_{\text{out}} \rightarrow \hat{v}_{\text{CP2}}$ and **CL$_3$:** $\hat{v}_{\text{CP2}} \rightarrow \hat{v}_{\text{CP1}} \rightarrow \hat{i}_{\text{CP1}} \rightarrow \hat{i}_{\text{out}} \rightarrow \hat{v}_{\text{out}} \rightarrow \hat{v}_{\text{CP2}}$. Their path transmittances can be calculated as $\text{CL}_1 = H_4 H_6 H_8 F_1$, $\text{CL}_2 = H_5 H_7 H_8 F_2$ and $\text{CL}_3 = H_3 H_4 H_6 H_8 F_2$, respectively. In these three closed loops, no non-touching loop pairs exist. Thus, the determinant of the small-signal SFG can be obtained as

$$\Delta_{\text{USFG}} = 1 - \sum_{i=1}^{3} CL_{\text{i}}. \tag{5.23}$$

Applying Mason's Gain Formula, the input-to-output transfer function of the SC converter can be derived as

Table 5.3 SC power converter transfer function coefficients

CG	a_1	a_2	b_1	b_2
1/2	K_1	K_1	$K_1 - K_2$	$K_1 - K_2$
2/3	$K_1(1 - K_2)$	K_1	$K_1 - K_2 - K_1 K_2$	K_1
1	$K_1 K_2$	$K_1 K_2$	$-K_2^2$	$-K_2^2$
3/2	$K_2(K_1 - K_2 + K_1 K_2)$	$-K_2^2$	$-K_2^2(1 - K_1)$	$-K_2^2$
2	$K_2(K_1 - K_2)$	$K_2(K_1 - K_2)$	$-K_2^2$	$-K_2^2$

$$H(s) = \frac{\hat{v}_{\text{out}}}{\hat{v}_{\text{in}}} = \frac{\sum_{j=1}^{3} FP_{\text{j}} \cdot \Delta_{\text{j}}}{\Delta_{\text{USFG}}}, \tag{5.24}$$

where Δ_{j} equals one minus the sum of the closed loop transmittances, after removing the forward path j ($j = 1, 2, 3$). Since no closed loops exist after removing each of the three forward paths, we get $\Delta_1 = \Delta_2 = \Delta_3 = 1$. Substituting the values of each parameter into Eq. (5.24), the input-to-output transfer function can be rewritten as

$$\begin{aligned} H(s) &= \frac{\hat{v}_{out}}{\hat{v}_{in}} = \frac{H_8 \cdot [H_6 \cdot H_4 \cdot (H_1 + H_2 \cdot H_3) + H_2 \cdot H_5 \cdot H_7]}{1 - H_8 \cdot [H_6 \cdot H_4 \cdot (F_1 + H_3 \cdot F_2) + H_5 \cdot H_7 \cdot F_2]} \\ &= \frac{s \cdot R_{\text{out}} \cdot C_1}{1 + s \cdot R_{\text{out}} \cdot C_2}, \end{aligned} \tag{5.25}$$

where

$$C_1 = a_1 \cdot C_{\text{P1}} + a_2 \cdot C_{\text{P2}} \quad \text{and} \quad C_2 = C_{\text{out}} + b_1 \cdot C_{\text{P1}} + b_2 \cdot C_{\text{P2}}. \tag{5.26}$$

The coefficients $a_{1\sim2}$ and $b_{1\sim3}$ are tabulated in Table 5.3. From Eq. (5.25), one zero is observed at the origin, and one pole is located at $\omega_{\text{p1}} = 1/R_{\text{out}} \cdot C_2$.

By adopting a similar analysis approach, the open-loop input and output impedances can be obtained as

$$\begin{aligned} Z_{\text{in}}(s) &= \frac{\hat{v}_{\text{in}}}{\hat{i}_{\text{in}}} = \frac{1}{H_1 \cdot H_4 \cdot H_9 + H_2 \cdot (H_5 \cdot H_{10} + H_3 \cdot H_4 \cdot H_9)} \\ &= \frac{1}{(c_1 \cdot C_{\text{P1}} + c_2 \cdot C_{\text{P2}}) \cdot s}, \end{aligned} \tag{5.27}$$

and

$$\begin{aligned} Z_{\text{out}}(s) &= \frac{\hat{v}_{\text{out}}}{\hat{i}_{\text{out}}} = \frac{H_8}{1 - H_8 \cdot \begin{pmatrix} H_4 \cdot H_6 \cdot F_1 + H_5 \cdot H_7 \cdot F_2 \\ + H_3 \cdot H_4 \cdot H_6 \cdot F_2 \end{pmatrix}} \\ &= \frac{R_{\text{out}}}{1 + R_{\text{out}} \cdot (C_{\text{out}} + d_1 \cdot C_{\text{P1}} + d_2 \cdot C_{\text{P2}}) \cdot s}. \end{aligned} \tag{5.28}$$

Table 5.4 SC power converter transfer function coefficients

CG	c_1	c_2	d_1	d_2
1/2	K_1^2	K_1^2	$K_1 - K_2$	$K_1 - K_2$
2/3	$K_1^2\ (1 - K_2)$	K_1^2	$K_1 - K_2 - K_1\ K_2$	K_1
1	K_1^2	K_1^2	$-K_2^2$	$-K_2^2$
3/2	$K_2(K_1 - K_2 + K_1\ K_2)$	0	$-K_2^2(1 - K_1)$	$-K_2^2$
2	$K_1(K_1 - K_2)$	$K_1(K_1 - K_2)$	$-K_2^2$	$-K_2^2$

The coefficients $c_{1\sim2}$ and $d_{1\sim2}$ are summarized in Table 5.4.

In summary, this section presents a signal flow graph based modeling and analysis approach for reconfigurable charge pumps. Using this approach, it is possible to optimally design the power stage with minimal number of components. This reduces the complexity of the feedback controller, along with the power loss components.

5.3 Case Studies for Practical Applications

Following the general study on SC charge pump topologies and SFG modeling techniques, this section investigates several case studies in SC power converter design for specific applications. The case studies will specifically focus on emerging applications, such as TEG based energy harvesting and monolithic power converter design for system miniaturization. Each of the power converters discussed are designed by considering various application-specific requirements such as efficiency, load power, transient response, form factor, and so on.

5.3.1 Case Study 1: Reconfigurable SC Power Converter for Low-Voltage, Low-Power TEG Applications

As electronic devices capable of operating at microwatt power levels are being developed, it is now possible to use many non-traditional power sources. As discussed in Chap. 1, many state-of-the-art applications employ energy harvesting techniques to recharge, or even replace the primary battery. Of the plethora of devices where such power sources are being introduced, wireless sensor networks form a dominant application. The need to power them remotely, as well as the small area requirement and the intermittent use of power makes it ideal for using an energy harvesting power source. For wireless sensor networks, thermoelectric generators (TEG) are quite applicable, due its small form factor and energy availability.

Figure 5.16 shows the role of a power converter in a wireless sensor node where the power management circuit works in conjunction with the battery and

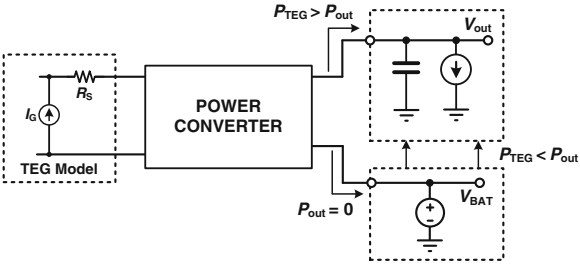


Fig. 5.16 Power management system with TEG as the power source

TEG. Based on the load demand, the power converter routes the power generated in the TEG to either the system load or an external battery. When there is no load demand, the power converter delivers the power to the battery, to store it. When there is a power demand from the external load, the converter checks to see if the output power from the TEG is sufficient to power the load. If the TEG is not capable of delivering sufficient power, the load draws power from the battery.

Designing a power converter for such a system is quite challenging. As discussed, due to the severe area constraint, switch mode power converters with bulky inductive components are not preferable. Moreover, wireless sensor nodes typically host transceiver circuits, which are very sensitive to EMI noise. Therefore, SC power converters are better suited for such applications. With respect to the power supply system design, the power and voltage levels generated by a TEG are usually very low and thus only require step-up voltage conversion. Additionally, due to the area constraint, it is preferable to use fully integrated capacitors. The system should also be capable of withstanding a wide input range due to the intermittent energy availability from the TEG, and a large load transient due to the sporadic operating characteristics of the load current. Lastly, since these systems operate at few mWs levels of power or lower, all sources of power loss need to be minimized, in order to obtain high efficiency and long runtimes.

Hence, this section first provides a comparison between several SC power converters, to identify the best power stage topology. The design strategy of the power stage is then discussed, with regards to ultra-low-power conversion. This involves the use of several system level and circuit techniques, such as charge recycling and adaptive body biasing.

5.3.1.1 Choice of Topology: SQSC or SPSC?

Traditionally, sequential switched-capacitor (SQSC) charge pump topologies have been the preferred power stage for the design of monolithic step-up SC power converters. In SQSC topologies, the pumping capacitors generate a step-up voltage in sequence. In the first stage, the capacitor is charged to V_{in}. The second capacitor is charged to $2V_{in}$ by the previous capacitor and the input voltage. The third capacitor is charged to $3V_{in}$ by the second capacitor and the input V_{in} and so on.

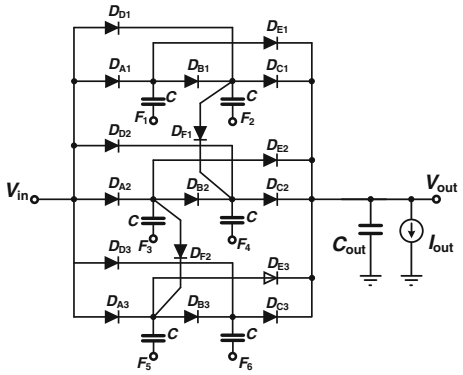


Fig. 5.17 SQSC power stage with multiple CG (2, 3 and 4) implementations

This sequence of voltage boosting continues until the output capacitor is ideally charged to a voltage level $(N + 1)\cdot V_{in}$, with N pumping capacitors. The main advantage of this implementation over the series parallel switched-capacitor (SPSC) topologies is that the bottom plate parasitic capacitor experiences a voltage swing of just V_{in}. For a SPSC converter, all the pumping capacitors are charged in parallel and discharged to V_{out} in series with the input voltage. Although this charge pump achieves an $(N + 1)\cdot V_{in}$ output voltage level with N pumping capacitors, during the discharge phase, the bottom plate parasitic capacitance of the first stage pumping capacitor is charged to V_{in}, the second to $2V_{in}$, the third to $3V_{in}$ and so on. At the final stage, the bottom plate capacitor experiences an $N\cdot V_{in}$ voltage swing. Therefore, the switching losses at these parasitic capacitors become significant. Due to this power loss mechanism, the SQSC converter has been the dominant topology.

One major drawback with the SQSC power stage topology is that it provides a step-up output voltage from a fixed input voltage source. However, the voltages that are produced by a TEG are not fixed. Moreover, the efficiency of a SC converter is highly affected by the voltage difference between V_{out} and $CG\cdot V_{in}$. Hence, the SC converter needs to be capable of providing multiple CGs, in order to be efficient. However, SQSC converters can provide only integer CG values. Providing multiple CGs with the same power stage can be very complicated. One example is shown in Fig. 5.17 where the SQSC power stage topology can provide the CG of 2, 3 and 4 [5]. For this topology, peak efficiency can be achieved at only three discrete output voltage levels for a given V_{in}.

On the other hand, it is relatively simple to provide multiple and fractional CGs with the SPSC topology. To illustrate this, a SPSC power stage topology is shown in Fig. 5.18. With half the capacitors than the SQSC topology, this power stage can provide five CGs (3/2, 2, 5/2, 3 and 4), leading to five peak efficiency points. As a result, the average efficiency of the converter over the entire input voltage range is higher than SQSC charge pumps, even after taking the bottom plate parasitic capacitors into account. In addition, with more capacitors, even higher number of CGs are possible, within the input voltage range. Therefore, in

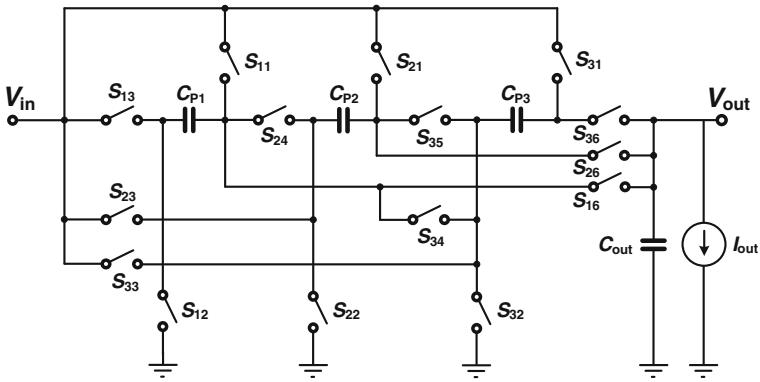


Fig. 5.18 SPSC power stage with multiple CG (3/2, 2, 5/2, 3, and 4) implementation

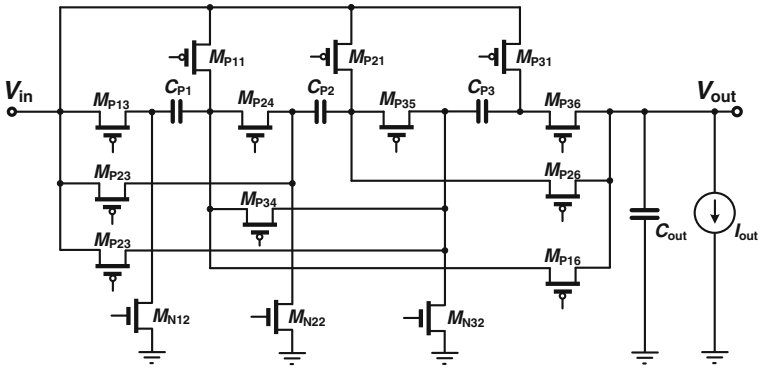


Fig. 5.19 Transistor level power stage implementation of the SPSC converter

self-powered applications that employ sources such as a TEG where the input voltage range is wide, it is more advantageous to use the SPSC topology since it operates at higher average efficiency.

The transistor level implementation of the power stage is shown in Fig. 5.19. It consists of three pumping capacitors and fifteen transistors. The top plate of each capacitor is connected to the input and the output terminals through power transistors M_{Pi1} and M_{Pi6} ($i = 1, 2, 3$), respectively. The bottom plate of each capacitor is connected to the ground or to the input terminal, through M_{Ni2} and M_{Pi3} ($i = 1, 2, 3$), respectively. M_{Pj4} ($j = 2, 3$) connects top plate of C_{P1} to the bottom plate of either C_{P2} or C_{P3} and finally M_{P35} connects top plate of C_{P2} to the bottom plate of C_{P3}. During the charge phase, the pumping capacitors are connected across the input voltage source with a configuration that charges them to either V_{in} or $V_{in}/2$ based on the CG. During the discharge phase, the capacitors are connected between V_{in} and V_{out}, with a configuration that also depends on the power stage CG.

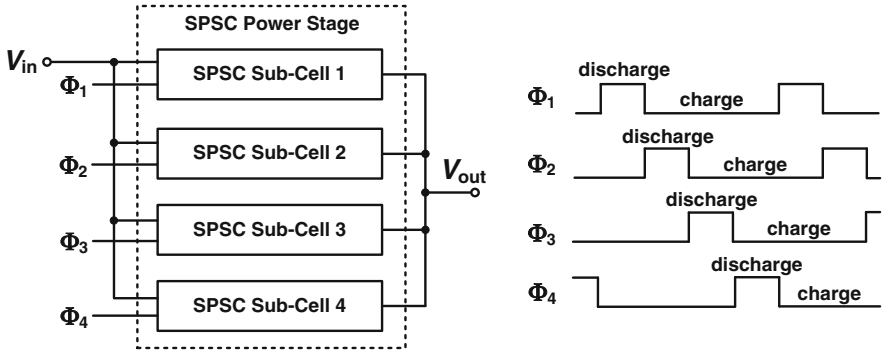


Fig. 5.20 Four cell interleaving SPSC power stage with 4-phase clock

Since the SPSC power converter is designed specifically for wireless sensor node applications, in order to minimize the system volume, all pumping capacitors have to be integrated on chip. Hence, the total capacitance in the power stage is limited by the available silicon area. Ideally, higher capacitance is preferred, as it enables the use of a lower switching frequency and thus reduced switching power loss. Therefore, to optimize the values of the capacitors, let the total available capacitance be C_{tot}, where

$$C_{tot} = C_{P1} + C_{P2} + C_{P3}. \tag{5.29}$$

To achieve a CG = 5/2, the capacitors C_{P2} and C_{P3} are connected in series during the charge phase. This causes each capacitor to be charged to $V_{in}/2$. This is possible when $C_{P2} = C_{P3}$. To achieve a CG = 3/2, the capacitors C_{P2} and C_{P3} are connected together and placed between V_{in} and C_{P1}, so that each capacitor is charged to $V_{in}/2$. To achieve this, $C_{P1} = C_{P2} + C_{P3}$. Solving for C_{P1}, C_{P2} and C_{P3} in terms of C_{tot} leads to, $C_{P1} = 1/2C_{tot}$, $C_{P2} = 1/4C_{tot}$, and $C_{P3} = 1/4C_{tot}$. The use of these capacitance values for the pumping capacitors allows the effective usage of the on-chip silicon area. In order to design the power switches, the similar methodology presented in Sect. 5.1 is employed.

The overall implementation of the power stage exploits the interleaving technique, as it is an effective means to reduce the overall switching noise in the system. The interleaving technique is employed in this reconfigurable SPSC power converter by dividing the power stage into four cells, and operating them with a four phase clock. Figure 5.20 illustrates the block diagram of the four-cell power stage, along with the associated timing diagram. From the figure, it can be observed that each cell of the power stage discharges to the output during one phase and charges from the input during the remaining three phases.

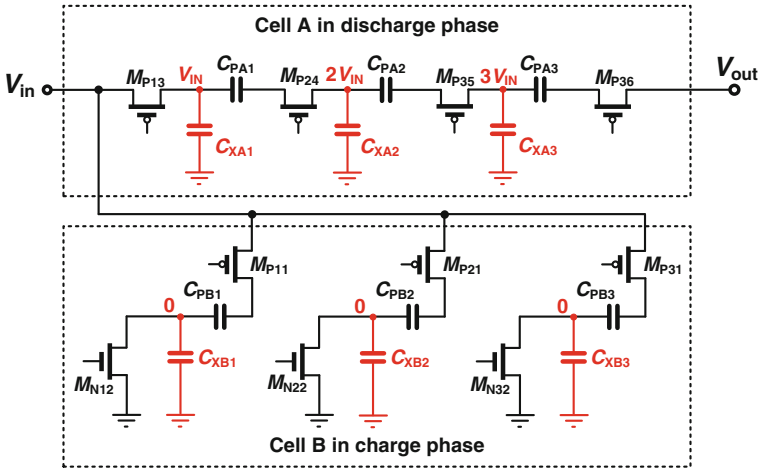


Fig. 5.21 Two cell SPSC power stage charge and discharge operation

5.3.1.2 Power Loss Minimization Techniques

The most significant source of power loss in monolithic SC power converters is the switching loss in the bottom plate parasitic capacitance. One technique to minimize this power loss is to employ a charge recycling technique. Charge recycling is applicable only to multi-cell power stage implementations. Since the SPSC power converter employs four cells in its power stage, this technique can be implemented easily. However, for simplicity, the operation is initially described considering a two-cell power stage.

Figure 5.21 shows the circuit configuration of a two cell SPSC power stage, during a single time frame. The converter provides a CG of 4, with all the parasitic capacitors in place. At this instant, consider the cell A to be discharging. As a result, the pumping capacitor C_{PA1}, C_{PA2} and C_{PA3} are connected in series with the input V_{in}. To provide a CG = 4, the bottom plate of the pumping capacitors are at voltages V_{in}, $2V_{in}$ and $3V_{in}$, respectively. On the other hand, cell B operates in the charge phase and the pumping capacitors C_{PB1}, C_{PB2} and C_{PB3} are placed in parallel with the input supply V_{in}. Their respective bottom plate capacitors are connected to ground and hence discharged. During the next transition phase, cell A operates in the charge phase and cell B operates in the discharge phase. As a result, the voltage across the parasitic capacitors would interchange. Hence, the bottom plate capacitors C_{XA1}, C_{XA2} and C_{XA3} would discharge to zero from V_{in}, $2V_{in}$ and $3V_{in}$, respectively. For cell B, the parasitic capacitors C_{XB1}, C_{XB2} and C_{XB3} have to be charged to V_{in}, $2V_{in}$ and $3V_{in}$. This additional charge would be supplied from the input V_{in}. As a result, charge would be lost from C_{PB1} and C_{PB2}, which would originally have been delivered to the output, leading to the degradation of the efficiency.

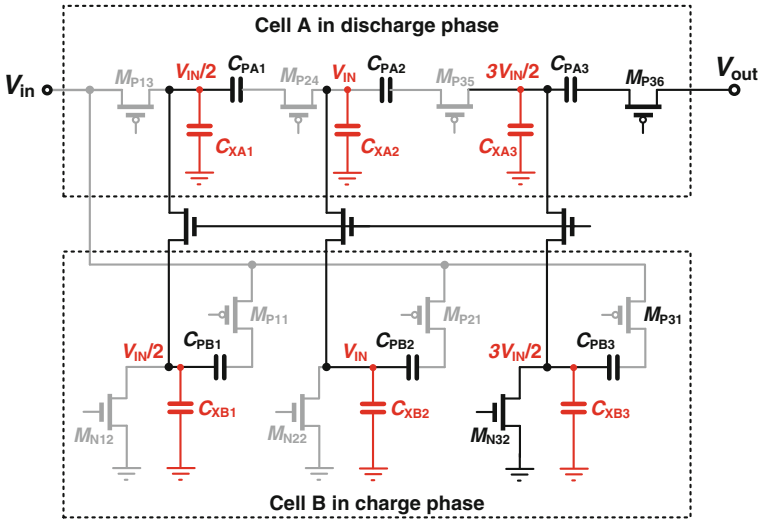


Fig. 5.22 Charge recycling during the transition phase

To overcome this drawback, Fig. 5.22 illustrates the operation of the charge recycling technique. This mechanism takes place during the transition time, where one cell changes from the discharge phase to charge phase and the other cell makes the opposite transition. In this technique, before the configuration of the pumping capacitors is altered, all the connections are broken by turning off all the power switches. At this instant, in cell A, the parasitic capacitors C_{XA1}, C_{XA2} and C_{XA3} are charged to V_{in}, $2V_{in}$ and $3V_{in}$, while in cell B, the parasitic capacitors C_{XB1}, C_{XB2} and C_{XB3} are all at zero potential. As observed in Fig. 5.22, during this transition period, C_{XA1} is connected to C_{XB1}, C_{XA2} is connected to C_{XB2}, and C_{XA3} is connected to C_{XB3}. As a result, charge is redistributed among the bottom plate capacitors. C_{XB1} is charged to $V_{in}/2$, C_{XB2} is charged to V_{in} and C_{XB3} is charged to $3V_{in}/2$. Therefore, when cell B enters the discharge phase, the input supply only needs to charge C_{XB1} from $V_{in}/2$ to V_{in} instead of from 0 to V_{in}. Similarly, C_{XB2} and C_{XB3} only need to be charged over half the voltage range of the original. With this technique, the charge that would have been lost when C_{XA1}, C_{XA2} and C_{XA3} are discharged to zero is re-utilized by the cell B parasitic capacitors. This conservation of charge between two interleaving cells significantly reduces the switching losses in the power stage, thereby improving the efficiency of the SPSC power converter.

With ultra-low output power, it is very important to maintain very low-power consumption for the controller. The controller of the SPSC converter includes a number of digital circuit blocks such as a 4-phase clock generator, clock signal router, etc. If these circuit blocks are operated directly from the input supply V_{in}, the power consumption due to the digital circuits increases exponentially with increasing V_{in}. At the highest input voltage level, the dynamic power consumption

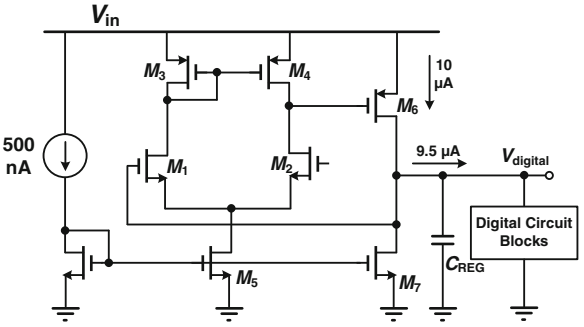


Fig. 5.23 Regulator circuit used for power digital circuit blocks

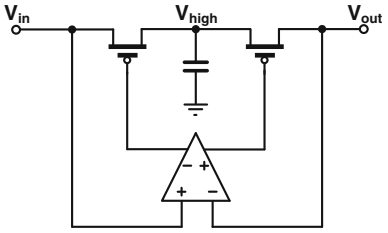


Fig. 5.24 Conventional gate drive circuit used in step-up SC power converters

due to the digital circuit becomes comparable to the switching loss. Therefore, to minimize the dynamic power consumption, a regulator is employed that controls the operating voltage of the digital circuits. The regulator allows the converter to save a significant amount of power by regulating the supply voltage of the digital circuits, with minimized voltage headroom. As illustrated in Fig. 5.23, the regulator is essentially a two-stage amplifier with very low-power consumption in the first stage. Since all the current that flows in the second stage powers the digital blocks, the additional power consumption due to regulator implementation is very low.

One of the critical challenges in the design of a step-up SC converter is driving the power transistors in the power stage, such that they operate as a switch with proper timing. For the correct operation of PMOS transistors, the gate voltage needs to be as high as any of its other terminals, to turn it off, and zero voltage at the gate-to turn it on. For controlling the NMOS transistors, the opposite is true.

In a conventional gate drive circuitry for a step-up SC converter, the drive circuitry is operated from the higher of V_{in} or V_{out} voltage [6]. Figure 5.24 shows the circuit that compares V_{in} and V_{out} and selects the higher voltage. This voltage is used to power the gate driver of the power transistors in the charge pump. However, this solution suffers from considerable reversion loss during the start-up process.

During start-up, the output voltage is still low. As such, the high voltage selection circuit selects V_{in} as the higher voltage. However, for CG = 4 during the discharge phase, the top plate capacitor nodes of C_{P1}, C_{P2} and C_{P3} are at potentials $2V_{in}$, $3V_{in}$ and $4V_{in}$, respectively. As a high voltage of V_{in} is applied to the gate terminals of the transistors M_{P11}, M_{P21} and M_{P31} in Fig. 5.25, these PMOS

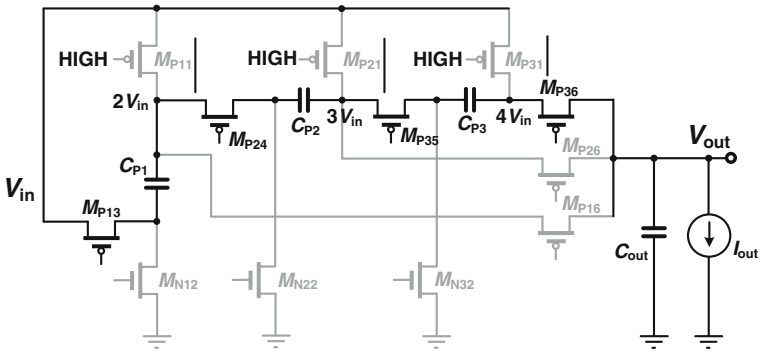


Fig. 5.25 Reversion loss at start-up with high voltage gate drive

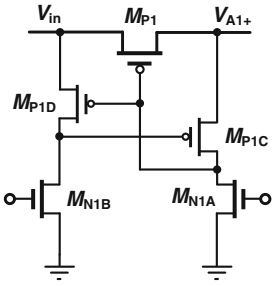


Fig. 5.26 Local gate drive circuit

transistors are not turned off properly. Therefore, these nodes have a direct path to V_{in}, causing severe reversion loss.

Figure 5.26 shows the local gate drive circuit used in the SPSC power converter designs, which is a modified version of a classic level shifter. It is controlled by differential gate signals applied at the NMOS transistor pair M_{N1A} and M_{N1B}. Its operation is illustrated in Fig. 5.27. Figure 5.27a depicts the state change of the power transistor M_{P1}, from the OFF state to the ON state. To achieve this, the potential at the gate terminal of M_{P1} should reach zero volt. At the same time, the gate voltage of M_{P1C} should go high, to prevent any shoot-through current. Hence, in order to control the power transistor, the gate control signal of M_{N1B} goes low, thereby turning it off, while the gate control signal of M_{N1A} goes high, turning it on. As a result, M_{N1A} pulls the gate voltage of M_{P1} and M_{P1D} to zero, turning on those transistors. As M_{P1D} is turned on, it generates a voltage V_{in} at the gate terminal of M_{P1C}. This action is reversed when M_{P1} transitions from on state to off state. Since this local gate drive circuit compares the internal node voltage of the power transistors to the input V_{in}, the highest voltage is always chosen, thereby preventing reversion loss even during the startup.

The circuit in Fig. 5.26 works well when the difference between the NMOS pair control signal voltage and the terminal voltage at the PMOS power transistor is moderate. If the difference becomes too large, the NMOS pair cannot discharge the

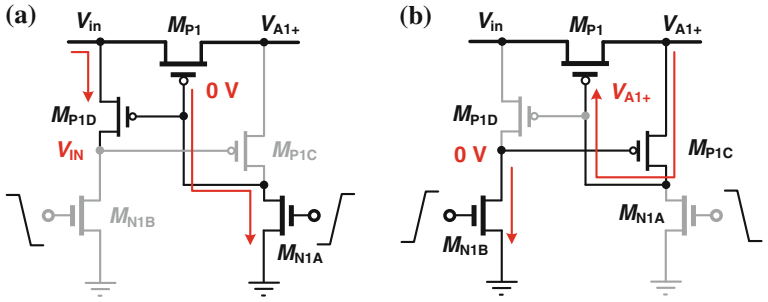


Fig. 5.27 Operation of the local gate drive circuit

Fig. 5.28 Gate drive circuit used for large voltage shifting

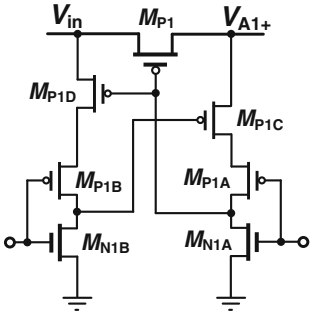
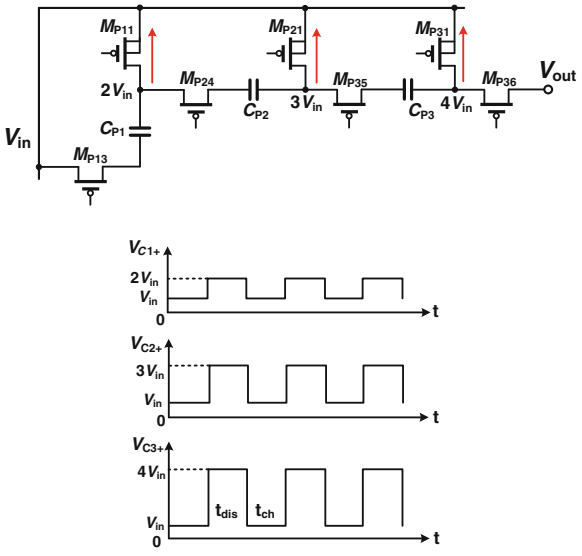


Fig. 5.29 Improper body biasing of the PMOS power transistors



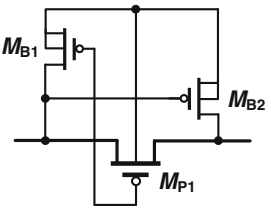


Fig. 5.30 Adaptive body biasing circuit

gate potential of the PMOS power transistor to zero quickly. This results in a large shoot-through current. To prevent this, an additional PMOS transistor is added to the shoot-through current paths as shown in Fig. 5.28. This transistor prevents a shoot-through current, even when a large voltage difference exists between the NMOS pair control signal and the voltage level at the gate terminal of the PMOS power transistor.

Due to large voltage swings at different nodes, the PMOS power transistors in the SPSC power converter experiences a large voltage change at their terminals. If the substrate of these transistors is connected to a voltage lower than any of its other terminal voltages, a reverse current can occur, as shown in Fig. 5.29. Moreover, always connecting the substrate of these devices to the highest voltage in the system is not a good solution as its leads to a large threshold voltage, when the transistor is turned on. Therefore, to obtain optimal performance, it is highly desirable to control the body bias of the power transistors in an adaptive manner.

Figure 5.30 shows the body bias circuitry which consists of only two transistors M_{B1} and M_{B2}. The operation of the circuitry is shown in Fig. 5.31. As shown in Fig. 5.31a, when the circuit is charging, the voltage at the gate terminal of M_{P1} is 0 V. This turns on M_{B1} and turns off M_{B2}. Therefore, parasitic capacitance at the body of M_{P1} is discharged to V_{in}, which cancels any threshold voltage modulation. During the discharge state shown in Fig. 5.31b, the gate and source terminals of M_{P1} are connected to a potential xV_{in}. This turns off M_{B1} and turns on M_{B2}, thereby charging the parasitic capacitance C_{par} to the voltage xV_{in}. Hence, any possible reverse current is prevented.

In conclusion, this section introduces a step-up SC power converter, designed specifically for TEG applications. It employs a series–parallel power stage, while utilizing multiple power loss minimization techniques such as charge recycling, local gate drive and adaptive body biasing.

5.3.2 *Case Study 2: Reconfigurable SC Power Converters for System Miniaturization*

System miniaturization and low-power operation is of critical importance for self-powered microsystems. Hence, this section presents the design of two low-power reconfigurable SC power converters. The first converter is a monolithic multiple-gain step-down SC power converter with on-chip pumping capacitor sizing.

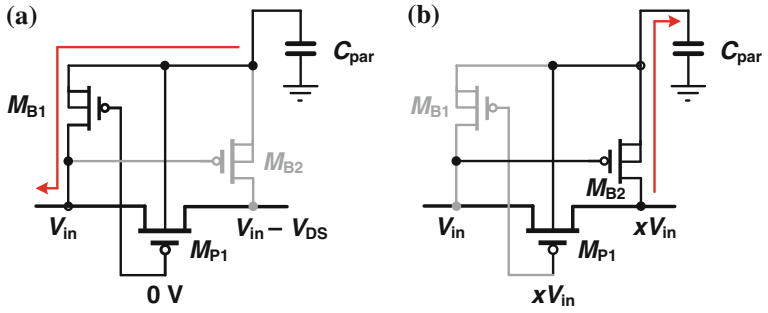


Fig. 5.31 Operation of adaptive body biasing technique during (**a**) charge phase and (**b**) discharge phase.discharge phase

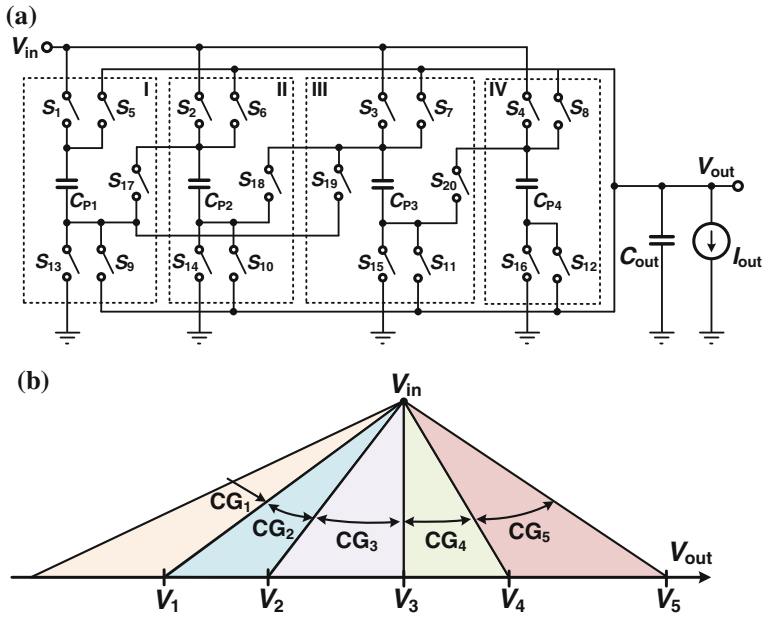


Fig. 5.32 (**a**) Reconfigurable step-down SC power stage and (**b**) V_{in} versus V_{out} relationship with adaptive gain control

The second converter further improves upon this design to provide both step-up and step-down voltage control.

The power stage of the multiple-gain, step-down, SC power converter is shown in Fig. 5.32a. It operates with a pair of complementary phases, Φ_1 and Φ_2. Instead of using large capacitors and switches in order to implement a single CG, 4 pumping capacitors C_{P1}, C_{P2}, C_{P3}, and C_{P4} and 20 switches are employed. This allows the converter to be reconfigured with 5 different CGs. For instance, as

Table 5.5 Switching schemes at different CGs

CG	V_{OUT}	Switches ON during Φ_1	Switches ON during Φ_2
3/5	$\leq V_1$	S_1, S_2, S_4, S_{10}, S_{11}, S_{12}, S_{19}	S_5, S_7, S_{14}, S_{16}, S_{17}, S_{20}
2/3	$V_1 \sim V_2$	S_1, S_2, S_7, S_9, S_{10}, S_{16}, S_{20}	S_3, S_4, S_5, S_{11}, S_{12}, S_{14}, S_{17}
3/4	$V_2 \sim V_3$	S_1, S_2, S_3, S_9, S_{10}, S_{11}	S_5, S_{15}, S_{17}, S_{18}
4/5	$V_3 \sim V_4$	$S_1 \sim S_4$, $S_9 \sim S_{12}$	S_5, S_{15}, S_{16}, S_{17}, S_{18}, S_{20}
1	$V_4 \sim V_5$	S_1, S_2, S_7, S_8, $S_{13} \sim S_{16}$	$S_3 \sim S_6$, $S_{13} \sim S_{16}$

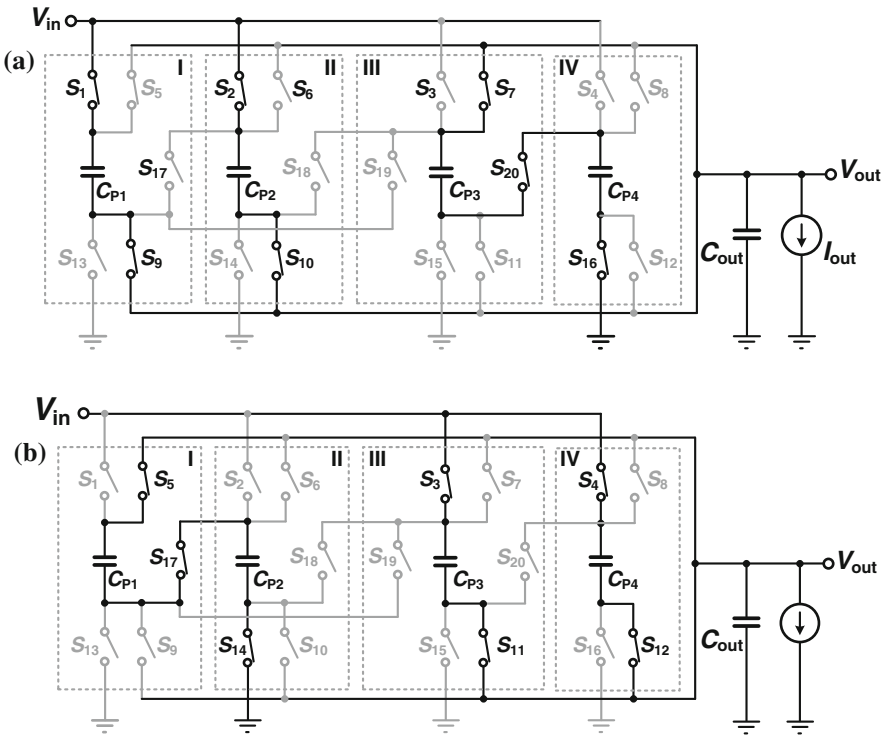


Fig. 5.33 SC power converter with a CG of 2/3, operating in phase (**a**) Φ_1 and (**b**) Φ_2

depicted in Fig. 5.32b, with a fixed input V_{in}, if V_{out} needs to be changed from V_5 to V_3, instead of modulating the duty ratio, which degrades the efficiency of the converter, the power stage is automatically reconfigured with a CG change from CG_5 to CG_3.

The step-down SC power converter in Fig. 5.32a can provide five different CGs, 3/5, 2/3, 3/4, 4/5 and 1. The entire output range can thus be divided into five different regions, from V_1 to V_5. For each region, appropriate switching actions lead to the regulation of the output voltage. Table 5.5 illustrates the switching schemes at the different CGs for the SC power converter.

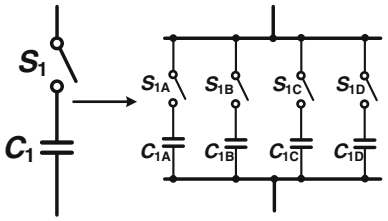


Fig. 5.34 Adjustable size capacitor implementation

Figure 5.33 illustrates the operation of the multiple CG SC power converter operating in the CG = 2/3 configuration. During the phase Φ_1, the power switches S_1, S_2, S_7, S_9, S_{10}, S_{16}, and S_{20} are turned on. This creates two charge paths for the pumping capacitors C_{P1} and C_{P2}, while charges accumulated in C_{P3} and C_{P4} are delivered to V_{out}. During the phase Φ_2, the switches S_3, S_4, S_5, S_{11}, S_{12}, S_{14}, S_{17} are turned on, as shown Fig. 5.33b. Accordingly, C_{P3} and C_{P4} are charged up, while C_{P1} and C_{P2} deliver power to V_{out}. If all the pumping capacitors have their capacitance equal to C_P, the voltage across the capacitors C_{P1} and C_{P2} (C_{P3} and C_{P4}) will be equal to $V_{in} - V_{out}$ ($V_{out}/2$) at the end of phase Φ_1, and be equal to $V_{out}/2$ ($V_{in} - V_{out}$) at the end of phase Φ_2, respectively. When the SC power converter reaches the steady state, the total net charge difference on the pumping capacitors should be equal to the charge consumed by the output load. Using a similar analysis as that employed in Eqs. (5.20) and (5.21), it can be shown that if $\frac{T_s}{2R_{out}C_P} << 3$ then, $V_{out} \approx 2V_{in}/3$. Thus, a step-down voltage conversion of 2/3 is achieved. As illustrated in Fig. 5.32b, based on the reference voltage, an optimal power converter topology can be chosen. Since the conversion gain is modulated instead of the duty ratio, the efficiency of the overall SC converter is improved.

The expression for V_{out} of the reconfigurable SC power converter is given by

$$V_{out} = \frac{2V_{in}}{3 + \frac{T_s}{2R_{out}C_P}}. \tag{5.30}$$

Equation (5.30) reveals that the output voltage of the SC power converter can be regulated to different levels if the pumping capacitor C_P or the switching frequency $1/T_S$ are adjustable. A higher switching frequency leads to an increase in the switching power loss and generates higher switching noise. On the other hand, adjusting the size of the pumping capacitor to regulate V_{out} leads to higher efficiency, when compared to modulating the duty ratio. Therefore, in order to further improve the efficiency when the voltage level change on V_{out} is relatively smaller, an on-chip capacitor sizing technique is proposed.

An adjustable size capacitor can be implemented with a series of smaller size unit capacitors and switches, as illustrated in Fig. 5.34. The final capacitance of the combination is determined by the status of the switches and connections between the unit capacitors. For example, if all the switches in Fig. 5.34 are turned on, an equivalent capacitance of $C_{1A} + C_{1B} + C_{1C} + C_{1D}$ is achieved. To decrease the capacitance, the switch S_{1D} can be turned off, leading to a total

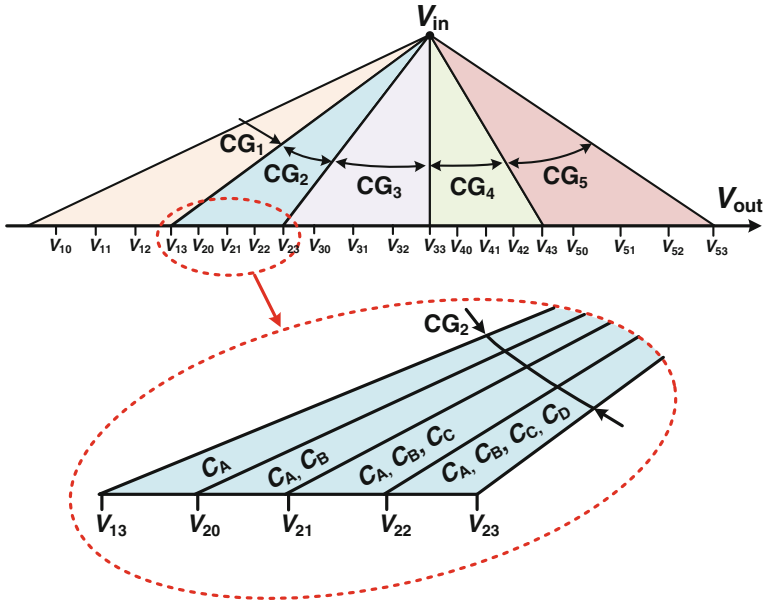


Fig. 5.35 On-chip capacitor sizing scheme for adaptive gain control in the SC power converter

capacitance of $C_{1A} + C_{1B} + C_{1C}$. The size of the sub-capacitors and sub-power switches are determined by their individual power flow, while the total capacitor size and power switch width remains constant. Thus

$$\begin{cases} C_{1A} + C_{1B} + C_{1C} + C_{1D} = C_1, \\ W_{1A} + W_{1B} + W_{1C} + W_{1D} = W_1, \end{cases} \tag{5.31}$$

where W_{1i} is the width of the power transistor S_{1i}, $i = a, b, c, d$ and W_1 is the width of the power transistor S_1. Correspondingly, employing adjustable size pumping capacitors decreases the capacitor redistribution loss, while using sub-power switches further lowers the switching power loss.

According to Table 5.5 and Fig. 5.32b, with 5 CGs, the biggest voltage gap $\Delta V = V_i - V_{i\_1}$, $i = 2, 3, 4, 5$ between adjacent regulation voltages V_i and V_{i_1} is 200 mV, if the converter is designed with a 1.8 V input voltage and a 50 % duty ratio. In this case, four reconfigurable on-chip capacitors are implemented to decrease ΔV to be less than 50 mV. This is illustrated in Fig. 5.35. Thus, the regulation error can be controlled below 25 mV. Hence, the on-chip capacitor sizing scheme fine tunes the regulation errors and helps to retain high efficiency.

From the perspective of circuit implementation, the SC cells I, II, III and IV in Fig. 5.32a are each implemented with 4 sub-cells. For example, Cell I consists of sub-cells I-a, I-b, I-c and I-d, as shown in Fig. 5.36a. These sub-cells share a common topology but employ different sizes of switches and capacitors, tailored

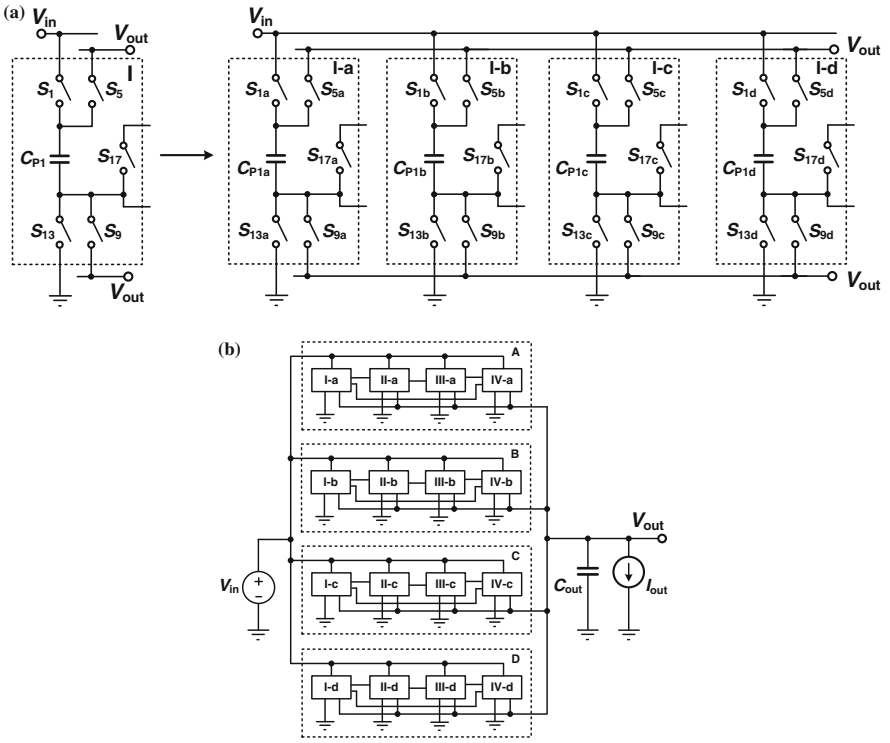


Fig. 5.36 (**a**) Capacitor sizing in one single cell and (**b**) grouping of the step-down SC power stage

for different regulation voltage levels. Eventually, based on the common charge and discharge switching behaviors, they are reorganized to groups A, B, C, D, as depicted in Fig. 5.36b.

To illustrate the design idea, consider the case when CG_2 is 2/3. With reference to Fig. 5.35 and Eq. (5.30), in order to allow the converter to regulate at the highest voltage in this region–V_{23}, all the 16 sub-cells from I-a to IV-d function actively. As a result, the largest on-chip capacitance is generated as the sum of each unit capacitors. If V_{out} needs to drop to the next voltage level V_{22}, all the sub-cells except those in the group D will stay active. Accordingly, the equivalent capacitance would be equal to the sum of total unit capacitance in the groups A, B and C. Similarly, if only one group A remains active with for a CG of 2/3, as shown in Fig. 5.35, the lowest output voltage in the region V_{20} would be achieved.

Such a grouping method ensures the most efficient chip area and layout routing. The first advantage of this structure is that each group is independent. No interconnections exist between two groups, except for the connection to V_{in}, V_{out} and ground. Thus, if one group in Fig. 5.36b fails, due to circuit malfunction or device failure, the other groups continue to operate in the power stage. Therefore, system

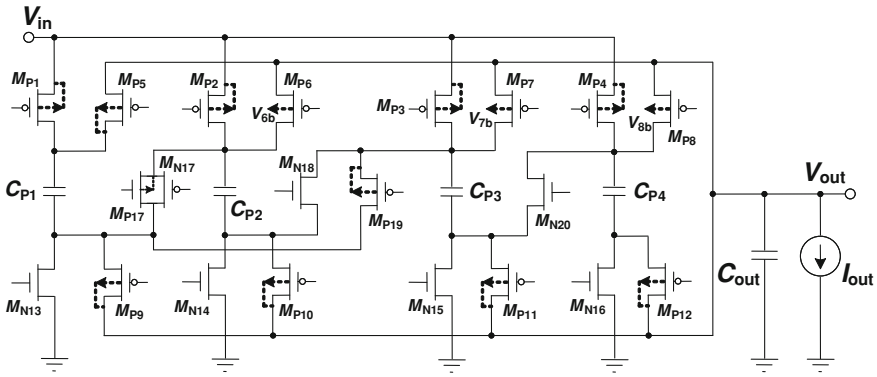


Fig. 5.37 Circuit implementation of group A in the reconfigurable power stage

robustness is significantly improved. The second advantage with this structure is the resulting reduction in power loss. Once a certain group of sub-cells are disabled in order to generate a lower output voltage, all the control signals for that group are either high or low to turn off the power transistors. As a result, the switching and conduction losses of that group are completely eliminated. Moreover, no switching loss is consumed in their corresponding buffer drive circuitry. The third advantage with the four-cell power stage is that an interleaving technique can be effectively applied. This can significantly reduce the output voltage ripple in the power supply.

Figure 5.37 illustrates the circuit implementation of group A in the power stage of the SC power converter. Switches $S_{13} \sim S_{16}$ that are connected to ground are implemented by NMOS transistors, and the switches $S_1 \sim S_4$ which are connected to V_{in} are implemented by PMOS transistors. In this SC converter, since V_{out} changes from V_{in} to $3/5V_{in}$, the power switches $S_5 \sim S_{12}$ which are connected to the output load are implemented through PMOS transistors. The substrate terminals of these transistors should be connected to its highest voltage, to avoid any leakage currents. In this scenario, the highest voltage is V_{in}. However, if the substrate is always directly connected to V_{in}, then the body effect of the PMOS transistor will increase its threshold voltage. Hence, in this design the substrate terminal of the PMOS transistors M_6, M_7 and M_8 are connected to the higher node between their corresponding drain and source terminals. The schematic diagram used to implement this function is similar to the circuit illustrated in Fig. 5.30. Moreover, from Fig. 5.37, it can be observed that the switch S_{17} is implemented as a transmission gate. This is because for a CG of 2/3, its V_{GS} voltage is $1/3V_{in}$ (≈ 0.6), while for a CG of 4/5 the V_{GS} voltage is $3/5V_{in}$. Thus, a transmission gate ensures that the switch is fully turned on or off in each scenario.

The optimization of the power stage is paramount, since it directly affects the efficiency of the entire system. For a SC power converter, the power loss from the power stage, consisting of the switching and conduction losses, dominates the

overall power loss of the converter. The conduction loss P_C of the step-down SC converter can be represented as

$$P_C = \sum_i D_{Si} R_{Si} \left(\frac{a_{Si}}{D_{Si}} I_{OUT} \right)^2, \tag{5.32}$$

where D_{si} and R_{si} represent the duty cycle and the turn-on resistance of the power transistor i, and a_{Si} is the switch charge multiplier vector. For a CG of 2/3, $a_{s1} = a_{s2} = a_{s3} = a_{s4} = a_{s5} = a_{s6} = a_{s7} = 1/3$. Note that R_{si} can be controlled by sizing the individual transistor i, since

$$R_{Si} \approx \frac{L}{\mu C_{ox} W_i (V_{GS} - V_{TH})}. \tag{5.33}$$

In this implementation, all the PMOS and NMOS power transistors are designed to have the same size, for system simplicity and symmetry. To ensure that the power loss is minimized, the ratio of the PMOS to NMOS size, k, where $k = W_P/W_N$ is optimized. To minimize the on-chip silicon area and parasitic capacitance, each transistor employs the minimum length of the semiconductor process. Lastly, if the conduction loss due to ESR of the pumping capacitors is also considered, the total conduction loss of charge pump is modified as

$$P_C = \sum_i D_{Si} R_{Si} \left(\frac{a_{Si}}{D_{Si}} I_{out} \right)^2 + ESR \cdot I_{out}^2. \tag{5.34}$$

The switching power loss P_{sw} of the power transistors is given and simplified as

$$P_{sw} = f_s \sum_i C_{GSi} V_{GSi}^2 = f_s C_{ox} \sum_i W_i \cdot V_{GSi}^2, \tag{5.35}$$

where C_{GSi} is the gate-to-source capacitance, W_i is width of power transistor i, and V_{GSi} is the voltage swing. Meanwhile, for a single transistor working in the linear region and cut off region, the drain-to-bulk voltage swing V_{DB} (drain-bulk capacitance C_{DB}) and source-to-bulk voltage swing V_{SB} (source-to-bulk capacitance C_{SB}) is much smaller than V_{GS} (C_{GS}). Thus, the power loss due to the parasitic capacitors C_{DB} and C_{SB} is much smaller than the power loss due to C_{GS}. As a result, Eq. (5.35) is approximated to be the total switching loss of the SC power converter.

In this SC step-down power converter, if non-overlapping clock signals are used to control the power stage, the reversion power loss can be minimized. Hence, the total power loss is approximately determined by the conduction and switching loss as

$$P_{tot} = P_c + P_{sw}. \tag{5.36}$$

In order to maximize the power efficiency, the optimized power transistor width W_N and the ratio k should satisfy the following requirements $\partial P_{tot}/\partial W_N = 0$ and

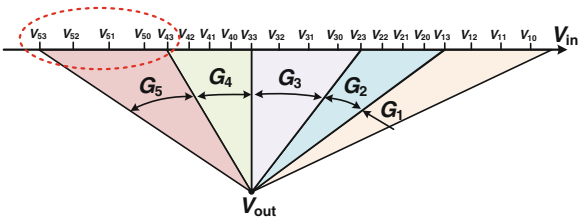


Fig. 5.38 Design extension for variable-input constant-output SC power converters

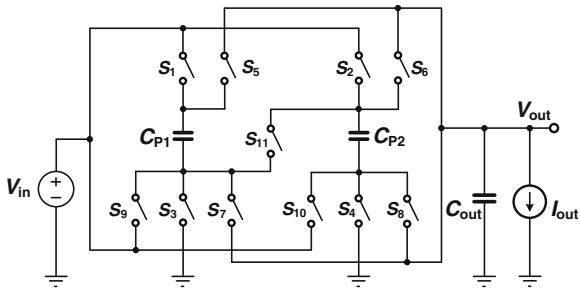


Fig. 5.39 The reconfigurable step-up and step-down SC power stage

$\partial P_{tot}/\partial k = 0$. For different CG topologies, the condition will generate different optimized power transistor widths W_N and ratios k. Based on these optimized parameters, the final power transistor size and k ratio to design the SC power converter for the maximized efficiency can be obtained.

The on-chip capacitor sizing techniques analyzed in this section for the step-down SC power converter can also be applied to variable-input and constant-output converters. This is extremely attractive for applications that employ unstable energy harvesting power sources. The approach is illustrated in Fig. 5.38. The only difference under this operation scenario is that the highest (lowest) gain and largest (smallest) pumping capacitors size are applied to the lowest (highest) input voltage to obtain a constant output voltage. For example, the lowest input V_{53} operates with the help of all the sub-cells and the highest gain CG_5. A slightly higher input voltage V_{52}, still employs the same power stage topology and CG, but all the sub-cells in group D will be deactivated, in order to reduce the effective on-chip capacitance.

5.3.2.1 A Reconfigurable Step-Up and Step-Down SC Power Converter

In certain applications, self-powered microsystems need both step-up and step-down conversion in the power stage, since battery voltages can decline over its operating lifetime, as the power is drained. Under these scenarios, the SC power converter discussed earlier is not sufficient. Hence, this section presents a reconfigurable SC power converter that can provide both step-up and step-down voltage conversions. Similar to the previous implementation, this converter also operates with a pair of complementary phases, Φ_1 and Φ_2. The power stage employs 2

Table 5.6 Switching schemes for the step-up and step-down reconfigurable SC power converter

CG	V_{out}	Switches ON during Φ_1	Switches ON during Φ_2
1/2	$\leq V_1$	S_1, S_2, S_7, S_8	$S_3 \sim S_6$
2/3	$V_1 \sim V_2$	S_1, S_2, S_7, S_8	S_4, S_5, S_{11}
1	$V_2 \sim V_3$	$S_1 \sim S_4$	$S_3 \sim S_6$
3/2	$V_3 \sim V_4$	S_1, S_4, S_{11}	S_5, S_6, S_9, S_{10}
2	$V_4 \sim V_5$	$S_1 \sim S_4$	S_5, S_6, S_9, S_{10}

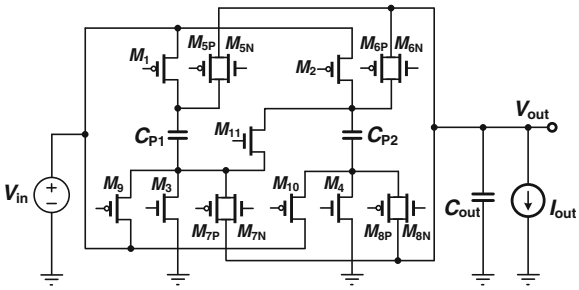


Fig. 5.40 Circuit implementation of the step-up/down reconfigurable SC power converter

pumping capacitors C_{P1} and C_{P2}, and 11 switches, as shown in Fig. 5.39. This allows the converter to be reconfigured with 5 different CGs, 1/2, 2/3, 1, 3/2, 2. Table 5.6 elaborates the switching schemes for the different configurations of the SC power converter.

The operation of the step-up/down SC power converter can be explained with the aid of Fig. 5.39, for a CG of 3/2. During the phase Φ_1, the power switches S_1, S_4, and S_{11} are turned on. This creates a charge path to pre-charge the pumping capacitors C_{P1} and C_{P2}. During the phase Φ_2, the switches S_5, S_6, S_9, S_{10} are turned on. Accordingly, this creates two discharge paths to discharge power from C_{P1} and C_{P2} to V_{out}. Note that if $C_{P1} = C_{P2}$, the voltage across the pumping capacitors will be equal to $V_{in}/2$ at the end of phase Φ_1 and $V_{out} - V_{in}$ at the end of Φ_2, respectively. When the SC power converter reaches steady state, the total net charge difference on the pumping capacitors C_{P1} and C_{P2} should be equal to the charge consumed by the load resistor R_{out}. As a result, using the steady state analysis used for the previous SC converters, the expression for V_{out} can be shown to be given by

$$V_{out} = \frac{3V_{in}}{2 + \frac{2T_s}{R_{out}C_P}}. \tag{5.37}$$

If $T_s/R_{out} \cdot C_P \ll 1$, then $V_{out} \approx 3/2 \cdot V_{in}$. Thus, a step-up voltage conversion of 3/2 is achieved.

The circuit implementation of the converter is illustrated in Fig. 5.40. Similar to the SC power converter discussed in Sect. 5.3.1, the power transistors sizes in this converter are optimized according to the power transferred in the charge and discharge phases.

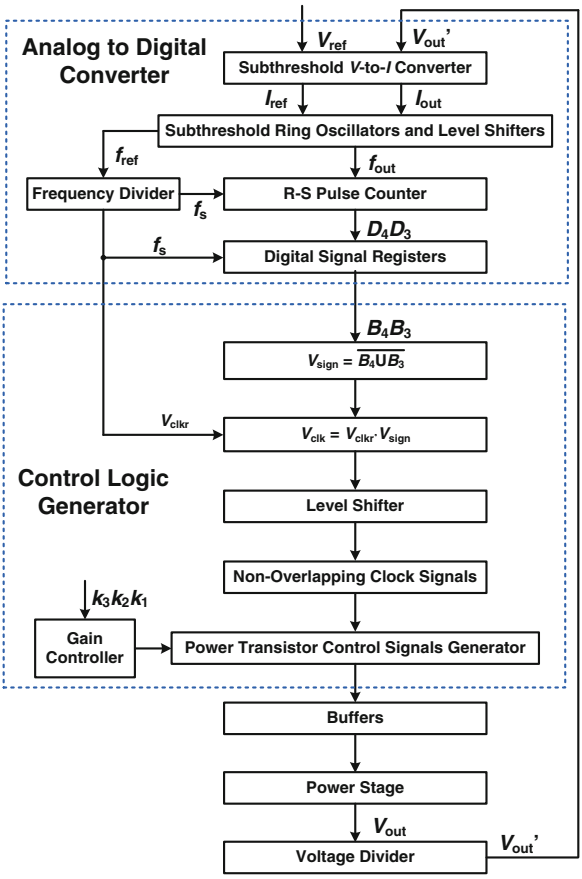


Fig. 5.41 Flowchart of the closed loop controller for the step-up/down SC power converter

Figure 5.41 shows the flow chart for the closed loop operation of the feedback controller. The controller fulfills two major functions: analog to digital conversion and generates the necessary control logic signals. The analog to digital converter senses the voltage regulation error and converts it to digital error signals. A differential V-to-I converter is employed to detect and amplify the error between V_{out}' (scaled from V_{out}) and the reference voltage V_{ref}. To achieve this, these two voltages are initially converted into corresponding currents values. A differential circuit topology provides the error information ΔI, while effectively canceling out even-order harmonics and temperature/process variations. Following the V-to-I conversion, two subthreshold ring oscillators further convert ΔI into a frequency difference Δf. Here, these two currents are used to to bias the two ring oscillators. With different biasing currents, the oscillation frequency of each oscillator varies accordingly. Following the flowchart in Fig. 5.41, the converted frequency information Δf is continuously turned into the digital binary signals by the frequency dividers, R-S pulse counters and digital signal registers. The frequency

dividers are composed of digital latches. To compare the frequencies in two subthreshold ring oscillators, R-S pulse counters are used to count the pulses generated by the subthreshold ring oscillator that is controlled by V_{out}', in one switching clock cycle.

In the control logic generator, the gain controller determines the power stage conversion CG, with 3-bit control signals. This is then combined with signal V_{sign}, which is generated from the analog to digital converter, in order to obtain the operation status for all the power transistors. For example, when $k_3k_2k_1 = 011$, the topology corresponding to the CG of 2/3 is chosen.

In conclusion, this section discusses two reconfigurable SC power converters for self-powered microsystems. The multiple-gain control helps these two converters to constantly maintain high efficiency over a wide operating range. The adjustable size pumping capacitors allow the output voltage to be regulated at different desired levels, with minimized power loss. The fully on-chip implementation significantly reduces system volume and switching noise. Hence, these state-of-the-art designs provide an effective solution for next generation monolithic power supply designs for self-powered portable devices.

5.4 Conclusions

This chapter presents various state-of-the-art reconfigurable SC power converters, designed specifically for self-powered microsystems. Based on the instantaneous operating conditions, these modern SC converters are capable of dynamic reconfiguration into the optimal power stage, thereby providing the desired CG that minimizes power losses and provides enhanced power regulation.

The chapter initially presented the general topologies and control schemes that are employed to achieve dynamic reconfiguration in SC power converters, in Sect. 5.1. To control the reconfigurable charge pump, an interleaving regulation scheme with multi-phase CG reconfiguration was discussed. This technique can be effectively employed to reduce output voltage ripple and improve the bandwidth for self-powered applications.

Following the discussion on generic reconfigurable charge pump topologies and control schemes, Sect. 5.2 presented a signal flow graph based modeling and analysis approach. Using this approach, it is possible to optimally design the power stage of a reconfigurable charge pump. Typically, the use of a highly reconfigurable power stage significantly increases the number of power components along with the complexity of the controller. This introduces considerable challenges during the optimization of SC power converters. The SFG technique leads to a reconfiguration algorithm that can be optimized to achieve multiple CGs, with highly-efficient energy delivery and minimized number of power components.

Section 5.3 discussed two case studies regarding reconfigurable SC power converter design for specific applications. The first case study presented the design of a reconfigurable step-up SC power converter, designed specifically for TEG

based energy harvesting applications. The design on this converter entailed an investigation upon an appropriate power stage topology. Based on the requirements, a series–parallel power stage was employed. In order to minimize power losses several low-power circuit techniques such as charge recycling, local gate drive and adaptive body biasing were employed. Next, the second case study that was discussed was the design of two low-power reconfigurable SC power converters for system miniaturization. The first converter discussed was a monolithic reconfigurable multiple-gain step-down SC power converter with on-chip pumping capacitor sizing. In this power supply design, a different approach is followed towards closed loop regulation. Instead of varying the duty ratio to obtain different output voltage levels, the power stage undergoes dynamic reconfiguration in terms of the topology and effective on-chip pumping capacitance. This leads to reduced power loss in the converter. The second converter employs this design principle, but provides both step-up and step-down voltage conversion.

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Chapter 6
Configuring Switched-Capacitor Power Converters Using Interleaving Regulation Techniques

6.1 Fundamental Principles

Due to their inherent switching operations, both switch mode and SC power converters exhibit output voltage ripples and current ripples, which lead to substantial switching noise. The switching actions in many power converters can cause their input current to be discontinuous. This can generate severe *di*/*dt* noise, which will propagate into the entire system. In the meanwhile, a discontinuous output current can severely impact the load regulation performance of SC converters. Such converters will respond to sudden load changes only at the start of the next switching cycle, which can cause large output voltage variations. Moreover, since a discontinuous output current energizes the output capacitor only during the discharge phase, the output voltage ripple is also considerably higher. As a consequence of these issues, the reliability and performance of load applications is severely impacted.

To illustrate the aforementioned issues, a voltage inverter is used as an example in Fig. 6.1. It is controlled by a pair of complementary clock signals, Φ_1 and Φ_2. Due to the presence of the load current, the output capacitor is periodically discharged, until it is recharged by the charge pump. From Fig. 6.1b, it can be observed that certain challenges exist in this design. Since the pumping capacitor C_P is disconnected from V_{in} during its discharge phase, the input current I_{in} is discontinuous. This generates large *di*/*dt* noise, which is coupled into V_{out}. Moreover, if the power converter experiences a sudden load transient during the phase $\Phi_1 = 1$, then charge pump is unable to respond until the start of the discharge phase $\Phi_2 = 1$. The output capacitor C_{out} has to provide the necessary charge to the load until the charge pump can respond, which causes a significant drop in V_{out}. Thus, the load regulation and transient response of the power converter is degraded. Furthermore, since the output current is discontinuous, the output voltage ripple is also significantly larger, which is highly undesirable. One

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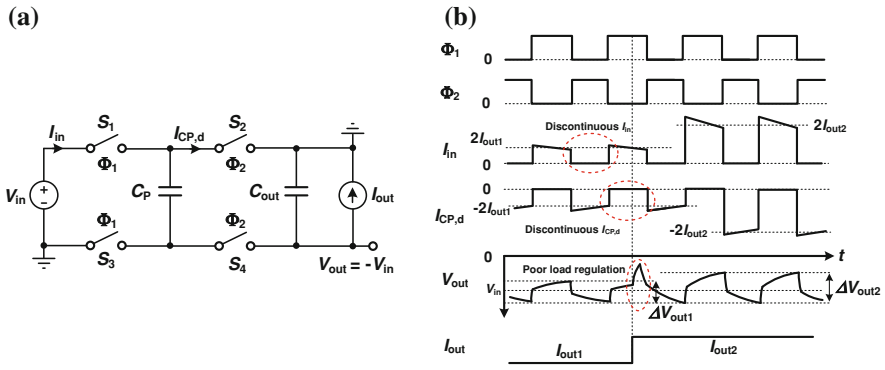


Fig. 6.1 Voltage inverter: **a** schematic and **b** timing waveforms

possible solution to overcome these drawbacks is to increase the switching frequency, however, at the expense of higher switching power loss of the converter.

One effective technique to minimize the voltage and current ripples in SC power converters and simultaneously improve its load regulation and transient response is to employ an interleaving regulation technique. Such a power converter exploits a cellular architecture, where a large power stage is divided into paralleled cells that share the same input and output power busses. Each cell processes a fraction of the total output power, leading to several benefits such as input and output ripple reduction and improved transient response.

The interleaving regulation scheme was originally introduced in switch mode power converters [1]. Its operating principle can be explained with the aid of Fig. 6.2. In a traditional buck converter illustrated in Fig. 6.2a, it can be observed that the inductor is charged when $\Phi_1 = 1$ and it is discharged when $\Phi_1 = 0$. This leads to a discontinuous input current, large inductor current ripples and large output voltage ripples. On the other hand, if n power stages are connected in parallel and operated with a phase difference of $360^o/n$ between the adjacent cells, the peak current and voltage levels can be significantly minimized. As an example, Fig. 6.2b illustrates four interleaved power stage cells, with each cell delivering a quarter of the total output power. The use of the interleaving regulation scheme leads to continuous input and output currents, which aids in minimizing the switching noise and improving load transient response.

While the interleaving scheme described in Fig. 6.2 is implemented for switch mode DC–DC converters, the same principles can be effectively applied to SC power converters while leveraging all its advantages. In general, the use of interleaving regulation through n sub-converters reduces the magnitude of the output voltage ripple by a factor of n, while also extending the system bandwidth by n times. Moreover, it significantly improves the robustness and fault tolerance capability of the power supply. For instance, if one sub-converter fails to operate due to circuit malfunction or device failure, the remaining $n-1$ sub-converters will extend their own regulation times and compensate for the loss.

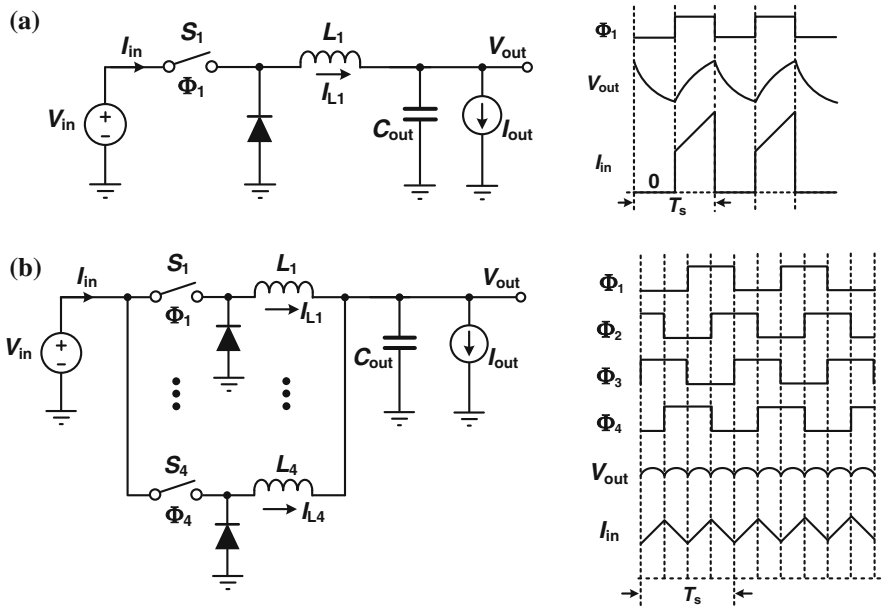


Fig. 6.2 Switch mode power converter and its timing diagrams **a** without and **b** with interleaving regulation (n = 4)

Hence, the remainder of this chapter deals with configuring SC power converters using the interleaving regulation scheme. Accordingly, state-of-the-art interleaving SC power converters are discussed, with regards to system architecture, control algorithms, power stage interleaving mechanisms and circuit design strategies.

6.2 Interleaving Regulation in Reconfigurable Charge Pumps

As the first SC power converter to be discussed in this chapter, this section presents the design of a reconfigurable SC power converter employing the interleaving regulation scheme. While the initial motivation for interleaved charge pump topologies was to improve the voltage/current ripple characteristics and the transient response, this principle can also be exploited in reconfigurable SC power converters.

As discussed in Chap. 5, reconfigurable SC power converters can regulate the output at multiple CGs, thereby broadening the operating voltage range. This makes these architectures highly attractive for modern portable devices that integrate diverse electronic components and employ energy harvesting mechanisms. In this context, the use of interleaving control techniques can further enhance the performance of reconfigurable SC power converters, making them

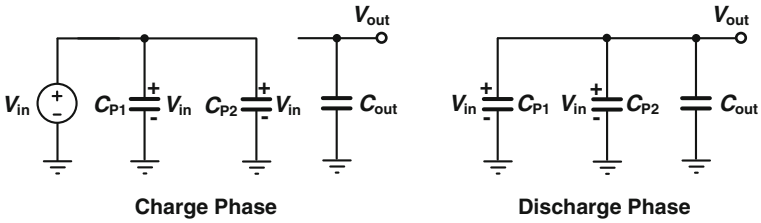
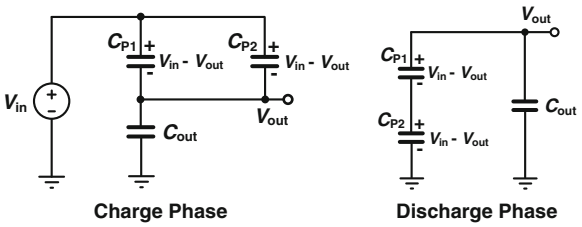


Fig. 6.3 Pumping capacitor configuration to implement CG = 1

Fig. 6.4 Pumping capacitor configuration to implement CG = 2/3



highly desirable for self-powered applications. Hence, as the first step, this section presents the reconfiguration mechanism of the pumping capacitors to achieve multiple CGs. Following this, the principle of interleaving regulation in the power stage is applied. Lastly, the overall operation and design of the reconfigurable step-down charge pump is discussed.

To achieve step-down voltage conversion, during the charge phase, the pumping capacitors are traditionally connected between the input and the output of the converter. During the discharge phase, the pumping capacitors are then connected in parallel with the output capacitor. As a design example, the step-down SC converter described in this section employs two pumping capacitors, C_{P1} and C_{P2}. This allows the power converter to provide multiple CGs of 1, 2/3, 1/2 and 1/3.

The configuration of the pumping capacitors to implement a CG = 1 is illustrated in Fig. 6.3. During the charge phase, the pumping capacitors C_{P1} and C_{P2} are connected across the input supply and the ground node. This causes both the capacitors to be charged to V_{in}. During the discharge phase, when the pumping capacitors are connected between the output node and ground, the voltage across C_{out} gets raised to V_{in}. In this manner, a CG of 1 is achieved.

Figure 6.4 illustrates the charge and discharge phase capacitor configurations for a CG = 2/3. During the charge phase, C_{P1} and C_{P2} are connected between the input and the output node. This charges the capacitors to a voltage $V_{in}-V_{out}$. During the discharge phase, C_{P1} is stacked on top of C_{P2} and this combination is connected in parallel with C_{out}. This leads to a V_{out} given by

$$V_{out} = 2 \times (V_{in} - V_{out}). \tag{6.1}$$

When Eq. (6.1) is solved, the conversion gain CG = V_{out}/V_{in} = 2/3.

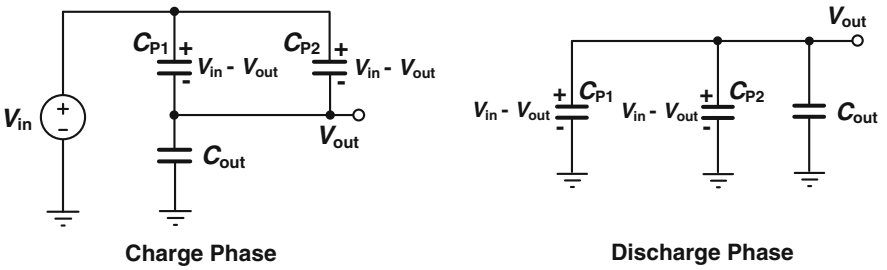


Fig. 6.5 Pumping capacitor configuration for CG = 1/2

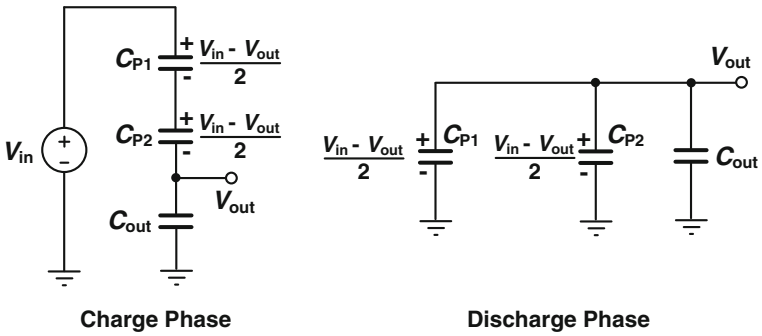


Fig. 6.6 Pumping capacitor configuration for CG = 1/3

Figure 6.5 illustrates the charge and discharge phase capacitor configurations to achieve a CG = 1/2. During the charge phase, C_{P1} and C_{P2} are connected between the input and the output node and each capacitor is charged to $V_{in}-V_{out}$. During the discharge phase shown, the pumping capacitors are connected between the output and ground. This charges the output to a voltage V_{out} given by

$$V_{out} = V_{in} - V_{out}. \tag{6.2}$$

When Eq. (6.2) is solved, CG = V_{out}/V_{in} = 1/2.

Figure 6.6 illustrates the capacitors configurations during the charge and discharge phase, for a CG = 1/3. During the charge phase, C_{P1} and C_{P2} are connected in series between the input and the output nodes. This connection charges the each of the capacitors to a voltage of $(V_{in}-V_{out})/2$. During the discharge phase, they are connected in parallel across C_{out} and V_{out} is calculated as

$$V_{out} = \frac{V_{in} - V_{out}}{2}. \tag{6.3}$$

When Eq. (6.3) is solved, CG = V_{out}/V_{in} = 1/3.

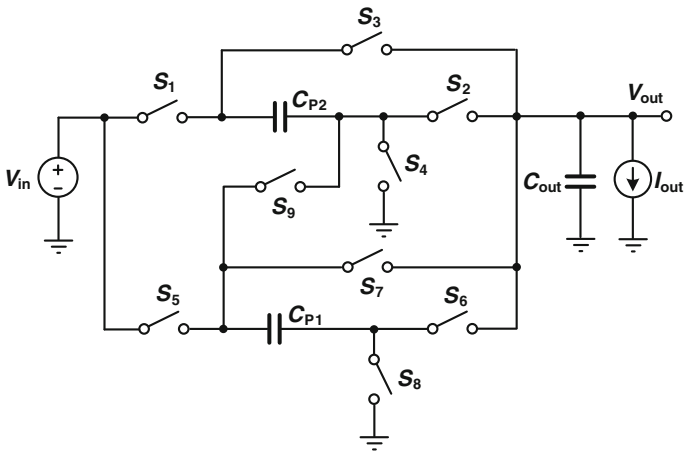


Fig. 6.7 Reconfigurable SC power stage with multiple step-down CGs

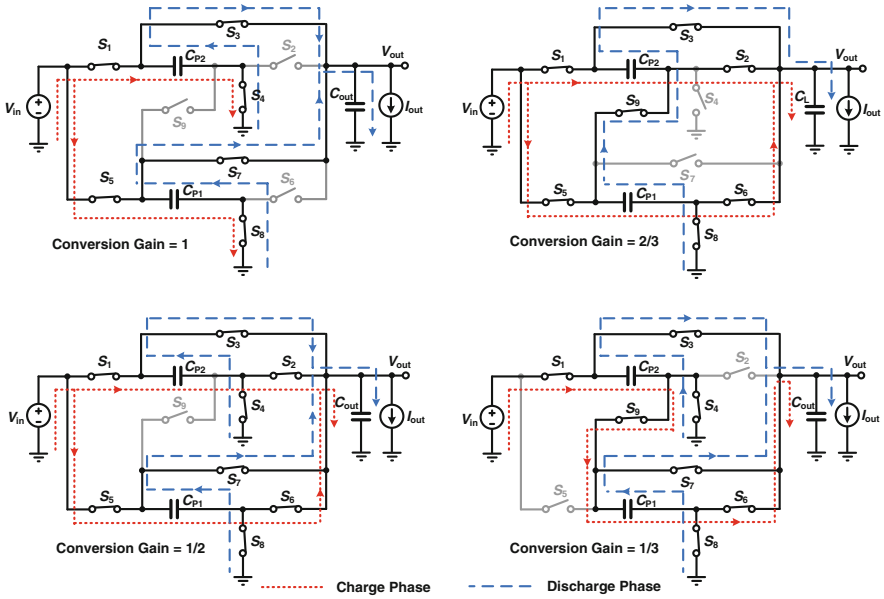


Fig. 6.8 Charge/discharge path reconfiguration to achieve multiple CGs

Based on the capacitor configurations required to achieve the desired step-down CGs, a reconfigurable charge pump is designed and is illustrated in Fig. 6.7. It employs nine switches that are strategically placed in order to achieve the required pumping capacitor topologies, during both the charge and the discharge phases. The configuration of the charge pump for each CG is illustrated in Fig. 6.8.

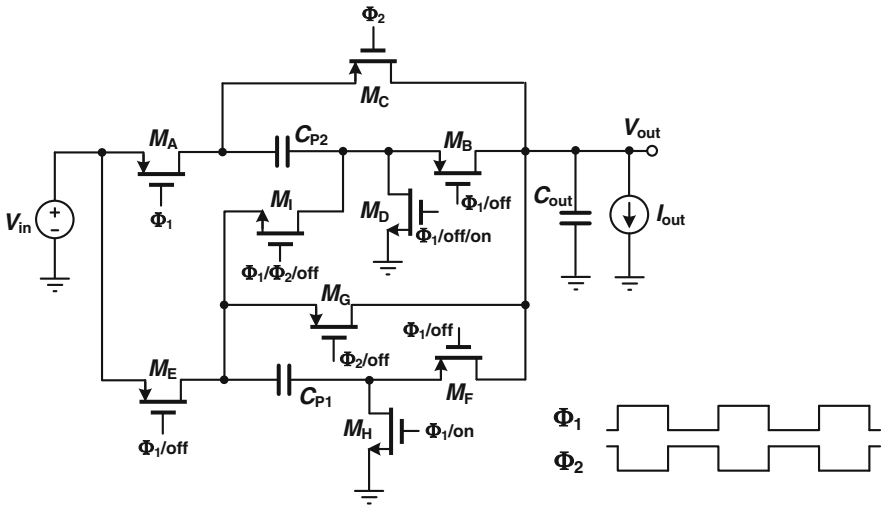


Fig. 6.9 Transistor level implementation of the reconfigurable step-down charge pump

Table 6.1 Gate control signals for the reconfigurable step-down SC power converter

CG	M_A	M_B	M_C	M_D	M_E	M_F	M_G	M_H	M_I
1	Φ_1	Off	Φ_2	On	Φ_1	Off	Φ_2	On	Off
2/3	Φ_1	Φ_1	Φ_2	Off	Φ_1	Φ_1	Off	Φ_1	Φ_1
1/2	Φ_1	Φ_1	Φ_2	Φ_1	Φ_1	Φ_1	Φ_2	Φ_1	Off
1/3	Φ_1	Off	Φ_2	Φ_1	Off	Φ_1	Φ_2	Φ_1	Φ_2

The multiple CG capability is used to jointly improve the efficiency, line/load regulation and DVS performance. The step-down SC power converter regulates the output voltage to its corresponding reference value while delivering power efficiently, under a wide range of input voltages. The converter achieves this through the use of a feedback controller that selects the appropriate CG. Moreover, during heavy loading scenarios, the SC power converter reconfigures the charge pump to provide a CG that is higher than the optimal value. This enhances the power delivery capability of the SC converter. Thus, using a combination of higher and optimum CGs provides a secondary control parameter to the controller to achieve improved system performance.

Figure 6.9 depicts the transistor level implementation of the reconfigurable step-down charge pump. NMOS and PMOS transistors are carefully selected in order to obtain charge/discharge power paths with minimum resistance and smallest transistor size. Furthermore, Table 6.1 gives the gate control signal for each transistor, in order to implement all the CGs, where Φ_1 and Φ_2 are complementary clock signals.

The operation of the charge pump is explained based on the gate control signals, for CG = 2/3 as an example. In each switching cycle, the operation of the charge pump can be divided into two phases, the charge phase Φ_1 and discharge phase Φ_2. In order to achieve a CG of 2/3, during the charge phase $\Phi_1 = 0$ ("0" effective), the PMOS switches M_A, M_B, M_E and M_F are turned on. As a result, the pumping capacitors C_{P1} and C_{P2} are connected in parallel between the input and output nodes and are charged to a voltage $V_{in}-V_{out}$. During the discharge phase $\Phi_2 = 0$ ("0" effective), the switches M_C, M_I and M_H are on, while M_A, M_B, M_E and M_F are off. C_{P1} and C_{P2} are now connected in series across the output terminal, causing the stored charges to be transferred to C_{out}. If $C_{P1} = C_{P2}$, the continuous charge and discharge process leads to a V_{out} equal to $2/3 \times V_{in}$. Similarly, the charge pump can be configured to achieve the other conversion gains.

In order to improve the transient performance and reduce the voltage/current ripples, the step-down SC power converter employs an interleaving regulation technique by adding an additional charge pump sub-cell to the system. The overall charge pump topology of the SC power converter is illustrated in Fig. 6.10. It consists of two sub-cells, Cell 1 and Cell 2 that are connected in parallel between the input and output terminals. To achieve an interleaved operation, the gate control signals of each transistor in Cell 1 and Cell 2 are made complementary to each other. Hence, when one cell operates in its charge phase and is disconnected from the output, the other cell operates in the discharge phase and regulates V_{out}. The presence of the additional cell in the power stage prevents the charge pump from having to wait until the next clock cycle, in order to respond to a load transient. As a result, the converter's transient response is improved. In addition, although the number of components is doubled, the size of each power transistor is reduced by half when compared to the original, in order to power the same load. Therefore, there is no additional penalty with respect to on-chip silicon area and cost. This implementation also reduces the output voltage ripple and switching noise.

In conclusion, this section discusses the design of a reconfigurable step-down SC power converter, which employs the interleaving regulation scheme. Due to the use of the interleaving scheme, the converter has improved dynamic response to provide good line and load regulation. Moreover, the ability to regulate the output at multiple CGs makes it a good candidate for DVS applications. This capability also enables the system to maintain high efficiency over a large input range.

6.3 Practical Interleaved SC Power Converters

Following the introduction to interleaving regulation in power converters and its use in reconfigurable charge pumps, this section investigates several cases in practical interleaved SC power converter designs. The study will focus on closed loop system designs to improve efficiency and performance, along with the design of power supplies for applications such as low power microsensors and highly

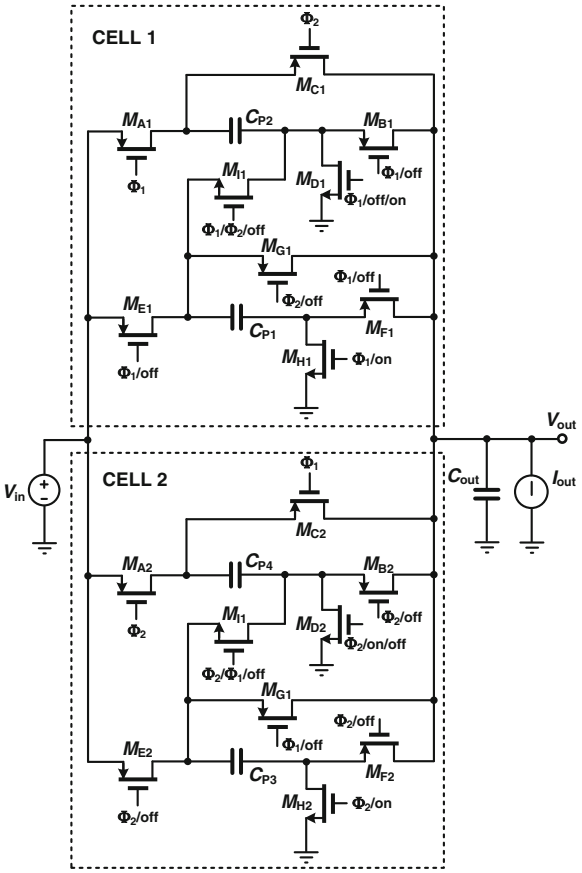


Fig. 6.10 The step-down SC power stage with dual interleaving cells

noise-sensitive devices. Each of the power converters discussed are designed by considering various application-specific requirements such as efficiency, load power, transient response, form factor, and so on.

6.3.1 Case Study 1: Interleaved Cross-Coupled Voltage Doubler

While applying interleaving regulation principles to SC power converters leads to numerous advantages, there are several challenges that have to be addressed during its practical implementation. In such power converter designs, the charge and discharge mechanism of each of the pumping capacitors involves the use of more power components, circuit loops and complex algorithms. This increases the cost and on-chip silicon area requirements, which are critical design constraints that can negate the performance gains achieved from interleaving topologies.

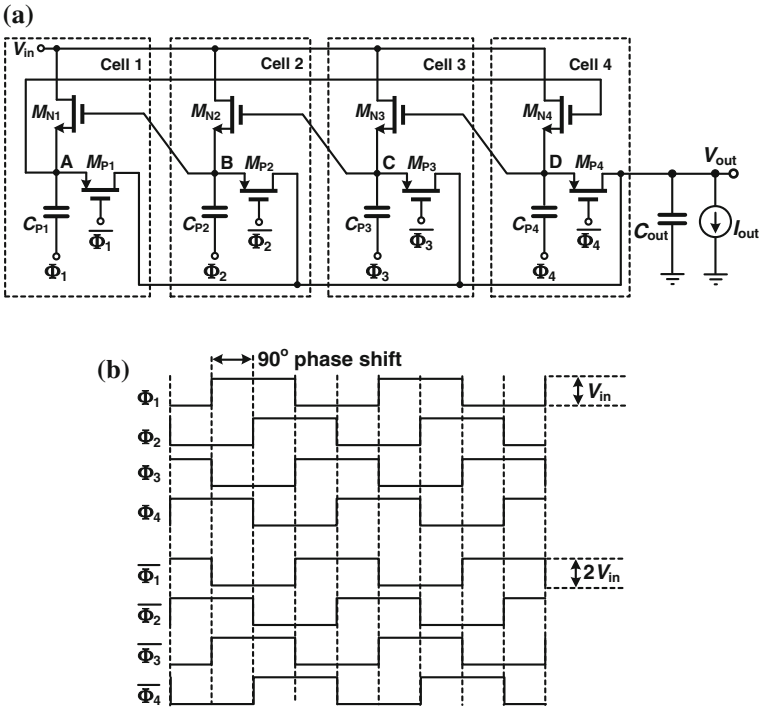


Fig. 6.11 A 4-cell interleaving charge pump **a** schematic, and **b** timing diagram

To illustrate these challenges, consider the implementation of a simple 4-phase interleaved charge pump. It consists of 4 sub-cells that are connected in a closed loop, as illustrated in Fig. 6.11a. The clock signals for the circuit are illustrated in Fig. 6.11b, where each clock signal has a 90° phase difference from its adjacent cell. The clock signal $\bar{\Phi}_i$ is the complement of Φ_i, but has an amplitude of $2V_{in}$. This is required to completely turn off the PMOS power transistors during the charge phase of the pumping capacitors. However, certain drawbacks exist with this design. Firstly, this charge pump requires the use of voltage boosting circuits to generate the complementary clock signals. This increases the cost and on-chip silicon area. Secondly, the input current from V_{in} is still discontinuous, due to the use of non-overlapping clock signals. As a result, the input current ripple and inrush currents are not improved. Lastly, when either of the clock signals is high, only one pumping capacitor operates in its charge phase. For example, during the phase $\Phi_1 = 1$, node A is charged to $2V_{in}$. This turns on the transistor M_{4N}, which charges the pumping capacitor C_{P4} to V_{in}. However, capacitors C_{P2} and C_{P3} have to wait until the next clock cycle before they are charged. Hence, even though the 4-cell charge pump has a better load transient performance when compared to its single cell counterpart, its transient response is not fully maximized.

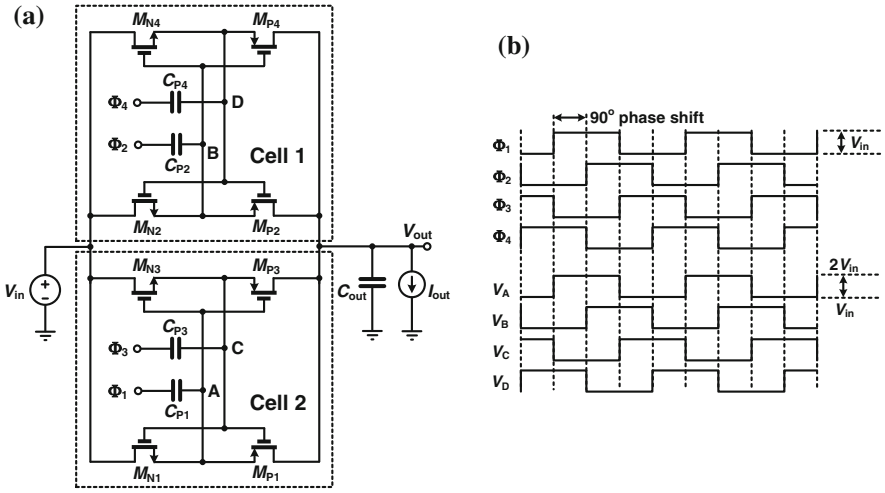


Fig. 6.12 A two-stage cross-coupled interleaved charge pump **a** schematic and **b** timing diagram

To overcome these drawbacks, this case study discusses the design of an interleaved charge pump topology for integrated SC power converters, as illustrated in Fig. 6.12. The circuit architecture consists of two parallel-connected cross-coupled voltage doublers. The charge pump is controlled by clock signals Φ_i, where $i = 1, 2, 3, 4$, with a 90^o phase shift between each other. One of the major improvements of this topology is that the gate control signals for each PMOS and NMOS power transistors are generated internally. This avoids the need for additional clock generators and voltage boosting circuits.

The operation of the charge pump in steady state can be explained as follows. From the timing diagram in Fig. 6.12b, it can be seen that, at any instant, two clock signals are always high. This allows two pumping capacitors to be charged to V_{in}, while the remaining two are discharged to V_{out}. For example, consider the case when the clock signals $\Phi_1 = 1$, $\Phi_2 = 1$, $\Phi_3 = 0$ and $\Phi_4 = 0$. In this scenario, node B in Cell 1 is charged to $2V_{in}$, while the voltage at node D is less than V_{in}. Hence, C_{P2} discharges to the output through the switch M_{P2}, while C_{P4} is charged to V_{in} through the switch M_{N4}. Simultaneously, in Cell 2 node A is charged to a voltage level of $2V_{in}$, while the voltage at node C is less than V_{in}. Thus, C_{P1} discharges to V_{out} through transistor M_{P1}, while C_{P3} is charged to V_{in} through M_{N3}. In this manner, since two capacitors always deliver charge to the output, the charge pump has a smaller output voltage ripple and a faster transient response.

The first step in the design of the interleaved cross-coupled SC power converter involves the design of the charge pump. To optimally size the power switches, similar to the charge pump design presented in Sect. 5.3.2, all the major power loss components have to be identified. For the cross-coupled charge pump, the total power loss is a summation of the conduction loss, switching loss and redistribution loss. To simplify its analysis, the charge pump can be considered to consist of four

sub-cells. Each cell can be regarded to comprise of one PMOS transistor, one NMOS transistor and a pumping capacitor. To ensure that the turn-on resistance is the same, the switches are designed such that $\mu_n W_{NMOS} = \mu_p W_{PMOS}$. Then, the total power loss can be modeled as

$$P_{tot} = \left(\frac{V_{out}}{R_{out}}\right)^2 \left[\frac{1}{2}\frac{1}{\mu_n C_{ox}(V_{in} - V_{TH})}\frac{L}{W_{NMOS}} + \frac{1}{4}ESR_{CP} + \frac{1}{4f_s C_P}\right] + 16C_{ox}f_s V_{in}^2 L W_{NMOS}. \quad (6.4)$$

The size of the NMOS power transistors is then chosen such that $\partial P_{tot}/\partial W_{NMOS} = 0$. Based on their relationship, the size of the PMOS transistors can also be appropriately chosen. Similarly, the optimal switching frequency f_s for the charge pump can be designed based on the condition $\partial P_{tot}/\partial f_s = 0$.

The second step in the design of the cross-coupled SC power converter involves the feedback controller design. As illustrated in Fig. 6.13, the system architecture employs a digital based feedback control technique. Digital circuits are well known for their large noise margin. Since SC power converters are typically noisy, due to frequent switching activities, it is desirable for the controller to be immune to this noise. Hence, a digital implementation becomes quite attractive. In addition, since a processor is a common core module in modern VLSI systems, the control functions of the feedback controller can be implemented by utilizing the abundant resources available in the processor. This mitigates the need for additional on-chip silicon real estate, thereby minimizing the system volume and cost.

Thus, the interleaving cross-coupled SC converter employs a digital hysteretic feedback control technique. As illustrated in Fig. 6.13, it consists of a digital hysteretic feedback controller and a reference clock generator, to achieve closed-loop voltage regulation. The first step involves the conversion of V_{out} from an analog voltage to a digital signal. This requires the design of an A/D converter. The use of traditional A/D converter structures, such as the pipelined ADC, flash ADC, SAR ADC, and so on are not preferred, since it occupies large silicon area, consumes considerable power and is very sensitive to noise. Recently, ring-oscillator and delay-line A/D converters have been reported [2]. Compared with the traditional designs, these implementations are more area and power efficient, since they rely on basic digital logic gates as their key building blocks.

In this converter design, a ring-oscillator based A/D converter is utilized, as illustrated in Fig. 6.14. This is because they are more area-efficient when compared to their delay-line counterparts, as delay elements are reused even within a single switching cycle. The circuit consists of a NOR gate, four delay cells, and one pulse counter. Each delay cell is comprised of two inverters. The pulse counter is an asynchronous positive edge triggered N-bit counter. Note that the NOR gate and the delay cells are powered by V_{out}. When the "Start" signal is high, the loop remains in a static state and the outputs of delay cells are maintained low. When the "Start" signal goes low, the loop oscillates and a series of pulses are generated at V_{ADC}, with an oscillation frequency of f_{out}. f_{out} is dependent on V_{out} as per the expression

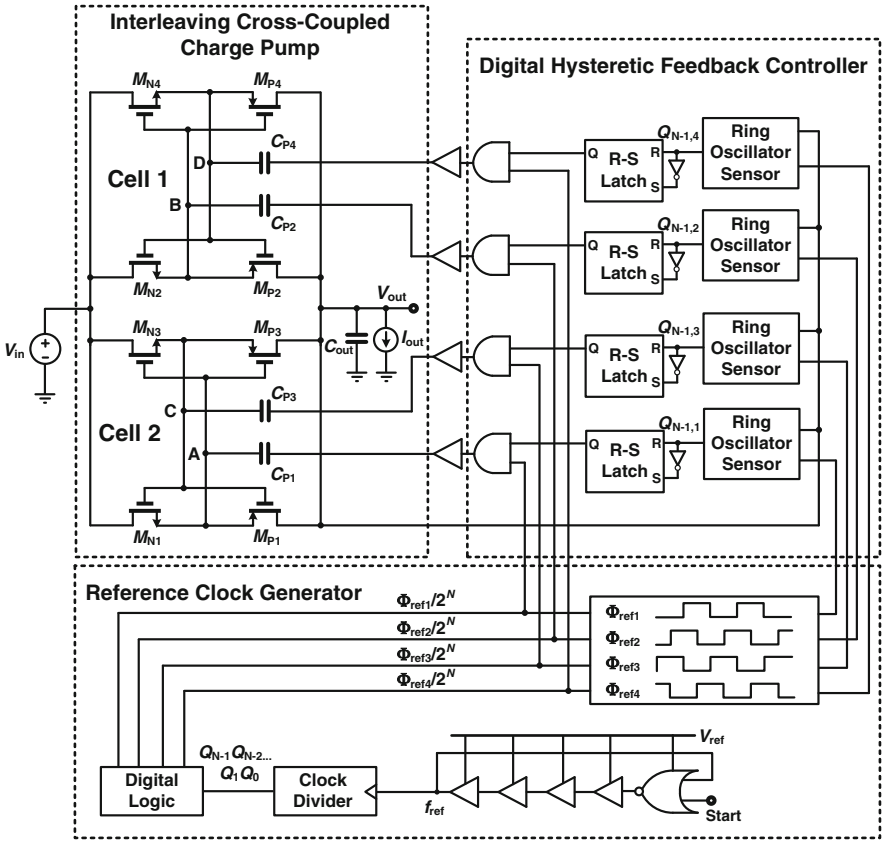


Fig. 6.13 System architecture of the digital based interleaving cross-coupled SC power converter

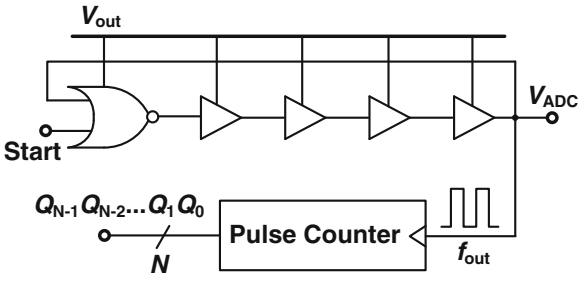


Fig. 6.14 Ring-oscillator based analog-to-digital converter

$$f_{\text{out}} = \frac{\beta(V_{\text{out}} - V_{\text{TH}})^2}{2k \times N \times C_{\text{delay}} \times V_{\text{out}}}, \tag{6.5}$$

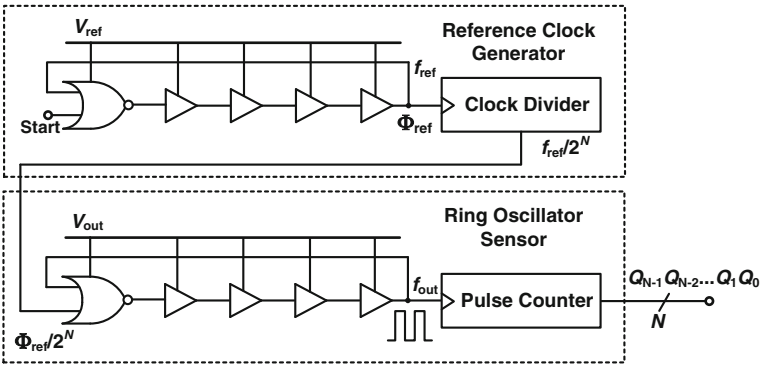


Fig. 6.15 Ring oscillator based error sensing circuit

where k and β are process dependent parameters, N is the number of stages in the ring oscillator, and C_{delay} is the output capacitance of one delay cell. From Fig. 6.14, it can be observed that f_{out} serves as the control signal for the N-bit pulse counter. Hence, by examining its output $Q_{N-1},\ldots,Q_0$, the digital representation of V_{out} is obtained.

To detect the voltage regulation error between V_{out} and V_{ref}, two identical ring oscillator based A/D converters are used as the voltage error sensor, as shown in Fig. 6.15. The upper ring oscillator is powered by V_{ref} and generates a clock signal Φ_{ref} with a frequency of f_{ref}. This signal passes through a clock divider and generates a second clock signal $\Phi_{ref}/2^N$ with a frequency equal to $f_{ref}/2^N$, where N is the number of bits in the clock divider. $\Phi_{ref}/2^N$ is then used as the "Start" signal for the second ring oscillator, which is powered by the output of the SC power converter. When $\Phi_{ref}/2^N = 0$, the second oscillator oscillates with a frequency of f_{out}. This drives the pulse counter to count the number of pulses in a fixed time period. Finally, the pulse counter generates a $(N-1)$-bit binary signal, $Q_{N-1},\ldots,Q_0$. Based on the value of $Q_{N-1},\ldots,Q_0$, the controller can identify the error between V_{out} and V_{ref} and thus regulate the output appropriately. In this design, $V_{out} < V_{ref}$ when $Q_{N-1},\ldots,Q_0 < 10\ldots0$, $V_{out} = V_{ref}$ when $Q_{N-1},\ldots,Q_0 = 10\ldots0$ and $V_{out} > V_{ref}$ when $Q_{N-1},\ldots,Q_0 > 10\ldots0$.

Hysteretic control has been typically employed in switch mode power converters for voltage regulation [3]. Its nonlinear control mechanism makes the closed-loop system unconditionally stable, because the control depends only on the current-state comparison between the output voltage and one of the hysteretic bounds and does not rely on previous states of the system. However, one of its major drawbacks has been observed during load transients. In such scenarios, the inductor current cannot immediately adapt to the sudden load change, thereby leading to large output voltage ripples. However, a charge pump does not suffer from this, due to the absence of inductive elements. When the output voltage is higher than the reference voltage, the PMOS switches are turned off and the output voltage drops immediately. When the output voltage is lower than the reference,

the PMOS switches are turned on. The charge stored on the pumping capacitor is transferred to the output, leading to an instantaneous rise in the output voltage. Hence, hysteretic control can be applied to SC power converters to achieve fast transient response.

The overall closed-loop operation of the SC power converter and the digital hysteretic controller can be explained with the aid of Fig. 6.13, as follows. Initially, the reference voltage V_{ref} is used to power a ring oscillator, in order to generate four reference clocks, $\Phi_{\text{ref}i}$ ($i = 1, 2, 3, 4$), through digital logic gates. These clock signals operate as the "Start" signal for four identical voltage error sensors that are powered by V_{out}. It was seen that if $V_{\text{out}} > V_{\text{ref}}$, then the $Q_{\text{N}-1}$ bit will be 1 and for other conditions it will be 0. Thus, the $Q_{\text{N}-1,\text{i}}$ bits from the sensors can indicate if the output voltage either exceeds or is lower than V_{ref}. Hence, these bits operate as the control signal to either activate or deactivate the charge pump cells. This is implemented through the use of simple R-S latches, which guarantee that the charge pump is clocked when the $Q_{\text{N}-1,\text{i}}$ bits are at logic 0 and vice versa when the bits are at logic 1. To achieve a hysteretic operation, a hysteresis window of 1-LSB of the ring oscillator A/D converter is utilized.

In conclusion, this section presents the design of an interleaving cross-coupled voltage doubler. The use of a fully digital control technique makes the system quite robust to noise and even device failure. The digital hysteretic control adopted in the controller significantly enhances the transient response, and allows for easy integration into advanced microprocessors based systems. Thus, when combined with the design principles for the power stage, the interleaving SC power converter can achieve optimal power efficiency, improved transient response and minimized voltage and current ripples. It provides a very cost-effective power supply solution for low voltage, high-performance integrated systems.

6.3.2 *Case Study 2: Master-Slave SC Power Converter Design for Ultra Low Power Energy Harvesting Microsensors*

Advances in biomedical and wireless sensing technologies have led to the proliferation of self-powered energy-efficient microsensors. These sensors rely on advanced energy harvesting techniques to extend their operating lifetime and improve system robustness. However, these applications operate with an ultra-low power budget, which makes the design of corresponding SC-based power management systems highly challenging.

Firstly, as the output load power decreases to sub-mW levels or below, power loss components that were initially ignorable for traditional designs become very critical and should be carefully re-evaluated. Of these power loss components, reversion loss that occurs when a high voltage node is shorted to a low voltage node, becomes critical at very low output power levels. Secondly, in traditional SC power converter designs, the power dissipation of the controller can be of the order of few mWs.

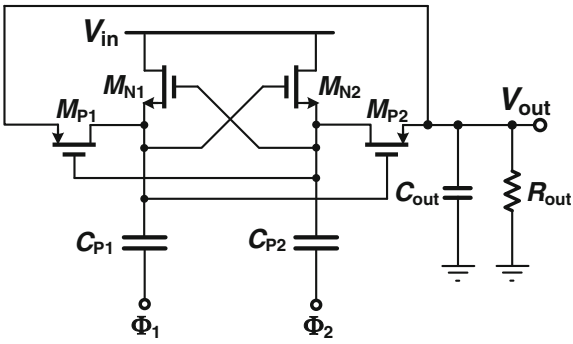


Fig. 6.16 A cross-coupled voltage doubler

However, for ultra-low power microsensors, the power budget of the entire system is expected that be maintained below 1 mW. As a result, the power dissipation of the controller should be scaled down to the order tens of μW or below. Thirdly, a SC power converter normally requires many off-chip capacitors, on-chip pads and IC pins, thereby increasing volume and cost. The resulting parasitic components can also cause serious switching noise and glitches. However, numerous emerging applications place considerable emphasis on system miniaturization, thereby providing a motivation to implement a monolithic power supply.

Therefore, to address these system level challenges for ultra low power supply designs, this section presents a monolithic SC power converter. It features a master-slave interleaving charge pump and a feedback controller that operates purely in the subthreshold region. The master-slave interleaving charge pump minimizes the reversion power loss and regulates the output voltage by adjusting the size of the pumping capacitor. When compared to the traditional duty ratio adjustment approach, this technique benefits the converter with higher efficiency. The subthreshold design significantly reduces the power dissipation in the controller, making it quite suitable for ultra-low power microsensor applications.

Figure 6.16 illustrates the schematic of the traditional cross-coupled voltage doubler, which is used to demonstrate the principle behind the development of the master-slave power stage. At steady-state, the expression for the output voltage of the voltage doubler can be written as

$$V_{\text{out}} = \frac{2V_{\text{in}}}{1 + \frac{T_s}{2R_{\text{out}}C_P}}. \tag{6.6}$$

Equation (6.6) reveals that the output voltage of the SC converter can be regulated to different voltage levels if the pumping capacitor C_P can be appropriately adjusted. This approach, when compared to the duty ratio adjustment technique, benefits the converter with a higher efficiency.

Based on this observation, as illustrated in Fig. 6.17, the charge pump consists of two cells that serve as the master and slave power stages. In general, the master cell operates at all load conditions, while the slave cell selectively works according

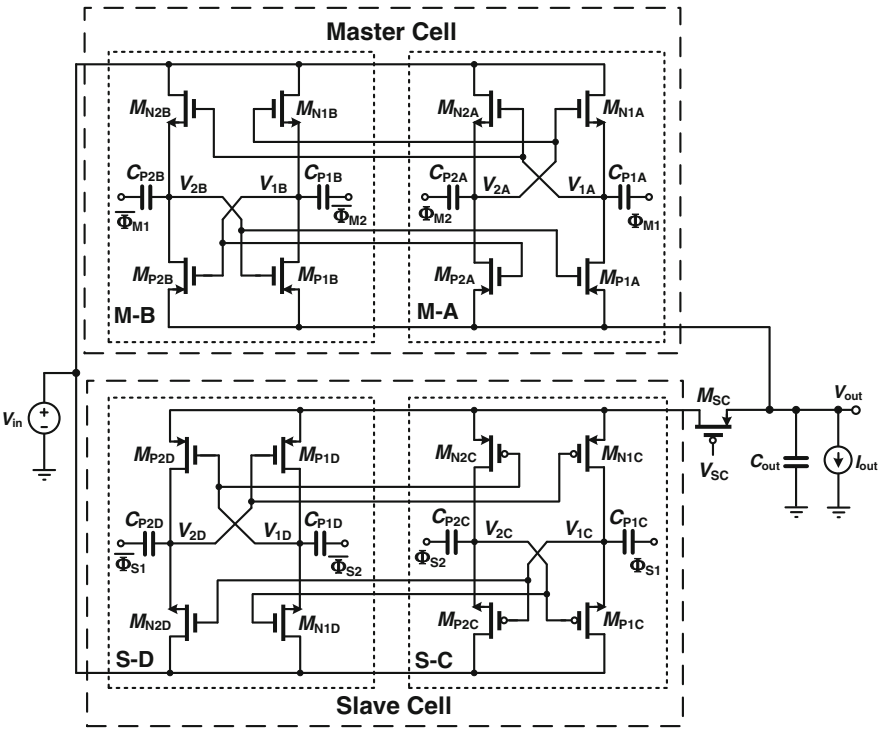


Fig. 6.17 The master-slave interleaving charge pump

to the instantaneous load condition. At light load, V_{out} is usually higher than the desired reference level and thus a large effective pumping capacitance is not required to boost the output voltage. A control signal V_{SC} is thus set to "1" to turn off the PMOS transistor M_{SC}, which shuts down the slave cell. The output voltage is regulated only by the master cell, leading to power savings. During heavy load conditions, typically V_{out} becomes equal to or lower than the reference level, due to a large load current demand. The slave cell is then activated to deliver more current to the output and increase the voltage level of V_{out}.

At the transistor level, the master cell and slave cell consists of interleaving cross-coupled voltage doublers. For example, the master cell is controlled by a set of non-overlapping clock signals Φ_{M1}, Φ_{M2}, $\bar{\Phi}_{\text{M1}}$ and $\bar{\Phi}_{\text{M2}}$. The circuit operation of the charge pump can be explained as follows. When $\Phi_{\text{M1}} = 1$ and $\Phi_{\text{M2}} = 0$, the voltage nodes $V_{1\text{A}}$ in the sub-cell M-A and $V_{1\text{B}}$ in the sub-cell M-B are charged to $2V_{\text{in}}$, while $V_{2\text{A}}$ and $V_{2\text{B}}$ stay at V_{in}. Thus, the power transistors M_{N2A}, M_{N2B}, M_{P1A} and M_{P1B} are turned on, thereby charging the pumping capacitors C_{P2A} and C_{P2B} to V_{in} through M_{N2A} and M_{N2B}, respectively. Meanwhile, the charge stored on C_{P1A} and C_{P1B} are transferred to C_{out} through M_{P1A} and M_{P1B}. When $\Phi_{\text{M1}} = 0$ and $\Phi_{\text{M2}} = 1$, the voltages $V_{1\text{A}}$ and $V_{1\text{B}}$ drop to V_{in}, while $V_{2\text{A}}$ and $V_{2\text{B}}$ is boosted to $2V_{\text{in}}$. This turns on the power transistors M_{N1A}, M_{N1B}, M_{P2A} and M_{P2B}. The

capacitors C_{P1A} and C_{P1B} are charged to V_{in} through M_{N1A} and M_{N1B}. Capacitors C_{P2A} and C_{P2B} pump their stored charge to C_{out} through M_{P2A} and M_{P2B}. As a result, the capacitor combinations C_{P1A}, C_{P1B} and C_{P2A}, C_{P2B} operate in an interleaving manner, to regulate the output voltage to the desired value.

During heavy load conditions, the control signal V_{SC} goes low, in order to activate the slave cell. The control signals for the slave cell are identical to the respective control signals in the master cell. At light load, all the control signals for the slave cell are disabled, thereby eliminating any switching power loss and conduction power loss in the power stage and their corresponding buffer drives. Thus, the power loss is greatly decreased in the charge pump and efficiency at light load is increased.

To minimize the reversion loss in this design, non-overlapping clock signals are employed to control the power switches. Hence, there exists a time duration during which both the clocks Φ_{M1} and Φ_{M2} are low, causing the voltages V_{1A} and V_{2A} to be equal to V_{in}, while V_{1B} and V_{2B} are charged up to $2V_{in}$. Under this condition, all the power transistors in the master sub-cells M-A and M-B are turned off. No reversion current can flow from C_{P1B} and C_{P2B} back to V_{in}, or from C_{out} back to C_{P1A} and C_{P2A}. Hence, reversion power loss is substantially eliminated.

To minimize the power loss contribution from the controller, it is operated in the subthreshold region. In this region of operation, the current densities are very low, resulting in a higher ratio of the transconductance to bias current of the transistor. The drain current is exponentially dependent on the gate voltage and is given by

$$I_D = I_0 \exp\left(\frac{V_{gs} - V_{TH}}{nV_T}\right), \tag{6.7}$$

where V_{TH} is the threshold voltage of the transistor, V_T is the thermal voltage and n equals $1 + C_{js}/C_{ox}$, where C_{js} is the depletion region capacitance and C_{ox} is the gate oxide capacitance. In contrast to traditional circuits, subthreshold circuits can be designed to operate at very low power levels, due to much lower gate drive voltage and current densities.

For example, Fig. 6.18 depicts the low power characteristics of a traditional digital ring oscillator and its subthreshold counterpart. Compared to traditional CMOS digital logic circuits that have a full gate-drive voltage swing of V_{in}, subthreshold circuits require a voltage swing of the order of a MOSFET threshold voltage or even lower, thereby leading to significant power savings.

The exponential relationship between the drain current I_D and gate-to-source voltage V_{gs} makes the subthreshold operation very suitable for implementing circuits that require widely adjustable parameters. To further enhance their robustness, source-coupled logic (SCL) designs are adopted for the implementation of reliable, ultra-low power controller circuits. In such SCL circuits, each logic gate operates at current levels of the order of tens of nAs and voltage swings of the order of hundreds of mVs. This allows subthreshold logic gates to operate in a low-voltage design environment, whiles still ensuring robust system operation.

In an SCL gate, the logic operation takes place mainly in the current domain. For example, Fig. 6.19 illustrates a conventional SCL-based inverter. The logic

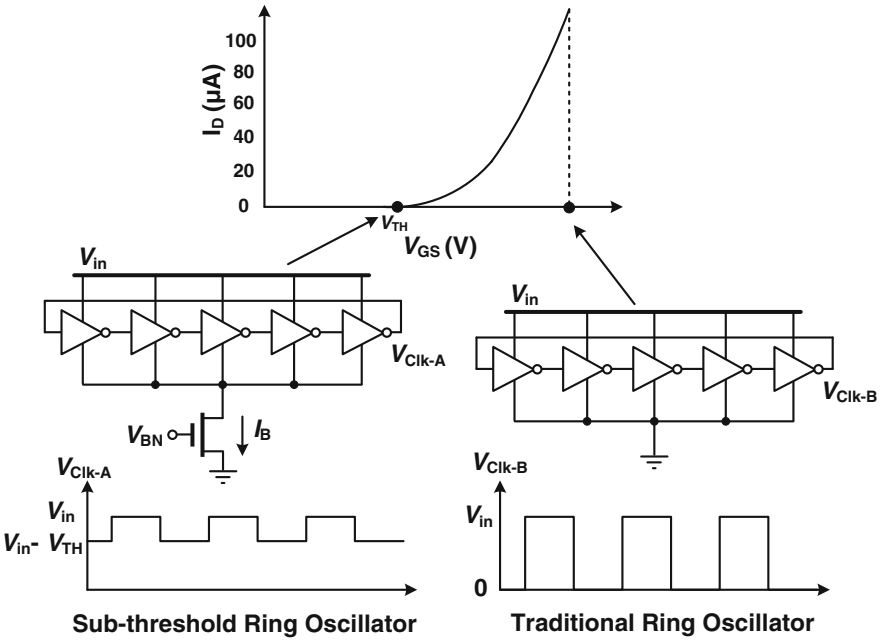


Fig. 6.18 Subthreshold and traditional ring oscillator implementations

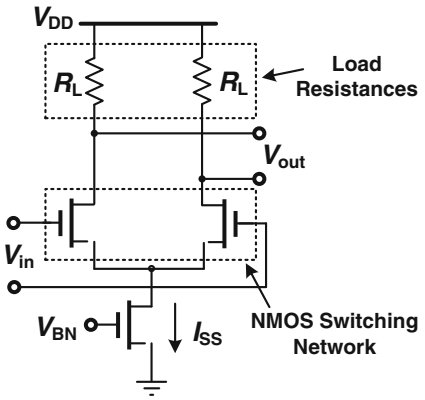


Fig. 6.19 A conventional SCL-based inverter/buffer circuit

network consists of an NMOS source coupled differential pair that steers the tail current I_{SS} to one of the output branches, based on the input logic levels. The load resistance R_L converts the branch current back into the voltage domain, in order to drive the subsequent SCL gates. Thus, the voltage swing at the output node, which is given by $V_{SW} = R_L \times I_{SS}$, should be large enough to drive the input differential pair, present in the subsequent stage. Based on this observation, the voltage swing should satisfy the condition

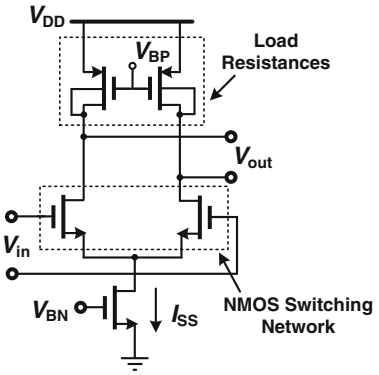


Fig. 6.20 A SCL-based inverter/buffer circuit with PMOS load device

$$V_{SW} > knV_T, \tag{6.8}$$

when the NMOS transistors are in weak inversion. Here, n is the subthreshold slope and V_T is the thermal voltage. k is a parameter that is dependent on the CMOS process being used. Thus, the required voltage swing when transistors operate in the subthreshold region can be as low as knV_T, which is approximately 150 mV at room temperature and assuming $n = 1.5$ and $k = 4$. From Eq. (6.8), it can be observed that the voltage swing in the subthreshold region depends only on n and k. It is independent of the threshold voltage of the NMOS transistors. Hence, if the load resistance can be made sufficiently high, then the switching operation of the NMOS transistors has a very low dependence on any process variations. Moreover, if the tail bias current I_{SS} is higher than the junction leakage currents and if the output impedance of the transistors is designed to be larger than the load resistance, then SCL circuits can be effective utilized for logic design, even in aggressively scaled deep-submicron technologies.

In the subthreshold region of operation, to effectively reduce the power dissipation, the tail bias current is typically of the order of a few nA or less. Therefore, to obtain a reasonable output voltage swing at these current levels, the load resistance is desired to be very large, with typical values in the range of hundreds of MΩ. Moreover, this resistance should be accurately controllable, based on the current I_{SS}. Hence, a well-controlled, high resistivity load device with small area is required. For this range of resistances, conventional PMOS transistors biased in the triode region cannot be utilized, since this would lead to impractical channel lengths. To overcome this drawback, voltage controlled PMOS load devices are employed, as illustrated in Fig. 6.20. These PMOS devices have their drain terminals connected to their body terminals, in order to realize a well-controlled resistor.

As the essential elements of the feedback controller, the circuit schematics of the subthreshold R-latch and S-latch are shown in Fig. 6.21.

Figure 6.22 illustrates the flowchart of the proposed control scheme. To achieve output voltage regulation, initially an A/D converter is employed to detect and amplify the error between the scaled output voltage βV_{out} and the reference voltage

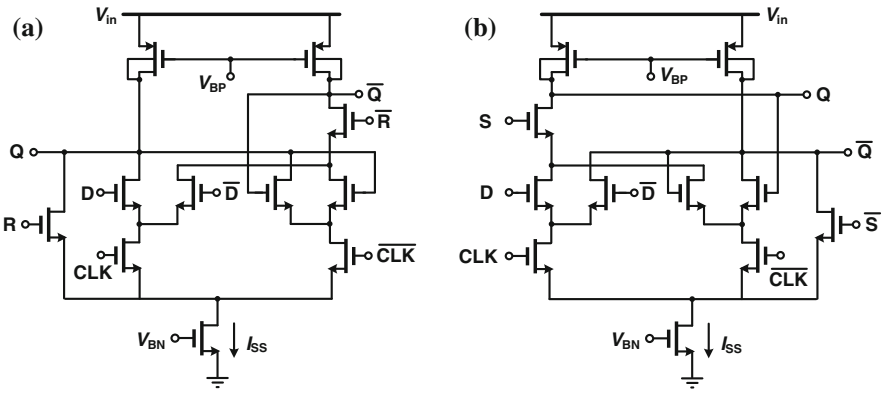


Fig. 6.21 **a** Subthreshold R-latch and **b** subthreshold S-latch

V_{ref}. To achieve this, *V*-to-*I* converters convert the voltage levels into corresponding current signals I_{out} and I_{ref}, respectively. The *V*-to-*I* converters are illustrated in Fig. 6.23, and employ a differential circuit topology that effectively cancels out even-order harmonics and temperature/process variations. Hence, the voltage regulation error is obtained in the form of current as

$$\Delta I = I_{out} - I_{ref} = g_m(\beta V_{out} - V_{ref}). \tag{6.9}$$

Following the *V*-to-*I* conversion, two subthreshold ring oscillators convert the current difference ΔI into a corresponding frequency difference Δf, as illustrated in 6.22. It can be observed that I_{ref} and I_{out} are used to bias the two ring oscillators. With different biasing currents, the oscillation frequency of each oscillator varies accordingly as

$$f_{osc} = k_{RO} I_{bias} + b. \tag{6.10}$$

Equation (6.10) reveals a linear relationship between the oscillation frequency and the biasing current, making the detected voltage error also linearly proportional to Δf. This is given by

$$\Delta f = f_{out} - f_{ref} = k_{RO}(I_{out} - I_{ref}) = k_{RO} g_m(\beta V_{out} - V_{ref}). \tag{6.11}$$

The linear frequency-error relationship greatly simplifies the system modeling and circuit designs.

Following the flow chart in Fig. 6.22, the frequency error information Δf is continuously converted into the digital binary signals, with the aid of subthreshold frequency dividers, R-S pulse counters and digital signal registers. The frequency dividers are composed with subthreshold digital latches. Meanwhile, the synchronous clock signal for the charge pump, which has frequency f_s, is generated with the aid of four subthreshold T flip-flops. The input signal for these flop-flops is obtained from the subthreshold ring oscillator that generates f_{ref}. Thus, the

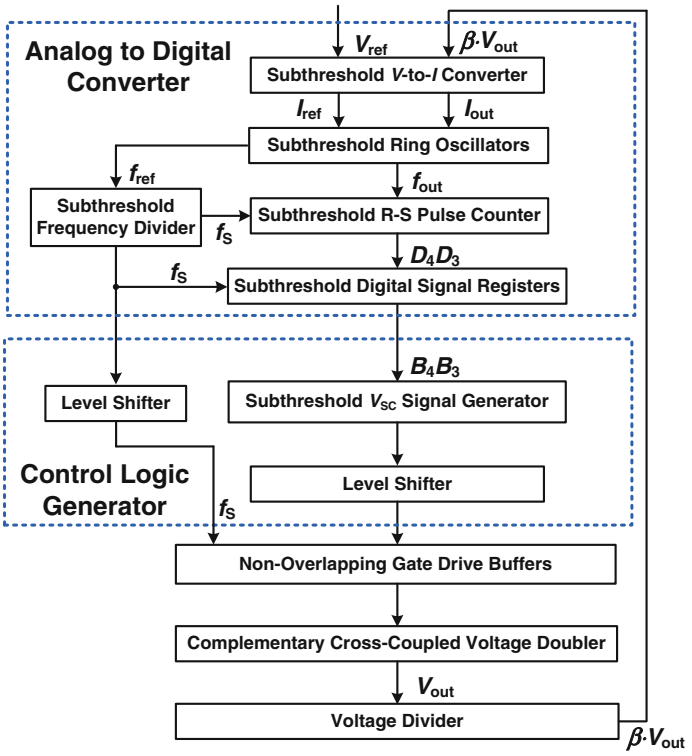


Fig. 6.22 Flow chart of the subthreshold feedback controller

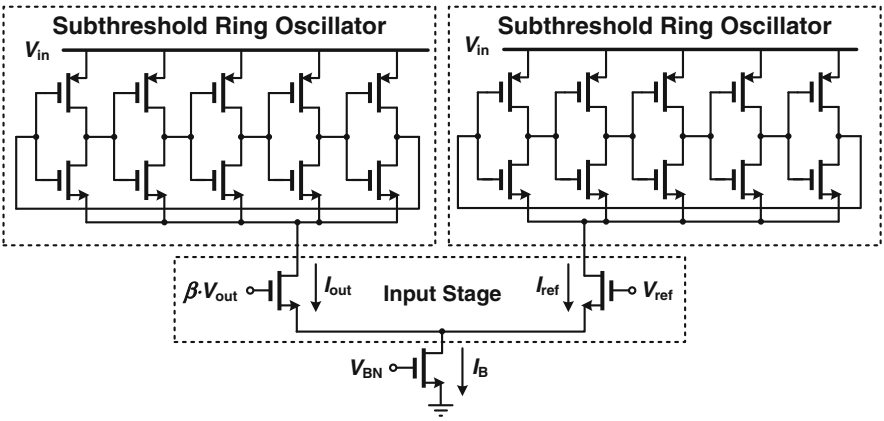


Fig. 6.23 Schematic of a differential *V*-to-*I* converter with subthreshold ring oscillators

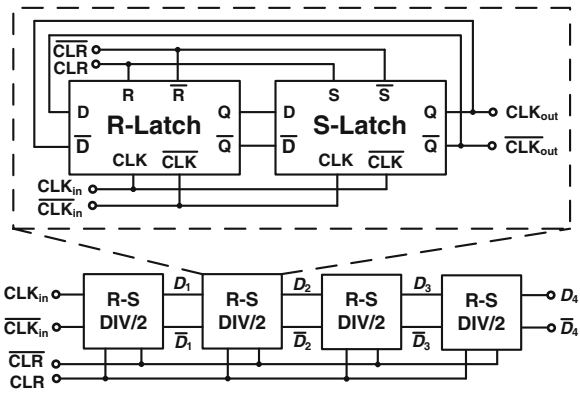


Fig. 6.24 Subthreshold R-S pulse counter

frequency error Δf between f_{out} and f_{ref} is determined by R-S pulse counters that count the number of pulses in the subthreshold ring oscillator controlled by $\beta \times V_{out}$. The circuit schematic of such a counter is illustrated in Fig. 6.24.

Consequently, the digital binary data $D_4D_3D_2D_1D_0$ contains the original error voltage information. The subthreshold digital registers then process this data and convert it to a normalized error data $B_4B_3B_2B_1B_0$. If $B_4B_3B_2B_1B_0$ is equal to "00111", the controller identifies this as the steady-state since this occurs when $\beta \times V_{out}$ is equal to V_{ref}. If $B_4B_3B_2B_1B_0 <$ "00111", $\beta \times V_{out}$ is lower than V_{ref}. The control signal V_{SC} will then be reset to "0", thereby activating the slave cell. Hence, the equivalent pumping capacitance is increased to boost V_{out}. On the other hand, if $B_4B_3B_2B_1B_0 >$ "00111", $\beta \times V_{out}$ is higher than V_{ref}. The control signal V_{SC} will be set as "1", in order to turn off the slave cell. As a result, the equivalent pumping capacitance is reduced to lower the output voltage.

Additionally, since all the controller circuit blocks are designed to operate in the subthreshold region, the voltage swing of each signal is very low. Hence, level shifters are used to recover the gate control signals, which swing from 0 to V_{in}. This allows the buffers to effectively turn on/off the power transistors in the charge pump. Moreover, for the PMOS master/slave control switch M_{SC}, a high gate control voltage level of $2V_{in}$ is required to effectively turn off M_{SC}. Lastly, non-overlapping gate drive buffers effectively switch the power transistors in the charge pump. These buffer drives are designed with sufficient non-overlapping periods, such that reversion currents are eliminated.

In conclusion, this section presents the design of a monolithic SC power converter. It employs a master-slave complementary charge pump with a purely subthreshold controller. By employing the techniques of the reversion loss minimization and subthreshold operation, it provides an effective power supply solution for ultra low-power applications such as wireless microsensors.

6.3.3 Case Study 3: Hybrid Interleaved SC Power Converter for Battery-Powered Portable Applications

As portable electronic devices evolve, a commensurate increase is also observed in transistor integration levels, on-chip system complexity and performance. Thus, stringent design requirements and challenges are placed on the performance and reliability of the power supply. One of the most critical reliability issues is inrush current. For many semiconductor ICs, during power turn-on, a significant inrush current surge can be measured, which can be of the order of a few hundred mAs or even higher. This severely jeopardizes device and circuit reliability and performance. In addition, to achieve power savings, modern power management techniques can switch the operating mode of load devices between 'active' and 'sleep' frequently. Large inrush current is observed even under these conditions. To limit the inrush current surge in power converters, soft-start mechanisms are usually employed. These techniques charge up the inductor current and/or the output voltage gradually with auxiliary circuitries such as oscillators, soft-start capacitors, delay timers, and so on. However, the soft-start periods usually last from tens to a few hundreds of ms, and cannot respond to quick wake-up commands and sudden supply voltage fluctuations.

To overcome the drawback of large inrush current, the interleaving regulation scheme was initially proposed. However, even with this scheme, modern SC power converters continue to suffer from large inrush current surges. To demonstrate this, consider the design of an interleaving SC power converter, presented in Fig. 6.25a [4]. It consists of two identical sets of SC voltage doublers, which are controlled by 2-phase clock signals $\Phi_{1A,2A}$ and $\Phi_{1B,2B}$. The two voltage doublers continuously deliver current to the output V_{out} in a time multiplexing manner. Thus, compared to conventional voltage doublers, this topology can achieve much lower output voltage ripples and switching noise and is more energy efficient. The detailed timing waveforms are illustrated in Fig. 6.25b. As shown in the figure, the two clock signals $\Phi_{1A,2A}$ and $\Phi_{1B,2B}$ are non-overlapping and complementary. A short dead time is inserted between $\Phi_{1A(1B)}$ and $\Phi_{2A(2B)}$ to avoid shoot-through current and thus reduce output switching noise. When $\Phi_{2A} = 1$ and $\Phi_{2B} = 0$, switches S_{3A} and S_{4A} are turned on and the top voltage doubler operates in the discharge phase. The node V_{2A} is charged up from ground to the input supply V_{in}, to deliver the charge stored on C_{P1} to the output capacitor C_{out}. The output voltage V_{out} then approximately settles at $2V_{in}$. In the meantime, S_{1B} and S_{2B} are closed and the bottom voltage doubler operates in the charge phase to charge up C_{P2}. Similarly, during the phase $\Phi_{2B} = 1$ and $\Phi_{2A} = 0$, the top voltage doubler operates in the charge phase to recharge C_{P1}, while the bottom doubler operates in the discharge phase to transfer the charge on C_{P2} to the output. Since V_{in} is always connected to one of the pumping capacitors, inrush current is reduced when compared to conventional voltage doublers. Moreover, since both pumping capacitors deliver current to V_{out} alternatively, output switching noise and voltage ripples are also significantly minimized. In addition, as depicted in Fig. 6.25b, a

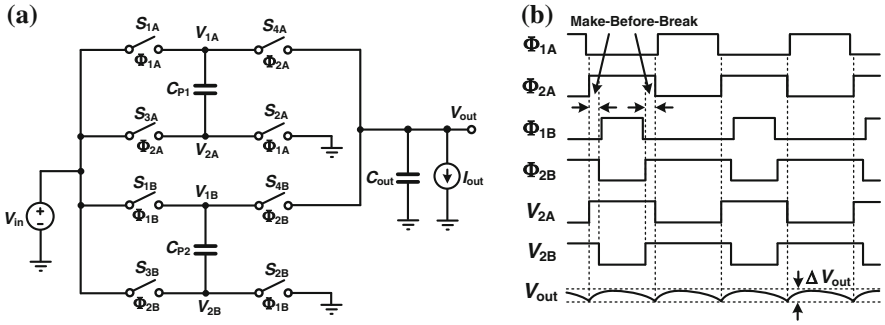


Fig. 6.25 Interleaved SC power converter **a** power stage and **b** timing waveforms

short "make-before-break" overlapping period is inserted between the two discharge phases Φ_{2A} and Φ_{2B} to ensure continuous output current delivery and further reduce ΔV_{out}.

Although the interleaved SC power converter in Fig. 6.25a has been an improvement over conventional SC voltage doublers, severe inrush current and switching noise occur during the phase transitions. In the steady state, during the discharge phase of either pumping capacitor, the parasitic capacitance at nodes V_{2A} and V_{2B} have to be charged and discharged between ground and V_{in} periodically. This causes a large inrush discharge current to flow into V_{out} through the interleaved discharge path. As a result, this induces high *di/dt* switching noise. Meanwhile, the sharp rising/falling edge of the voltages at nodes V_{2A} and V_{2B}, will also be coupled to V_{out} by C_{P1} and C_{P2}. This will be imposed onto the *di/dt* switching noise and cause even larger variations in V_{out}. Furthermore, during the load transient when a sudden load current change occurs, the input current I_{in} is forced to change drastically to accommodate the load current demand. This causes severe switching noise at V_{out}. Similar scenarios also occur during start-up transients, wherein a large inrush current surge will be injected into V_{out}.

To overcome the aforementioned design issues, a hybrid interleaved SC power converter is presented in this case study, which significantly improves both the quality and reliability of on-chip power supplies. Its architecture is illustrated in Fig. 6.26a, from which it can be observed that the structure consists of an interleaved SC voltage doubler and a cascaded linear regulator. Hence, it jointly integrates the advantages of achieving high efficiency and fast transient speeds from the interleaved SC power stage, along with the low output voltage ripple characteristics of a linear regulator. As highlighted in the system architecture, the power converter consists of an on-chip surge suppression feedback loop. It is composed of a linear regulator that is controlled through a feedback controller. The pass transistor of the regulator is implemented using a PMOS transistor M_P, which is cascaded with the interleaved discharge paths. Its gate voltage is continuously adjusted by the feedback controller based on the instantaneous load current. This leads to source-side surge suppression caused by the load fluctuations.

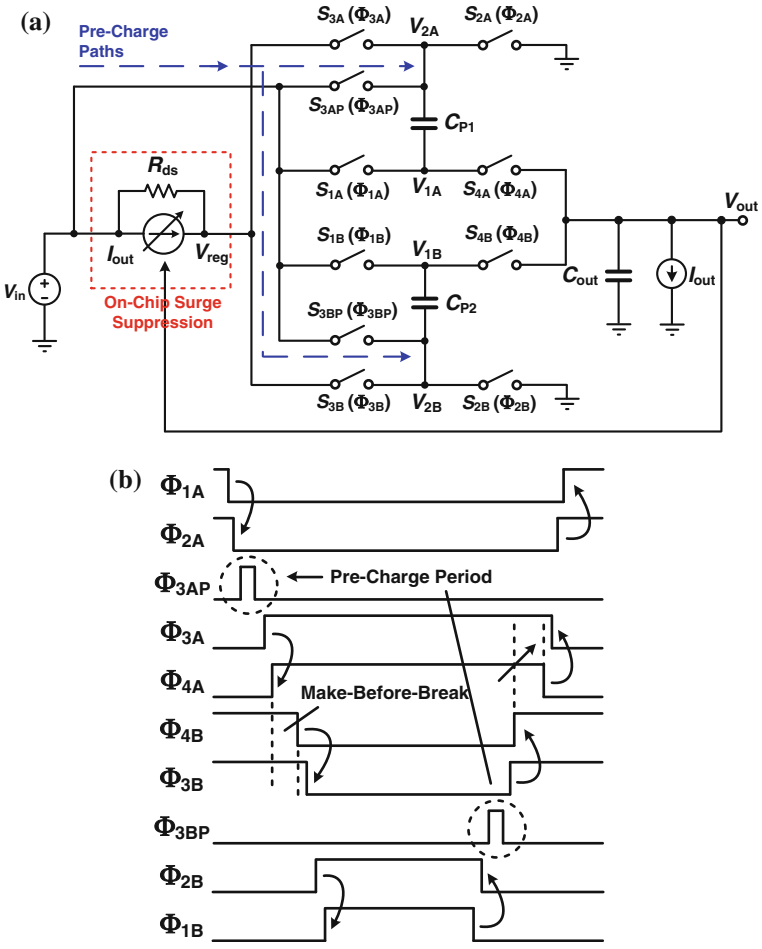


Fig. 6.26 Hybrid interleaving SC power converter **a** system architecture and **b** timing diagram

To get a better understanding on how the effect of input inrush current can be isolated from V_{out}, it was observed that the charge pump in Fig. 6.25a suffers from large *di*/*dt* discharge currents required to charge the parasitic capacitance at nodes V_{2A} and V_{2B}. To overcome this challenge in the hybrid interleaving SC power converter, a PMOS pass device M_p is cascaded at the very front of the current delivery path. This provides an accurate and adaptive control on the discharge current through the feedback control loop. Since M_p operates in the saturation region, sharp changes in the discharge currents are strictly limited to a very low level by the large channel resistance R_{ds}. Moreover, R_{ds} also serves as a strong ringing damper and prevents large oscillations at V_{out}. Furthermore, when the load fluctuates, the discharge current can be adaptively adjusted at the source side promptly, which significantly reduces the large current transient and *di*/*dt* noise caused by large dynamic transients.

Similarly, the proposed technique also applies for inrush current surge suppression during start-up periods to protect the converter from potential over-current damages.

Inrush currents can be further suppressed by employing a pre-charge mechanism. Each voltage doubler employs a pre-charge path between the input and the nodes $V_{2A(2B)}$, in order to charge up the parasitic capacitances. To understand how the pre-charge mechanism can be employed to suppress inrush currents, consider the operation of the charge pump, along with its timing diagram illustrated in Fig. 6.26b. The two voltage doublers in the hybrid interleaved SC converter are operated with the "make-before-break" interleaving mechanism. Hence, each of the 4 power switches and 1 pre-charge switch in one doubler are accurately controlled by a set of phase-delayed clock signals ($\Phi_{1A\sim4A}$ and $\Phi_{1B\sim4B}$). As depicted in the figure, when the top voltage doubler is about to switch to the discharge phase, node V_{2A} is charged up before turning on switch S_{3A}. Hence, a one-shot pre-charge phase $\Phi_{3AP} = 1$ is first triggered, which turns on the pre-charge switch S_{3AP}. As a result, the node V_{2A} is charged from ground to V_{in}. When $\Phi_{3AP} = 0$, S_{3A} is first turned on and after a short phase delay, S_{4A} is turned on in order to start the discharge phase of pumping capacitor C_{P1}. This leads to a very smooth rising-edge transition in V_{2A} and prevents a large inrush current surge from V_{in}. In addition, when the discharge phase ends and V_{2A} needs to be discharged, S_{4A} is turned off earlier than S_{3A}. This protects V_{out} from any noise interference. A similar scheme is also applied to S_{1A} and S_{2A} on the charge path to reduce inrush charge current. Hence, with the joint efforts of the on-chip surge suppression and pre-charge mechanism, the total inrush current and output switching noise can be significantly suppressed.

The circuit implementation of the hybrid SC power converter is illustrated in Fig. 6.27. Based on the voltage applied to each power transistor, $M_{1A,1B}$ and $M_{2A,2B}$ on the charge path are implemented with NMOS transistors, while $M_{3A,3B}$ and $M_{4A,4B}$ on the discharge path are implemented with PMOS transistors. To minimize the total power loss, the size of each power component is carefully designed. In this design, the sizing optimization of all 8 power switches and two pumping capacitors C_{P1} and C_{P2} is conducted using the method presented Sect. 5.3.2, to achieve a minimized total power loss. As depicted in Fig. 6.27, the two pre-charge paths are controlled by two PMOS switches M_{3AP} and M_{3BP}, respectively. Since the pre-charge paths conduct only for a very short period before M_{3A} or M_{3B} is turned on, and do not deliver any power to the load, the sizes of M_{3AP} and M_{3BP} are much smaller than the other power switches.

From the circuit implementation of the hybrid interleaved SC power converter, it can be observed that the nodes V_{1A} and V_{1B} are switched between V_{in} and V_{out} alternatively every half-clock cycle. Hence, the generation of the gate control signals for power switches $M_{1A,1B}$ and $M_{4A,4B}$ can be challenging. To fully turn on the NMOS switches M_{1a} and M_{1B} and to turn off the PMOS switches M_{4A} and M_{4B}, the logic levels of the gate control signals $\Phi_{1A,1B}$ and $\Phi_{4A,4B}$ have to be boosted up. Hence, as illustrated in Fig. 6.27, additional internal charge pump based gate drivers are employed. When clock signals $\Phi_{1A,1B}$ switch from 0 to V_{in}, their corresponding boosted clock signals $\Phi_{1A,CP}$ and $\Phi_{1B,CP}$ switch between 0 and

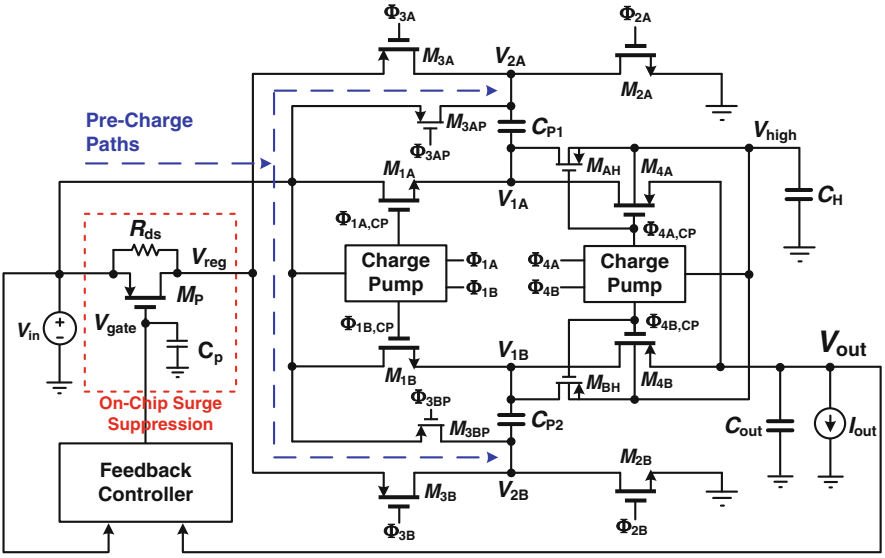


Fig. 6.27 Circuit implementation of the hybrid interleaving SC power converter

$2V_{in}$, thereby ensuring the NMOS switches $M_{1A,1B}$ can effectively turn on. Similarly, the clock signals $\Phi_{4A,CP}$ and $\Phi_{4B,CP}$ switch between 0 and $2V_{in}$, in order to effectively turn off the PMOS $M_{4A,4B}$. Lastly, from Fig. 6.27, it can be observed that in order to provide a sufficient voltage swing in the charge pump gate drive circuitry and to bias the substrates of $M_{4A,4B}$, a separate boosted voltage of V_H is required. Hence, two additional transistors, M_{AH} and M_{BH} are needed to generate this boosted voltage. The size of these transistors is much smaller than the power switches, as they are required only to power the gate drive circuits.

In conclusion, this section presents the design of a hybrid interleaved SC power converter. The hybrid structure comprises of a dual-cell voltage doubler charge pump, along with a linear regulator. By effectively operating the linear regulator through the on-chip surge suppression feedback loop and through the pre-charge mechanism, any inrush currents that would have generated noise on the input and output nodes of the converter are significantly reduced.

6.4 Conclusions

This chapter presents the design of various interleaved SC power converters. In this regulation scheme, the SC power converter employs a cellular architecture, wherein a large power stage is divided into several paralleled cells that are connected between the input and output voltage terminals. By controlling the cells in an interleaving manner, each cell is assigned to process a fraction of the total output power.

Section 6.1 presents the fundamental design concepts and topologies of interleaved SC power converters. The section describes how the interleaving regulation principles, which were initially applied to switch mode power converters, can be extended to charge pumps. This leads to several benefits such as the reduction in the output voltage ripple and input current ripple, along with enhanced transient response.

Section 6.2 then applies the interleaved regulation scheme to reconfigurable SC power converters. A design of a reconfigurable multi-gain step-down SC power converter is presented. By employing two capacitors and nine on-chip power switches, the charge pump is capable of regulating the output voltage at five conversion gains. Moreover, due to the use of an interleaving scheme, the converter has improved dynamic response to provide good line and load regulation. Moreover, its output reference tracking capability makes it a candidate for DVS-based applications.

Section 6.3 introduces several case studies, which presents the design of practical interleaved SC power converters. The first SC power converter discussed is the dual-cell cross-coupled voltage doubler. This converter is regulated using a digital hysteretic control scheme. The second case study analyzes a master-slave interleaving charge pump, designed especially for ultra-low power applications. The charge pump was demonstrated to consist of a master cell, which continuously regulates the output voltage for all loading conditions, while the slave cell was employed during heavy loading scenarios. Moreover, to ensure ultra low power consumption, the entire feedback controller is designed to operate in the subthreshold region, making it quite suitable for ultra-low power microsensor applications. Lastly, the third case study to be presented was the design of a hybrid interleaved SC power converter. The converter employs an interleaved voltage doubler charge pump, along with a linear regulator in order to minimize the effects of inrush currents and switching noise.

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Chapter 7
Switched-Capacitor Power Converter Design and Modeling in z-Domain

In any power converter design, identifying the closed loop transfer function is critical for the overall system design, especially for the system stability. Typically, the power stage transfer function of switch mode and SC power converters are modeled in the z-domain, due to their nonlinear large signal behaviors. Hence, the focus of this chapter involves modeling SC power converters in the z-domain and the corresponding design of control algorithms and feedback controller circuits, to achieve efficient output voltage regulation.

The chapter begins by reviewing fundamental z-domain concepts in charge pump circuits. Following this discussion, the chapter then presents case studies investigating the designs of several SC power converters. The first converter to be discussed is an interleaving cross-coupled voltage doubler, which employs an analog PWM feedback control scheme. By modeling the transfer function of the charge pump in the z-domain, the feedback controller and corresponding compensation circuits can be optimally designed to accurately regulate the output. The second SC power converter is geared specifically for state-of-the-art ultra-low power applications. It is a step-down SC converter that employs a digital PWM control scheme. Lastly, the third case to be investigated is an adaptive step-down converter. It employs the principle of sensor-less line/load monitoring, which is used to implement a very cost-effective dual-loop observation based feedback controller. Each case study will include an in depth discussion, with respect to their system architectures, power stage optimization, control schemes and circuit designs.

7.1 Fundamental z-Domain Principles

This section introduces fundamental z-domain principles required to analyze SC charge pumps. It begins by analyzing the switching action of a single capacitor and deriving its equivalent circuit in the z-domain. Using the equivalent circuit concept, more complex charge pump circuits can be analyzed.

D. Ma and R. Bondade, *Reconfigurable Switched-Capacitor Power Converters*,
DOI: 10.1007/978-1-4614-4187-8_7,

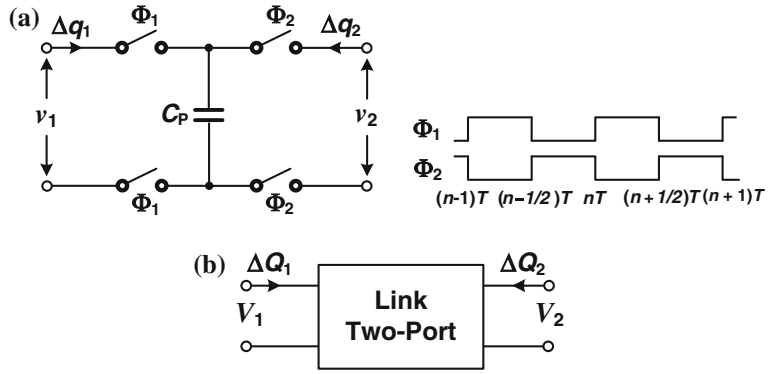

Fig. 7.1 **a** A charge pump circuit, and **b** its link two-port representation

As any charge pump involves an array of one of more switches and capacitors, the first step in understanding their operation using z-domain analysis involves deriving the equivalent circuit of a capacitor in an SC network. To achieve this, Fig. 7.1 illustrates a charge pump consisting of a capacitor C_P that is switched between voltages v_1 and v_2, during the phase $\Phi_1 = 1$ and $\Phi_2 = 1$, respectively.

Let the voltage across the capacitor at time nT, when $\Phi_1 = 1$ be denoted as $v_1(nT)$ and at an immediate previous instant of time when $\Phi_2 = 1$ as $v_2((n - ½)T)$. Then, the charge Δq_1 flowing into C_P at the instant nT can be expressed as

$$\Delta q_1 = C_P\left[v_1(nT) - v_2\left(\left(n - 1/2\right)T\right)\right]. \tag{7.1}$$

Similarly, the charge that flows into the capacitor C_P during the previous half cycle, when $\Phi_2 = 1$ can be written as

$$\Delta q_2 = C_P\left[v_2\left(\left(n - 1/2\right)T\right) - v_1((n-1)T)\right]. \tag{7.2}$$

Equations (7.1) and (7.2) denote the charge–voltage relationship for the capacitor C_P. Moreover, the voltage across C_P during the phase $\Phi_2 = 1$ is delayed by a half-cycle with respect to phase $\Phi_1 = 1$. The behavior of the charge pump in the z-domain can be examined by taking z-transform of Eqs. (7.1) and (7.2) as given by

$$\Delta Q_1(z) = C_P\left[V_1(z) - z^{-1/2} \cdot V_2(z)\right], \tag{7.3a}$$

$$z^{-1/2} \cdot \Delta Q_2(z) = C_P\left[z^{-1/2} \cdot V_2(z) - z^{-1} \cdot V_1(z)\right]. \tag{7.3b}$$

Equations (7.3a) and (7.3b) can be written in matrix form as

$$\begin{bmatrix} \Delta Q_1(z) \\ \Delta Q_2(z) \end{bmatrix} = \begin{bmatrix} C_P & -C_P z^{-1/2} \\ -C_P z^{-1/2} & C_P \end{bmatrix} \begin{bmatrix} V_1(z) \\ V_2(z) \end{bmatrix}. \tag{7.4}$$

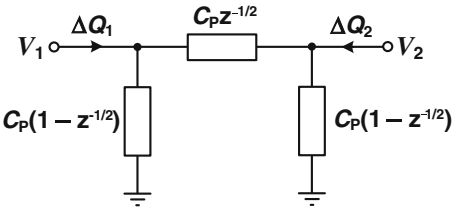

Fig. 7.2 Equivalent z-domain circuit representation

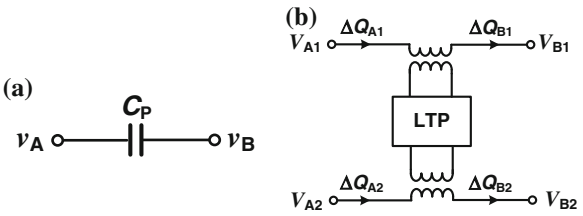

Fig. 7.3 **a** A pumping capacitor connected in series between two voltage nodes, and **b** its equivalent LTP representation

Equation (7.4) represents a two-port equivalent of a capacitor in a charge pump. It is known as a *link two-port* (LTP) representation [1, 2], since it links the voltages across the capacitor C_P and the charges flowing into the capacitor during the two phases. Equations (7.3a) and (7.3b) can also be rearranged to obtain the transmission matrix representation as

$$\begin{bmatrix} V_1(z) \\ \Delta Q_1(z) \end{bmatrix} = \begin{bmatrix} z^{1/2} & \frac{z^{1/2}}{C_P} \\ C_P(1-z^{-1}) \cdot z^{1/2} & z^{1/2} \end{bmatrix} \begin{bmatrix} V_2(z) \\ -\Delta Q_2(z) \end{bmatrix}. \tag{7.5}$$

Equations (7.4) and (7.5) are utilized to characterize the link two-port. The LTP block diagram of any pumping capacitor in a charge pump is illustrated as shown in Fig. 7.1b. It is used to represent the charge flowing into the capacitor to the voltages across it, in two distinct charge and discharge phases. Based on the principle of link two-port, any SC network can be represented using an LTP representation.

While Eq. (7.4) represents the behavior of the pumping capacitor in the z-domain based on a matrix representation, it is possible to represent it using circuit elements. To do so, consider Eq. (7.3a), which can be re-formulated as

$$\begin{aligned} \Delta Q_1(z) &= C_P\left[V_1(z) - z^{-1/2} \cdot V_2(z)\right] \\ &= C_P V_1(z) - z^{-1/2} \cdot C_P V_1(z) + z^{-1/2} \cdot C_P V_1(z) - z^{-1/2} \cdot C_P V_2(z) \\ &= C_P\left(1 - z^{-1/2}\right) V_1(z) + C_P z^{-1/2}[V_1(z) - V_2(z)]. \end{aligned} \tag{7.6}$$

Similarly, Eq. (7.3b) can be re-formulated and expressed as

$$\Delta Q_2(z) = C_P\left(1 - z^{-1/2}\right) V_2(z) + C_P z^{-1/2}[V_2(z) - V_1(z)]. \tag{7.7}$$

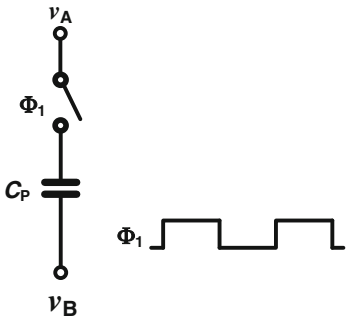

Fig. 7.4 A capacitor and a switch connected in series

Based on Eq. (7.6) and (7.7), the equivalent z-domain circuit of the pumping capacitor can be illustrated as shown in Fig. 7.2. While operating in the charge phase Φ_1, the voltage across C_P is V_1 and the charge transferred is Δq_1. In the discharge phase Φ_2, the total voltage across the capacitor is V_2 and the charge transferred is Δq_2.

As an example, consider a capacitor connected in series between two voltages v_A and v_B, as illustrated in Fig. 7.3a. In this network, in addition to the relationship between the charges flowing into the capacitor and the voltages across it, due to the series connection the charge entering the capacitor at one terminal should be equal to the charge leaving at the other terminal. This can be expressed as

$$\begin{aligned} \Delta Q_{A1} &= \Delta Q_{B1}, \\ \Delta Q_{A2} &= \Delta Q_{B2}. \end{aligned} \tag{7.8}$$

In Eq. (7.8), the first subscript represents the circuit node and the second subscript represents the operation phase. This notation is employed since the LTP representation characterizes the charge–voltage relationship for any capacitor in a charge pump into two phases, the charge and discharge phase. In the example in Fig. 7.3, two separate phases do not exist. However, by representing the charge transfer mechanisms explicitly in two phases, the generic LTP representation can be utilized. Hence, let Φ_1 be the charge phase, with voltages V_{A1} and V_{B1} across the capacitor and Φ_2 be the discharge phase, with voltages V_{A2} and V_{B2} across the capacitor. Then, the LTP representation of the capacitor connected in series with two voltages is illustrated in Fig. 7.3b. Furthermore, it should be noted that the condition in Eq. (7.8) can be satisfied using transformers to couple the voltages across the capacitor in each of the two phases.

While the example discussed in Fig. 7.3 discussed a capacitor connected in series across two voltages, most SC networks employ capacitors in conjunction with switches to control the charge transfer mechanisms. Hence, Fig. 7.4 illustrates a simple system consisting of a capacitor connected in series with a switch. During the phase $\Phi_1 = 1$, the capacitor is charged from voltages v_A and v_B, and it is open during the phase $\Phi_1 = 0$.

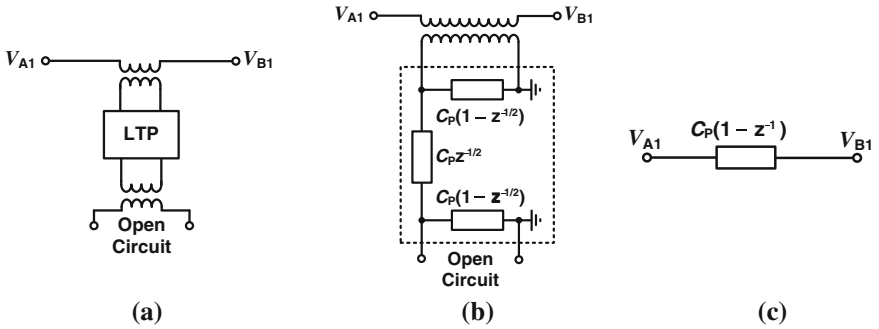

Fig. 7.5 **a** LTP block diagram, **b** z-domain representation and **c** equivalent circuit of a series switch and capacitor network

The equivalent LTP block diagram of the series switch and capacitor system is illustrated in Fig. 7.5a. Similar to Fig. 7.3b, the LTP block diagram represents the voltages across the capacitor C_P during the phase $\Phi_1 = 1$ as V_{A1} and V_{B1}, whereas it is represented through an open circuit during the discharge phase. To obtain the equivalent circuit in the z-domain, as shown in Fig. 7.5b, the LTP block diagram is replaced with the z-domain circuit of a pumping capacitor. Due to the open circuit behavior during the phase $\Phi_1 = 0$, the z-domain equivalent circuit can be simplified as

$$C_P\left(1 - z^{-1/2}\right) + \frac{C_P\left(1 - z^{-1/2}\right) \cdot C_P z^{-1/2}}{C_P(1 - z^{-1/2}) + C_P z^{-1/2}} = C_P\left(1 - z^{-1}\right). \tag{7.9}$$

Thus, from Eq. (7.9), the z-domain equivalent circuit of a series connected switch and capacitor network can be represented as illustrated in Fig. 7.5c.

It is possible to employ the LTP representation of SC networks to obtain the transfer function of charge pumps. Hence, as a final design example, consider the voltage replicator charge pump, which is illustrated in Fig. 7.6. Similar to the z-domain representation in Fig. 7.5, it is possible to obtain an equivalent circuit of the voltage replicator and derive its transfer function. This is illustrated in Fig. 7.7.

Figure 7.7a illustrates the equivalent circuit of the voltage replicator in the z-domain, using the principles of LTP. As discussed before, a LTP system is used to represent the charge–voltage relationship for each capacitor during its charge and discharge phases. Hence, V_{in1} and V_{in2} represent the effective input voltages during the phases $\Phi_1 = 1$ and $\Phi_2 = 1$, respectively. V_{out1} and V_{out2} follow the similar nomenclature. Since switch S_1 is open during phase $\Phi_2 = 1$ and S_2 is open during $\Phi_1 = 1$, the simplified z-domain circuit of the voltage replicator can be obtained as depicted in Fig. 7.7b. Using Fig. 7.7b, it is possible to obtain the transfer functions V_{out1}/V_{in1} and V_{out2}/V_{in1} as

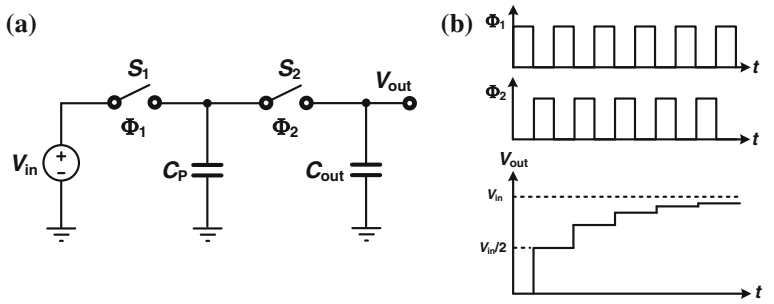

Fig. 7.6 **a** Circuit schematic and **b** output voltage waveforms for a SC voltage replicator

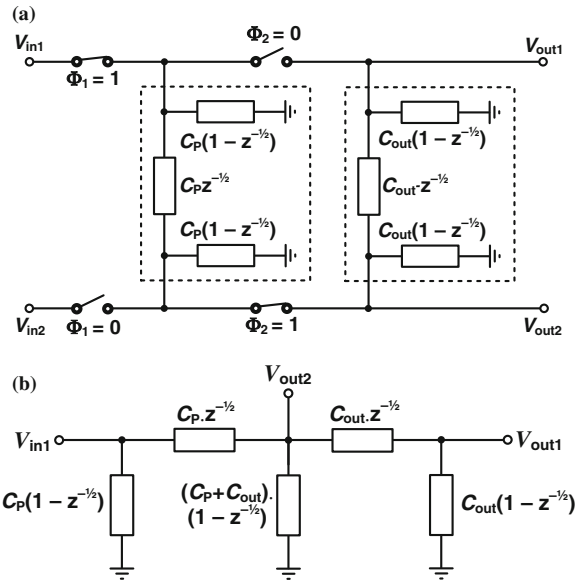

Fig. 7.7 Equivalent z-domain circuits of the voltage replicator charge pump

$$\frac{V_{\text{out1}}}{V_{\text{in1}}} = \frac{C_{\text{P}} z^{-1/2}}{C_{\text{P}} + C_{\text{out}}(1 - z^{-1})}, \qquad \frac{V_{\text{out2}}}{V_{\text{in1}}} = \frac{C_{\text{P}} z^{-1}}{C_{\text{P}} + C_{\text{out}}(1 - z^{-1})}. \tag{7.10}$$

In conclusion, modeling the power stage of a SC converter is quite important for the design of the overall power conversion system. Based on these principles, advanced closed loop controller can be designed, which can be optimized for enhanced performance, efficiency and robustness. Moreover, the principle of linear two-port can be applied to model the transfer function of any of the previously discussed SC power converters. However, each of the converter designs

significantly increases the circuit complexity by employing advanced principles such as interleaving regulation, power stage reconfiguration and so on. As a result, each of the subsequent power converter designs in Sect. 7.2 will be analyzed in the z-domain on an individual case basis. The analysis will be carried out by employing the fundamental capacitor charge–voltage relationships, which form the basis of the LTP representation, discussed in Sect. 7.1.

7.2 Case Studies: Practical SC Power Converters

Following the discussion of the fundamental principles to model the charge pump in the z-domain, this section investigates several cases in practical SC power converter designs. The study will focus on closed loop system designs to improve efficiency and performance. Each of the power converters discussed are designed by considering various application-specific requirements such as efficiency, load power, transient response, form factor, and so on.

7.2.1 Case Study 1: Interleaved Cross-Coupled SC Voltage Doubler Design in z-Domain

The first case study presents the design of an interleaved SC power converter. As discussed in Chap. 6, interleaved power stage topologies can reduce the output voltage ripples and improve the load regulation of power converters. Hence, this section investigates the design of an interleaved cross-coupled voltage doubler in the z-domain. It employs an analog interleaving PWM control scheme to achieve precise closed loop voltage regulation. The section first models the transfer function of the power stage in the z-domain. Following this, the closed loop feedback controller is designed along with its compensation circuitry.

Figure 7.8 illustrates the system architecture of the interleaved SC power converter. The power stage is a cross-coupled voltage doubler that is regulated using an analog PWM controller. Its closed loop operation is as follows. Initially, V_{out} is scaled down with the aid of a resistive voltage divider. This scaled voltage is then compared with the desired reference voltage V_{ref} and the corresponding voltage regulation error is determined and amplified by the error amplifier. The output of the error amplifier is then used to determine the duty ratio of each charge pump sub-cell. To implement this, it can be observed that the error signal is compared with four interleaved ramp signals, which have a phase difference of 90^{o} between each other. The output of each comparator then generates the reset signal for the corresponding RS latches, which determines the duty ratio of each sub-cell.

One of the major challenges in the design of the SC converter is during its start-up transient period. During this period, the output voltage is zero, thereby leading

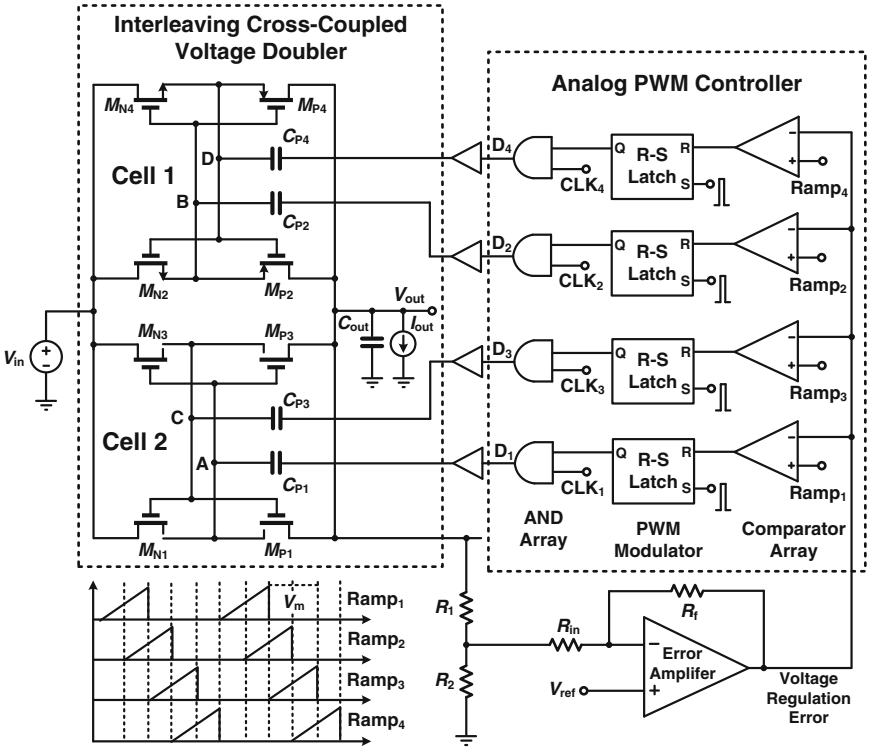

Fig. 7.8 System architecture of the interleaved SC power converter with analog PWM controller

to a large voltage regulation error between V_{out} and V_{ref}. This error is amplified by the error amplifier, thereby causing the duty ratios generated from the RS latches to be very close to 100 %. Hence, all four clock signals would stay high simultaneously, thereby preventing any of the PMOS transistors from being turned on. Thus, none of the pumping capacitors would discharge to the output and V_{out} would continue to stay at zero volts. In order to overcome this problem, the maximum duty ratio of each cell is limited to 50 %. This is achieved through the setup of the digital AND array and the ramp signals.

During steady state, V_{out} is well regulated by the PWM controller. If V_{out} varies such that it becomes slightly higher/lower than the desired level, then the output voltage of the error amplifier will decrease/increase accordingly. This leads to a smaller/larger duty ratio to be generated by the RS latches. Hence, the charge pump at the power stage will deliver less/more current to the output, thereby adjusting V_{out} back to its desired value.

Since the interleaved SC power converter employs an analog PWM control scheme to achieve closed loop regulation, identifying the closed loop transfer function of the overall system becomes critical. Based on the transfer function of the power stage, the compensation network can then be appropriately designed,

in order to achieve stable operation. Typically, the power stage in SC power converters exhibit a nonlinear large signal behavior, thereby making it suitable for z-domain modeling. On the other hand, since the controller is traditionally designed with linear analog circuits, it is commonly modeled in the s-domain. As a result, to model the entire closed loop gain, domain transformation is unavoidable. To achieve this, state space averaging or other averaging modeling techniques have been proposed to approximately model the power stage in the s-domain. However, in the process of averaging, high-frequency poles and zeros of the system are usually missed. To overcome this drawback, a z-domain model for the interleaving cross-coupled charge pump is presented.

To analyze the transfer function of the cross-coupled voltage doubler, Fig. 7.9 illustrates the charge and discharge process of one charge pump cell. The charge pump operates in a full charge mode (FCM). In this mode, the current delivered by the pumping capacitors C_{Pi} at the end of each switching interval drops to a very low level, in comparison to its peak value. Since the two cross-coupled cells do not exchange charge or power at any instant during their operation, they can be modeled as separate elements. To derive the transfer function, first consider the operation of the charge pump when $\Phi_1 = 0$ and $\Phi_3 = 1$, between the time instants of $(n - 1)T_{\mathrm{s}}$ and $(n - 1/2)T_{\mathrm{s}}$. In this time period, C_{P1} is charged to V_{in}, while C_{P3} is discharged until its voltage drops to $V_{\mathrm{out}} - V_{\mathrm{in}}$. Hence, the charge stored in C_{P1}, C_{P3} and C_{out} at the instant $(n - 1)T_{\mathrm{s}}$ is computed as

$$\begin{aligned} Q_1(n-1)T_{\mathrm{s}} &= C_{\mathrm{P}} \cdot V_{\mathrm{in}}(n-1)T_{\mathrm{s}}, \\ Q_3(n-1)T_{\mathrm{s}} &= C_{\mathrm{P}} \cdot (V_{\mathrm{out}}(n-1)T_{\mathrm{s}} - V_{\mathrm{in}}(n-1)T_{\mathrm{s}}), \\ Q_{\mathrm{out}}(n-1)T_{\mathrm{s}} &= C_{\mathrm{out}} \cdot V_{\mathrm{out}}(n-1)T_{\mathrm{s}}. \end{aligned} \tag{7.11}$$

Here, it is assumed that the capacitances of all pumping capacitors are equal to C_{P}. During the next phase, when $\Phi_1 = 1$ and $\Phi_3 = 0$ (between the time instants $(n - 1/2)T_{\mathrm{s}}$ and nT_{s}), C_{P1} is discharged to V_{out} and its voltage drops to $V_{\mathrm{out}} - V_{\mathrm{in}}$. At the same time, C_{P3} is charged from the input to V_{in}. Hence, at the instant of nT_{s}, the charge stored in C_{P1}, C_{P3} and C_{out} are equal to

$$\begin{aligned} Q_1(nT_{\mathrm{s}}) &= C_{\mathrm{P}} \cdot (V_{\mathrm{out}}(nT_{\mathrm{s}}) - V_{\mathrm{in}}(nT_{\mathrm{s}})), \\ Q_3(nT_{\mathrm{s}}) &= C_{\mathrm{P}} \cdot V_{\mathrm{in}}(nT_{\mathrm{s}}), \\ Q_{\mathrm{out}}(nT_{\mathrm{s}}) &= C_{\mathrm{out}} \cdot V_{\mathrm{out}}(nT_{\mathrm{s}}). \end{aligned} \tag{7.12}$$

By comparing the charge equations for the two phases reveals that the charge transferred from C_{P1} to the output load is equal to $Q_1(n - 1)T_{\mathrm{s}} - Q_1(nT_{\mathrm{s}})$. On the other hand, the total charge transferred from C_{P3} to V_{out} is equal to $Q_3(nT_{\mathrm{s}}) - Q_3(n - 1)T_{\mathrm{s}}$. Lastly, the charge transferred from C_{out} to the output load from the time $(n - 1)T_{\mathrm{s}}$ to nT_{s} is given as $Q_{\mathrm{out}}(n - 1)T_{\mathrm{s}} - Q_{\mathrm{out}}(nT_{\mathrm{s}})$.

Since all pumping capacitors are assumed to be equal, each cell transfers the same amount of charge in a switching cycle. Thus, the total charge transferred from the pumping capacitors to the output load is doubled. According to the charge conservation theorem, when the charge pump reaches its steady state, the total

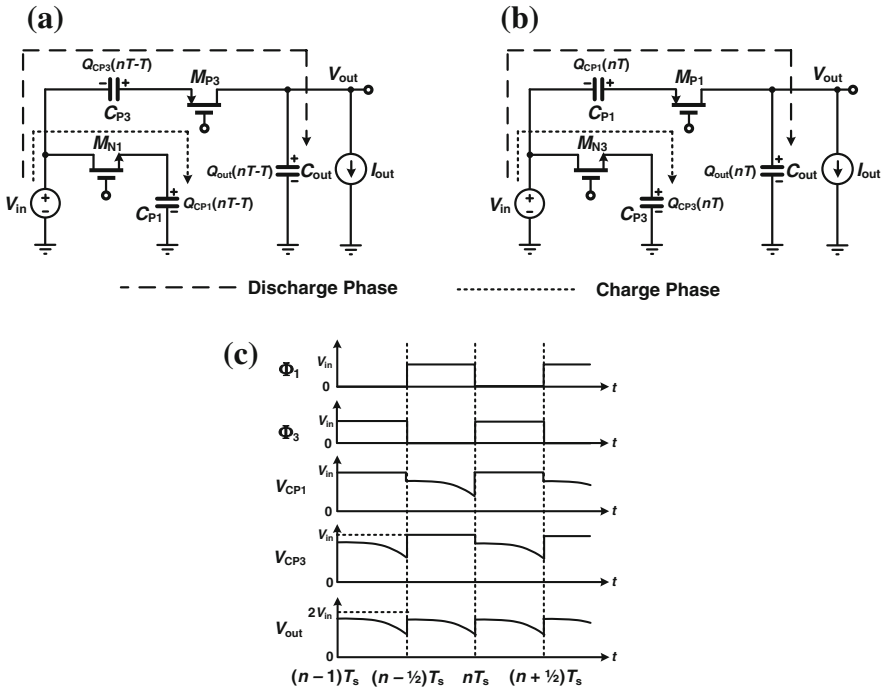

Fig. 7.9 Charge and discharge phases for the interleaving SC power converter when **a** $\Phi_3 = 1$, **b** $\Phi_1 = 1$ and **c** corresponding timing diagram

charge transferred to the output load should be equal to the charge consumed in the output load resistor. This can be expressed as

$$2[Q_1(n-1)T_s - Q_1(nT_s) + Q_3(nT_s) - Q_3(n-1)T_s] + [Q_{out}(n-1)T_s - Q_{out}(nT_s)] = \frac{T_s}{2}\left[\frac{V_{out}(n-1)T_s}{R_{out}} + \frac{V_{out}(nT_s)}{R_{out}}\right]. \tag{7.13}$$

This can be simplified to

$$2C_P[2V_{in}(n-1)T_s + 2V_{in}(nT_s) - V_{out}(nT_s) - V_{out}(n-1)T_s] + C_{out}[V_{out}(n-1)T_s - V_{out}(nT_s)] = \frac{T_s}{2}\left[\frac{V_{out}(n-1)T_s}{R_{out}} + \frac{V_{out}(nT_s)}{R_{out}}\right]. \tag{7.14}$$

Applying z-domain transform to the Eq. (7.14) gives

$$2C_P\left[2V_{in}\left(z^{-1}+1\right) - V_{out}\left(z^{-1}+1\right)\right] + C_{out}V_{out}\left(z^{-1}-1\right) = \frac{T_s}{2}\frac{V_{out}}{R_{out}}\left(z^{-1}+1\right) \tag{7.15}$$

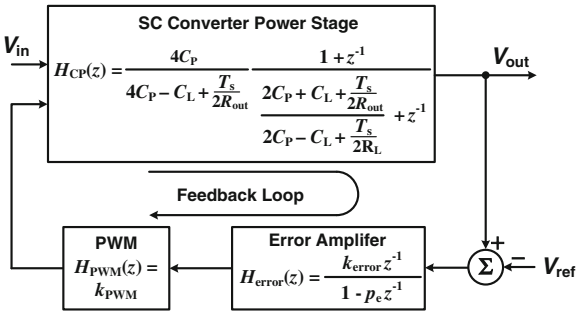

Fig. 7.10 z-domain closed loop control block diagram of the interleaving SC power conversion system

Thus, V_{out} can be expressed as

$$V_{out} = \frac{4C_P(1 + z^{-1})V_{in}}{\left(2C_P - C_{out} + \frac{T_s}{2R_{out}}\right)\left(\frac{2C_P + C_{out} + \frac{T_s}{2R_{out}}}{2C_P - C_{out} + \frac{T_s}{2R_{out}}} + z^{-1}\right)}. \tag{7.16}$$

The transfer function of the power stage can be written as

$$\begin{aligned} H_{CP}(z) &= \frac{V_{out}}{V_{in}} = \frac{a(1 + z^{-1})}{b + z^{-1}}, \\ \text{where } a &= \frac{4C_P}{\left(2C_P - C_{out} + \frac{T_s}{2R_{out}}\right)}, \\ \text{and } b &= \frac{2C_P + C_{out} + \frac{T_s}{2R_{out}}}{2C_P - C_{out} + \frac{T}{2R_{out}}}. \end{aligned} \tag{7.17}$$

The only pole in the system is located at $z = -1/b < 1$. For the ideal case, when the switching frequency is infinity and $z = 1$, the transfer function becomes

$$\left.\frac{V_{out}}{V_{in}}\right|_{z=1, T_s=0} = \frac{2a}{b + 1} = 2. \tag{7.18}$$

This is consistent with the DC conversion gain of an ideal voltage doubler.

Figure 7.10 shows the control block diagram of the SC power converter in the z-domain. The closed loop modeling is based on the analog PWM controller. As illustrated in Fig. 7.8, the feedback controller accomplishes three major functions: error detection, resolution enhancement and PWM modulation. The error amplifier detects the regulation error between V_{out} and V_{ref}. It also provides a proportional control that enhances the signal processing resolution and improves the regulation accuracy. In this design, a dominant pole in the amplifier p_e has to be designed such that $p_e < 1$, in the z-domain. Thus, the error amplifier can be modeled as

$$H_{error}(z) = \frac{k_{error} z^{-1}}{1 - p_e z^{-1}}. \tag{7.19}$$

The second major part of the feedback controller is the PWM modulator. The PWM modulator imposes the computed error onto a reference clock signal and thus generates the instantaneous duty ratio. In the z-domain, this is modeled as

$$H_{\mathrm{PWM}}(z) = k_{\mathrm{PWM}}. \tag{7.20}$$

By combining Eqs. (7.17), (7.19) and (7.20), the loop gain for the entire system is obtained as

$$\begin{aligned} T(z) =& H_{\mathrm{CP}}(z) \cdot H_{\mathrm{error}}(z) \cdot H_{\mathrm{PWM}}(z) \\ =& \frac{4ak_{\mathrm{PWM}}k_{\mathrm{error}}z^{-1}(1+z^{-1})}{(1-p_{\mathrm{e}}z^{-1})(b+z^{-1})}. \end{aligned} \tag{7.21}$$

From Eq. (7.21), it can be observed that the pole from the charge pump power stage is located at $z = -1/b < 1$. If the pole from the error amplifier p_{e} is designed to lie within the unit circle, then the system is naturally stable and an additional compensation network is not required.

In conclusion, this case study presents the design of an interleaved cross-coupled SC voltage doubler, which is regulated using an analog PWM control scheme. The accurate design of the closed loop system entails modeling both the power stage and the feedback controller. However, due to its non-linear switching behavior, the power stage is typically modeled in the z-domain, while the feedback controller is modeled in the s-domain due to the use of linear analog components. To avoid cross-domain conversion, this section jointly models both the charge pump and the feedback controller in the z-domain. By employing an interleaving power stage topology, it provides a very cost-effective design with low noise performance and fast transient response for high-performance integrated systems.

7.2.2 *Case Study 2: Monolithic SC Power Converter for Ultra-Low Power Applications*

This section investigates the design of an ultra-low power, monolithic SC power converter for emerging self-powered applications. The major design thrust for this converter is to implement a monolithic power supply at very low power levels, which is capable of operating over a widely varying input and output voltage range. These requirements impose unprecedented challenges on power regulation systems and entails a detailed design approach at all levels, from system architecture, control techniques to circuit implementation [3].

For the power stage design, most SC power converters such as voltage doublers achieve step-up voltage conversion. However, for many DVS-based applications, a step-down topology is necessary. Unfortunately, step-down SC converters are not as common and typically suffer from low efficiencies. Secondly, to achieve multiple CGs, SC power converters require many off-chip pumping capacitors, on-chip

pads and IC pins. This significantly increases the system volume, which is undesirable for monolithic implementations.

For the design of the controller, due to large variations from renewable energy sources, an open-loop charge pump design does not suffice. Thus, to facilitate accurate regulation and achieve high efficiency, the converter must employ a feedback and/or a feed-forward controller. In addition, its output voltage is highly preferred to be variable for DVS operations. While sophisticated feedback control techniques exist in traditional designs, the implementation of a controller that operates at microwatt power levels is significantly more challenging. Therefore, based on these challenges, this section presents a SC power supply for emerging low-power applications. It features an efficient step-down charge pump and a subthreshold-region DPWM digital feedback controller. To enhance the efficiency, the switching frequency of the converter is programmable based on the instantaneous loading conditions. In contrast to traditional pulse-frequency modulation (PFM) control, which exhibits a random noise spectrum, the switching noise spectrum in this design remains discrete and predictable. The section also discusses the system architecture, circuit implementation, along with a design strategy and optimization technique to implement an efficient power converter.

Figure 7.11 illustrates the system architecture and the timing diagram of the step-down SC power converter with sub-threshold DPWM feedback controller. With reference to the timing diagram in Fig. 7.11b, the charge pump is operated in two complementary phases–the charge phase when $\Phi_1 = 1$ and $\Phi_2 = 0$, and the discharge phase when $\Phi_2 = 1$ and $\Phi_1 = 0$. In the charge phase, the PMOS power switches M_{P1}, M_{P2}, M_{P3} and M_{P4} are turned on by the gate control signals Φ_C and $\Phi_{P,}$ which are generated by the non-overlapping gate drive buffers. This action creates two charge paths to charge the pumping capacitors C_{P1} and C_{P2}. From Fig. 7.11a, it can be observed that the pumping capacitors are connected in parallel between the input power supply and the output nodes. As a result, C_{P1} and C_{P2} are charged to a voltage $V_{in} - V_{out}$.

During the discharge phase, the switches M_{P1}, M_{P2}, M_{P3} and M_{P4} are turned off, while the NMOS switches M_{N6} and M_{N7} and the PMOS switch M_{P5} are turned on by the gate control signals Φ_N and Φ_P. Accordingly, a discharge path is formed and the two pumping capacitors are connected in series across C_{out}. The load is isolated from the input power supply V_{in}, and is powered solely by C_{P1} and C_{P2}. Note that if C_{P1} and C_{P2} are identical, the voltage across each of the capacitors will be equal to $V_{out}/2$ at the end of the discharge phase. When the charge pump reaches the steady state, if $C_{P1} = C_{P2} = C_P$, V_{out} is equal to

$$V_{out} = \frac{2V_{in}}{3 + \frac{T_s}{R_{out}C_P}}. \tag{7.22}$$

In Eq. (7.22), if $T_s/R_{out}C_P << 3$, $V_{out} = 2/3V_{in}$. Hence, a 2-to-3 step-down voltage conversion is obtained.

The optimization of the step-down charge pump is paramount, especially at ultra low power levels. Power loss components that are typically ignorable have to

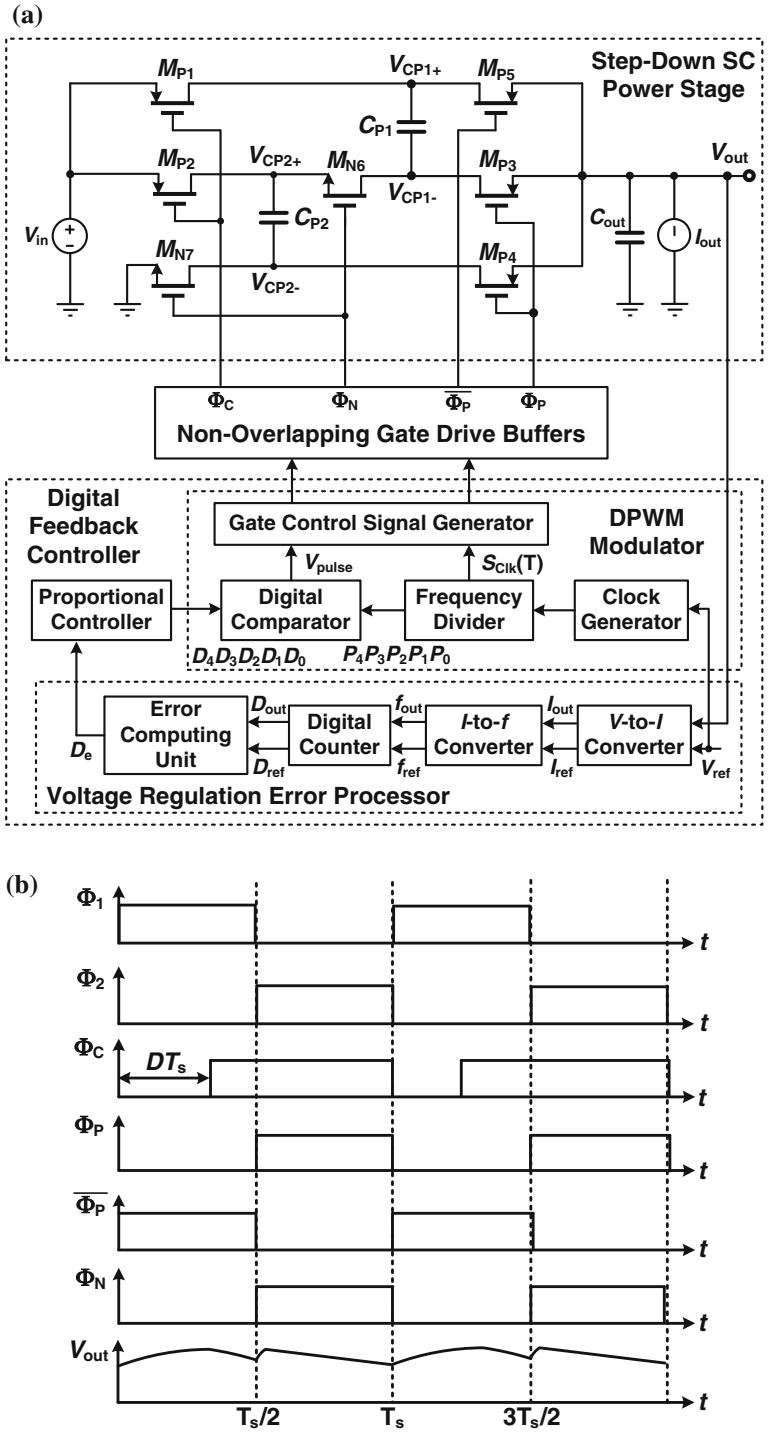

Fig. 7.11 **a** System architecture and **b** timing diagram of the step-down SC power converter with DPWM control

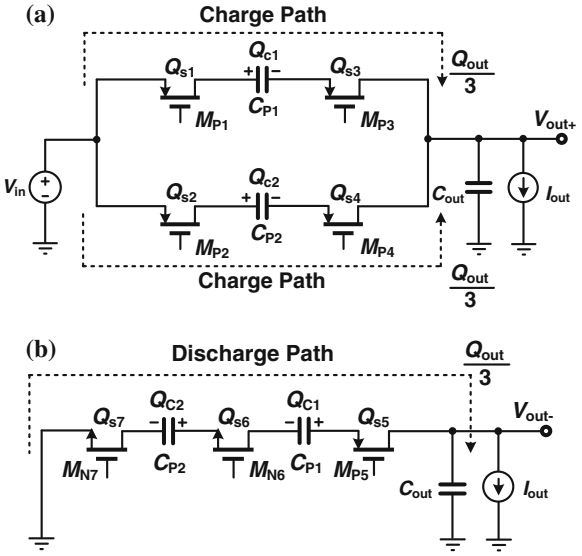

Fig. 7.12 Equivalent charge pump circuit in **a** the charge phase and **b** the discharge phase

be considered, in order to improve the efficiency of the converter. This can be achieved by studying the charge flows illustrated in Fig. 7.12.

For a SC power converter, the power loss in the charge pump usually dominates the total power loss of the entire system and has to be minimized to achieve high efficiency. As discussed in Chap. 4, the power loss in the charge pump is mainly comprised of the conduction loss and switching loss of the power transistors, the conduction loss due to the ESR of the pumping capacitors and the charge redistribution loss. To design the power stage, as discussed in Sect. 5.3.2, the minimum channel length allowed by the process technology, $L_{\min}$ is typically employed. Moreover, for simplicity all the power transistors are sized so that their turn-on resistances are equal. Note that due to the difference of the overdrive voltages, the optimized width of each transistor may not be the same, as shown in Table 7.1. W_{opt} represents the normalized width for the power transistors and the terms k_μ and k_R are defined as $k_\mu = \mu_p/\mu_n$ and $k_R = L_{\min}/(\mu_p C_{ox} W_{opt})$. In order to maximize the efficiency, the optimized width of the power transistor, W_{opt}, should meet the criteria, $\partial P_{L,tot}/\partial W = 0$, where $P_{L,tot}$ is the total power dissipated in the charge pump. Once W_{opt} is determined, the sizes of all the power transistors are uniquely defined by Table 7.1. With a similar technique, the optimal switching frequency f_s of the converter can be determined by solving $\partial P_{L,tot}/\partial f_s = 0$.

A closer look at the power stage operation indicates that in order to vary V_{out}, the related RC charge time in the charge path (for example, the path consisting of M_{P1}, C_{P1} and M_{P3} in Fig. 7.12a) should not deviate significantly from $T_s/2$. If the charge time is too short and the required output voltage needs to be lower than $2V_{in}/3$, the turn-on time of M_{P1} and M_{P2} (DT_s) will be even shorter. This implies that the entire closed loop system should be capable of responding very quickly

Table 7.1 Optimization power transistor parameters

Power transistor	Overdrive voltage	Width	Length	Turn-on resistance
M_1	$V_{in} - \lvert V_{THp}\rvert$	W_{opt}	L_{min}	$k_R/(V_{in} - \lvert V_{THp}\rvert)$
M_2	$V_{in} - \lvert V_{THp}\rvert$	W_{opt}	L_{min}	$k_R/(V_{in} - \lvert V_{THp}\rvert)$
M_3	$V_{in} - \lvert V_{THp}\rvert$	$2W_{opt}$	L_{min}	$k_R/2(V_{out} - \lvert V_{THp}\rvert)$
M_4	$V_{in} - \lvert V_{THp}\rvert$	$2W_{opt}$	L_{min}	$k_R/2(V_{out} - \lvert V_{THp}\rvert)$
M_5	$V_{in} - \lvert V_{THp}\rvert$	$2W_{opt}$	L_{min}	$k_R/2(V_{out} - \lvert V_{THp}\rvert)$
M_6	$V_{in} - V_{out}/2 - V_{THn}$	$2\ k_\mu W_{opt}$	L_{min}	$k_R/2(V_{in} - V_{out}/2 - \lvert V_{THp}\rvert)$
M_7	$V_{in} - V_{THn}$	$k_\mu W_{opt}$	L_{min}	$k_R/(V_{in} - V_{THn})$

and would require very high speed circuits. On the other hand, if DT_s is longer than the charge time, the capacitors C_{P1} and C_{P2} would be fully charged, thereby always maintaining V_{out} at $2V_{in}/3$. Furthermore, if the charge time is longer than $T_s/2$, the voltage levels near the upper limit of $2V_{in}/3$ would be unachievable. As a result, this places new design constraints on proper transistor sizing, selection of the pumping capacitors and the switching frequency f_s.

According to Fig. 7.12a, if KVL is applied to the charge path of the charge pump, then

$$C_{P1}\frac{d}{dt}(V_{CP1}(t)) \cdot (R_{on1} + R_{on3}) + V_{CP1}(t) = V_{in} - V_{out}, \tag{7.23}$$

where the $V_{CP1}(t)$ is the voltage across the capacitor C_{P1}, R_{on1} and R_{on3} are the turn-on resistances of power transistors M_{P1} and M_{P3}. Solving Eq. (7.23), $V_{CP1}(t)$ is obtained as

$$V_{CP1}(t) = (V_{in} - V_{out})\left[1 - e^{-\frac{t}{(R_{on1}+R_{on3})C_{P1}}}\right] = (V_{in} - V_{out})\left(1 - e^{-\frac{t}{\tau_c}}\right), \tag{7.24}$$

where the time constant τ_c can be defined as

$$\tau_c = (R_{on1} + R_{on2}) \cdot C_{P1} = \frac{2C_{P1}L_{min}}{\mu_P C_{ox} W_{opt}\left(V_{in} - \left|V_{THp}\right|\right)}. \tag{7.25}$$

Based on the charge requirements discussed above, in this charge pump τ_c is designed to satisfy the condition

$$\frac{T_s}{10} \le 3\tau_c \le \frac{T_s}{2}. \tag{7.26}$$

Since it takes the charge pump three time constants to reach 95 % of the fully charged voltage value, the period $3\tau_C$ is employed in Eq. (7.26) to define the duty ratio boundaries. Accordingly

$$\frac{1}{30\tau_c} \le f_s \le \frac{1}{6\tau_c}, \tag{7.27}$$

$$\frac{12 f_s C_P L_{min}}{\mu_P C_{ox}\left(V_{in} - \left|V_{THp}\right|\right)} \leq W_{opt} \leq \frac{48 f_s C_P L_{min}}{\mu_P C_{ox}\left(V_{in} - \left|V_{THp}\right|\right)}. \tag{7.28}$$

Hence, Eqs. (7.27) and (7.28) offer another design guideline in identifying the optimal values for W_p and f_s.

To determine the size of the pumping capacitors, from the charge flows depicted in the Fig. 7.12, the total net charge on the pumping capacitors C_{P1} and C_{P2} should be equal to the net charge in the load capacitor C_{out}, leading to

$$2C_P\left[(V_{in} - V_{out}) - \frac{V_{out}}{2}\right] = C_{out}\Delta V_{out}. \tag{7.29}$$

ΔV_{out} is the output ripple voltage and is defined as

$$\Delta V_{out} = V_{out+} - V_{out-}. \tag{7.30}$$

V_{out+} and V_{out-} are the output voltages during the charge and discharge phases, respectively. The total energy transferred by the pumping capacitors to C_{out} in each switching cycle is then given as

$$E_{transfer} = \frac{1}{2} C_{out}\left(V_{out+}^2 - V_{out-}^2\right). \tag{7.31}$$

If $\Delta V_{out} << V_{out}$, then $(V_{out+} + V_{out-}) \approx 2V_{out}$, Eq. (7.31) transforms to

$$E_{transfer} \approx C_{out} V_{out} \Delta V_{out}. \tag{7.32}$$

In a switching cycle, the energy consumed by the load is

$$E_{out} = \frac{V_{out}^2}{R_{out} f_s}. \tag{7.33}$$

In the steady state, the energy transferred from the two pumping capacitors to C_{out} should be equal to the energy consumed by the load. Hence, by equating Eqs. (7.32) and (7.33), the value of C_P can be obtained as

$$C_P = \frac{V_{out}}{(2V_{in} - 3V_{out}) \cdot R_{out} f_s}. \tag{7.34}$$

Similarly, the load capacitor can be determined as

$$C_{out} = \frac{V_{out}}{\Delta V_{out} R_{out} f_s}. \tag{7.35}$$

Note that although the power transistors and capacitors are optimized separately, they are correlated in determining the charge and discharge time constants.

As illustrated in Fig. 7.11, the SC power converter operates as a closed loop system. This guarantees that the duty ratio of the clock signal is tuned to accurately regulate the output voltage during load variations and due to the presence of

parasitic components. Moreover, a variable output power supply is highly desirable, especially for DVS-enabled low power VLSI systems. To facilitate a variable V_{out}, the duty ratio of the power switches is modulated, so that the amount of charge flow can be adaptively controlled to obtain the preferred output voltage level. Accordingly, a digital pulse width modulation (DPWM) control technique is employed to modulate the duty ratios of the power transistors M_{P1} and M_{P2}. This is illustrated in Fig. 7.11b, where the gate control signal Φ_c is modulated and remains high for a time period of DT_s in the charge phase Φ_1, while the other control signals remain unchanged. However, before the controller design can be studied, it is necessary to develop the transfer function of the power stage. With the aid of the transfer function, critical controller circuits such as the compensation network can then be designed.

To obtain the transfer function in the z–domain, first consider the charge phase, as illustrated in Fig. 7.12a. During the charge phase Φ_1, the voltage across each pumping capacitor is equal to $V_{in} - V_{out}$ and the voltage across the output capacitor C_{out} is equal to V_{out}. Hence, the total charge stored in the charge pump during Φ_1 at the instant of $(n-1)T_s$ is given by

$$Q(n-1)T_s = 2C_P[V_{in}(n-1)T_s - V_{out}(n-1)T_s] + C_{out}V_{out}(n-1)T_s. \quad (7.36)$$

Similarly, during the discharge phase Φ_2, the total charge stored in the charge pump is

$$Q(nT_s) = 2C_P\left(\frac{1}{2}V_{out}(nT_s)\right) + C_{out}V_{out}(nT_s). \quad (7.37)$$

From the charge conservation theorem, when the charge pump reaches its steady state, the total net charge on the pumping capacitors C_{P1} and C_{P2} should be equal to the charge consumed by the load R_{out}. This can be expressed as

$$Q(nT_s - T_s) - Q(nT_s) = \frac{T_s}{2}\left[\frac{V_{out}(nT_s - T_s)}{R_{out}} + \frac{V_{out}(nT_s)}{R_{out}}\right]. \quad (7.38)$$

Substituting Eqs. (7.36) and (7.37), Eq. (7.38) transforms to

$$2C_P[V_{in}(n-1)T_s - V_{out}(n-1)T_s] + C_{out}V_{out}(n-1)T_s - (C_P + C_{out})V_{out}(nT_s) = \frac{T_s}{2}\left[\frac{V_{out}(n-1)T_s}{R_{out}} + \frac{V_{out}(nT_s)}{R_{out}}\right]. \quad (7.39)$$

Applying z-domain transform to Eq. (7.39) gives

$$2C_P(V_{in} - V_{out})z^{-1} + C_{out}V_{out}z^{-1} - (C_P + C_{out})V_{out} = \frac{T_s}{2R_{out}}V_{out}\left(z^{-1} + 1\right). \quad (7.40)$$

Therefore, V_{out} can be denoted as

$$V_{out} = \frac{2C_P V_{in} z^{-1}}{\left(C_P + C_{out} + \frac{T_s}{2R_{out}}\right) - \left(C_{out} - 2C_P - \frac{T_s}{2R_{out}}\right) z^{-1}}. \tag{7.41}$$

The power stage transfer function can thus be represented as

$$H_{CP}(z) = \frac{V_{out}}{V_{in}} = \frac{az^{-1}}{1 - bz^{-1}} = \frac{a}{z - b}, \tag{7.42}$$

where, $a = \frac{2C_P}{C_P + C_{out} + \frac{T_s}{2R_{out}}}$ and $b = \frac{C_{out} - 2C_P - \frac{T_s}{2R_{out}}}{C_P + C_{out} + \frac{T_s}{2R_{out}}}$.

From Eq. (7.42), it can be seen that the power stage has one single pole in its transfer function. As long as a second low frequency pole is not introduced by the controller design, the power converter is stable and does not require additional compensation. This leaves large design margins for regulation accuracy enhancement and low power design. To verify the validity of this derivation, when the switching frequency in increased to infinity, the CG in the transfer function is

$$\frac{V_{out}}{V_{in}} = \frac{a}{z - b}\bigg|_{z=1, T_s=0} = \frac{2C_P/C_P + C_{out}}{1 - C_{out} - 2C_P/C_P + C_{out}} = \frac{2}{3}, \tag{7.43}$$

which is consistent with the result previously derived.

The z-domain model for the SC power converter can also be derived for the closed loop DPWM feedback controller. Its corresponding system flow chart and block diagram are illustrated in Fig. 7.13. The controller fulfills three major functions, error processing, error amplification with a proportional control and DPWM duty ratio determination. As illustrated in Fig. 7.13a, the voltage regulation error between V_{out} and V_{ref} is determined by the error processor by converting the voltages into corresponding currents signals. These currents are transferred into the frequency domain, based on which the error is finally represented as digital value. The computed error can be modeled as

$$D_e(z) = k_{RO} g_m T_s V_e(z), \tag{7.44}$$

where k_{RO} represents the current-to-frequency gain of the ring oscillator, g_m is the transconductance of the voltage-to-current converter and $V_e(z) = V_{out}(z) - V_{ref}(z)$.The transfer function for the error processor can then be modeled as

$$H_{EP}(z) = k_{RO} g_m T_s. \tag{7.45}$$

To enhance the processing resolution and improve the regulation accuracy, a proportional controller is included in the feedback loop. As illustrated in Fig. 7.13a, this process amplifies the error signals from $n + 1$ bits to $n + k + 1$ bits. It is modeled as

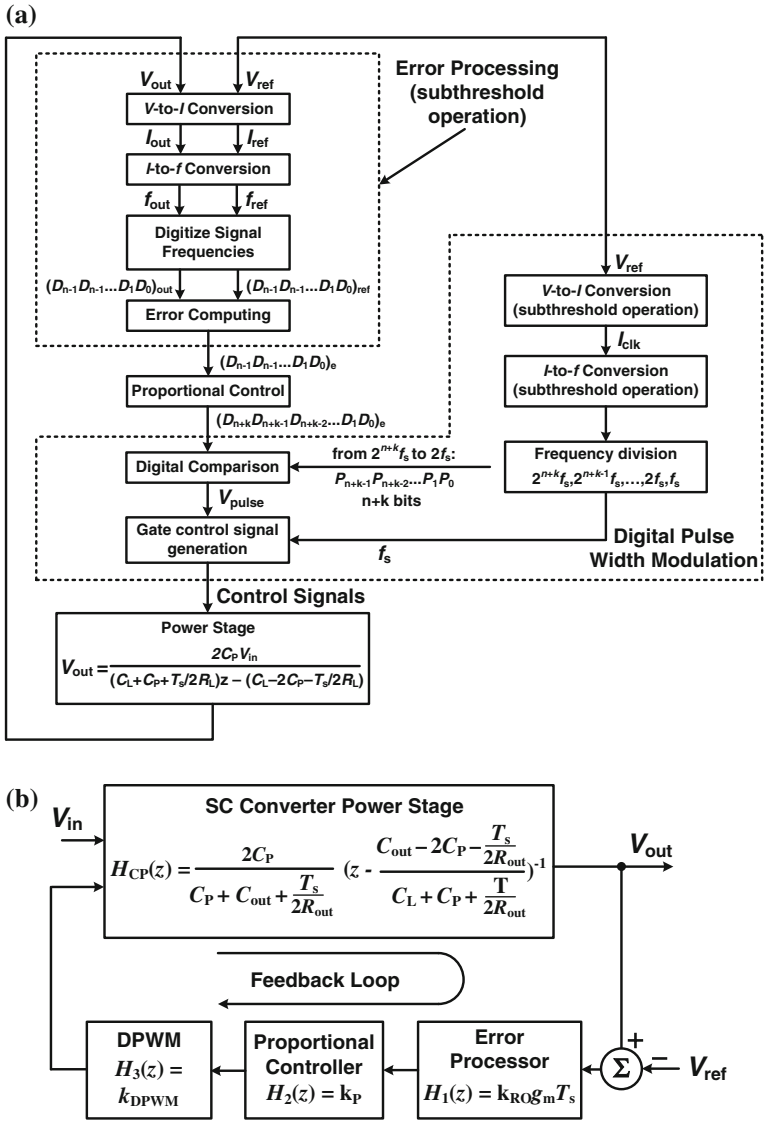

Fig. 7.13 **a** System control flow chart and **b** z-domain control block diagram

$$H_{\mathrm{PC}}(z) = k_{\mathrm{P}}. \tag{7.46}$$

Another major part of the feedback controller is the digital pulse width modulator. This block is responsible for modulating the pulse width of the gate control signals, based on the instantaneous error signals. To maintain a high signal processing resolution ($n + k + 1$ bits), when V_{ref} is converted into its corresponding digital signal, it is also amplified to $n + k + 1$ bits. Hence, the DPWM can be modeled as

$$H_{\mathrm{DPWM}}(z) = k_{\mathrm{DPWM}}. \tag{7.47}$$

As illustrated in Fig. 7.13b, the closed loop gain of the entire system, after combining the feedback controller with the power stage is obtained as

$$\begin{aligned} T(z) =& H_{\mathrm{DPWM}}(z) \cdot H_{\mathrm{PC}}(z) \cdot H_{\mathrm{EP}}(z) \cdot H_{\mathrm{CP}}(z) \\ =& k_{\mathrm{DPWM}} k_{\mathrm{P}} k_{\mathrm{RO}} g_{\mathrm{m}} T \frac{a}{z-b}. \end{aligned} \tag{7.48}$$

Another important feature of the DPWM controller is its capability to adjust the switching frequency of the power converter, with respect to the instantaneous loading condition. When the converter has to deliver large power or generate a high output voltage, a higher switching frequency is employed to ensure fast transient response and low output voltage ripple. However, when the load becomes very light, the switching frequency is reduced to minimize the switching loss and obtain high efficiency. It should be noted that although the switching frequency is variable, this operation scheme is different from PFM which has a random, unpredictable switching noise spectrum and is thus not preferred in many noise-sensitive applications. Instead, in this design, the switching frequency is varied at multiples of the fundamental frequency. Hence, the switching noise spectrum remains discrete and predictable.

In conclusion, this section studies a new monolithic step-down SC power converter design. With the subthreshold controller and frequency programmable DPWM regulation scheme, the power consumption and signal processing speed are adaptively optimized. The fully on-chip implementation significantly reduces system volume and switching noises. The number of I/O pins and on-chip bonding pads as well as parasitic components is significantly reduced. Thus, this design provides an effective solution for new generation, monolithic power supplies for self-powered devices.

7.2.3 *Case Study 3: Adaptive Step-down SC Power Converter with Observation-Based Line-Load Regulation Control*

While the first type of SC power converter discussed was specifically designed for ultra-low power, monolithic implementations, this case study presents an adaptive step-down SC power converter with features such as superior line and load regulation and DVS capability [4]. The power converter employs the concept of the dual-loop, observation-based (OB) line and load sensing to provide robust line regulation for an unstable input power source and tight load regulation on output ripple and transient dynamics. Moreover, in contrast to conventional designs, the OB controller avoids the use of additional sensing circuits, thereby saving on power and silicon area of the overall system. Instead, the OB controller relies on purely switched-capacitors circuits, to form a consistent z-domain circuit environment in

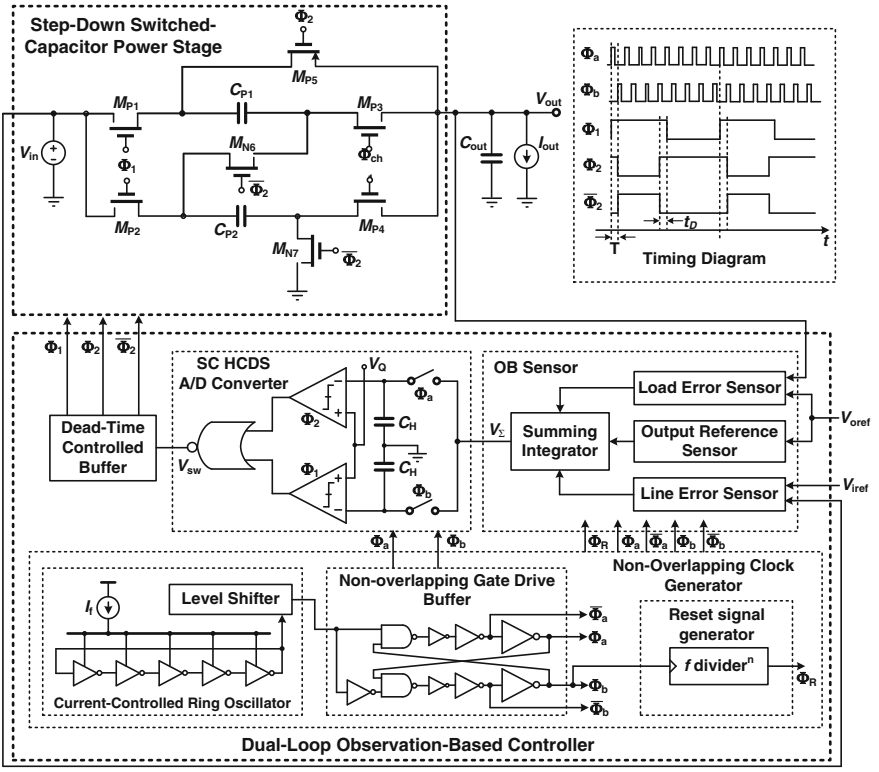

Fig. 7.14 System block diagram

the entire closed loop. This further simplifies the accurate system modeling, by preventing the need for cross-domain conversion. Thus, this section discusses the complete system architecture, z–domain modeling, control algorithms and circuit implementations of the adaptive step-down SC power converter.

7.2.3.1 Charge Pump Modeling and Design

Figure 7.14 illustrates the system architecture and timing diagram of the SC power converter. It consists of the step-down SC power stage, an OB line/load sensor, a half-clock double-sampled (HCDS) SC A/D converter, a dead-time controlled buffer and a non-overlapping clock generator. The power stage achieves a 2/3 step-down voltage conversion.

In the OB controller, a cost-effective SC sensing device is employed to sense variations in the input source V_{in}, the regulated output V_{out} and their corresponding reference voltages, V_{iref} and V_{oref}, simultaneously. This combined design has notable advantages over other conventional multi-loop regulation schemes. Firstly,

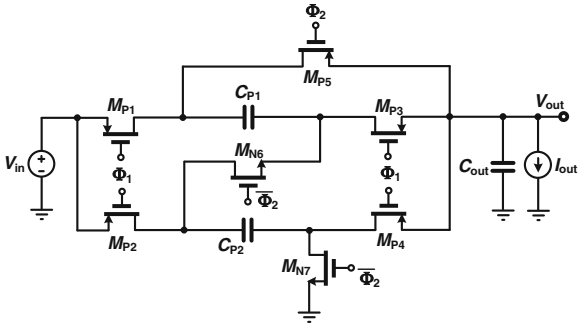

Fig. 7.15 Circuit implementation of the step-down SC power stage

it saves the power consumption and silicon area due to additional complex sensing circuitry used in the multi-loop regulation techniques. Secondly, the design complexity is significantly reduced since it employs a single operational amplifier as the only critical analog circuit block. Moreover, this module is fully designed in the discrete z-domain, with the implementation of the switched capacitor circuits. Hence, very accurate signal processing can be achieved due to its discrete sampling behavior.

To increase the sampling speed and simplify the design requirements on the amplifier, a HCDS scheme is employed. If a conventional A/D converter requires a signal to be sampled at a frequency of f_{clk}, the comparator and its corresponding clock signal should also be operated at f_{clk}. However, this design only needs a clock frequency of $f_{clk}/2$ and a slower comparator. In other words, with the same circuit modules, the proposed scheme doubles the sampling resolution.

Figure 7.15 illustrates the circuit implementation of the SC power stage. It employs seven power switched to achieve a 2/3 step-down voltage conversion with high efficiency. In each switching cycle, it operates in two phases, the charge phase Φ_1 and the discharge phase Φ_2. As shown in Fig. 7.16a during Φ_1 ("0" effective), the PMOS switches M_{P1}, M_{P2}, M_{P3} and M_{P4} are turned on. The pumping capacitors C_{P1} and C_{P2} are connected in parallel between V_{in} and V_{out}. As a result, each pumping capacitor is charged to a voltage level $V_{in} - V_{out}$. During the discharge phase Φ_2 ("0" effective) illustrated in Fig. 7.16b, the switches M_{P5}, M_{N6} and M_{N7} are turned on, while M_{P1}, M_{P2}, M_{P3} and M_{P4} are turned off. Hence, C_{P1} and C_{P2} are connected in series across V_{out}. The stored charge in C_{P1} and C_{P2} is then transferred to C_{out} and R_{out}.

As it can be observed from the following discussion, since C_{out} is charged in both phases, the output voltage ripple is smaller. Also, since the discharge current is sourced from the ground during Φ_2, the output current 3/2 times of the input current. This current multiplication improves the efficiency of the converter even when there is a large dropout between V_{in} and V_{out}. Note that, although Φ_1 and Φ_2 are in phase, a non-overlapping period t_D is introduced to avoid shoot-through current between the switches.

The next step in the design of the step-down SC power converter involves modeling its power stage. As illustrated in Fig. 7.16a, during the charge phase

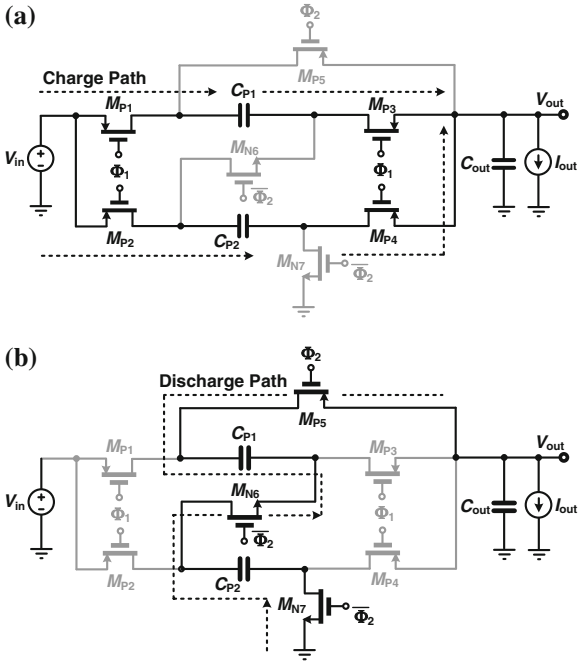

Fig. 7.16 **a** Charge and **b** discharge phase of the SC power converter

$\Phi_1 = 1$, voltage across the pumping capacitors is equal to $V_{in} - V_{out}$, while the voltage across the output capacitor is V_{out}. Thus, the total charge stored in the power stage Q_{ch} is given by

$$\begin{aligned} Q_{ch} =& 2C_P \cdot [V_{in}(t) - V_{out}(t)] + C_{out} \cdot V_{out}(t) \\ =& 2C_P \cdot V_{in}(t) + (C_{out} - 2C_P) \cdot V_{out}(t). \end{aligned} \tag{7.49}$$

During the discharge phase, as shown in Fig. 7.16b, the voltage across each of the pumping capacitors is $V_{out}/2$, while the voltage across C_{out} is V_{out}. Hence, the total charge in the power stage during the discharge phase Q_{dch} is

$$\begin{aligned} Q_{dch} =& 2C_P \cdot \left[\frac{1}{2} V_{out}(t + T_s)\right] + C_{out} \cdot V_{out}(t + T_s) \\ =& (C_P + C_{out}) \cdot V_{out}(t + T_s). \end{aligned} \tag{7.50}$$

According to the charge conservation theory, in steady state, $Q_{ch} = Q_{dch}$, thus

$$(C_P + C_{out}) \cdot V_{out}(t + T_s) = 2C_P \cdot V_{in}(t) + (C_{out} - 2C_P) \cdot V_{out}(t). \tag{7.51}$$

Equation (7.51) can be solved for $V_{out}(t + T_s)$ as

$$V_{out}(t + T_s) = a \cdot V_{in}(t) + b \cdot V_{out}(t). \tag{7.52}$$

$$\text{where, } a = \frac{2C_P}{C_P + C_{out}} \text{ and } b = \frac{C_{out} - 2C_P}{C_P + C_{out}}.$$

For the next switching period, the same equations can be applied to formulate V_{out}, as given by

$$\begin{aligned} V_{out}(t + 2T_s) =& a \cdot V_{in}(t + T_s) + b \cdot V_{out}(t + T_s), \\ =& a \cdot V_{in}(t + T_s) + b \cdot [a \cdot V_{in}(t) + b \cdot V_{out}(t)] \\ =& a \cdot (1 + b)V_{in}(t) + b^2 \cdot V_{out}(t). \end{aligned} \tag{7.53}$$

For the nth switching cycle, the expression for V_{out} can be written as

$$V_{out}(t + nT_s) = a \cdot \left(1 + b + b^2 + \ldots + b^{n-1}\right) V_{in}(t) + b^n \cdot V_{out}(t). \tag{7.54}$$

As $n \to \infty$, $b^n \to 0$. Then the polynomial from of $1 + b + b^2 + \ldots = 1/(1 - b)$. Hence, the CG can be determined as

$$\frac{V_{out}}{V_{in}} = \frac{a}{1 - b} = \frac{\frac{2C_P}{C_P + C_{out}}}{1 - \frac{C_{out} - 2C_P}{C_{out} + C_P}} = \frac{2}{3}. \tag{7.55}$$

To obtain the z–domain model of the charge pump, similar to the time domain analysis, during the charge phase, the voltage across the pumping capacitor is $V_{in} - V_{out}$ and the voltage across the output capacitor is V_{out}. Therefore, the total charge stored in the power stage during charge phase Q_{ch} is

$$\begin{aligned} Q_{ch}(n - 1)T_s =& 2C_P \cdot [V_{in}(n - 1)T_s - V_{out}(n - 1)T_s] + C_{out} \cdot V_{out}(n - 1)T_s \\ =& 2C_P \cdot V_{in}(n - 1)T_s + (C_{out} - 2C_P) \cdot V_{out}(n - 1)T_s. \end{aligned} \tag{7.56}$$

During the discharge state, the voltage across each pumping capacitor is $V_{out}/2$, while the voltage across C_{out} is V_{out}. Then, the total charge in the power stage during the discharge phase is

$$\begin{aligned} Q_{dch}(nT_s) =& 2C_P \cdot \left[\frac{1}{2} V_{out}(nT_s)\right] + C_{out} \cdot V_{out}(nT_s) \\ =& (C_P + C_{out}) \cdot V_{out}(nT_s). \end{aligned} \tag{7.57}$$

According to the charge conservation theory, $Q_{ch}(n - 1)T_s = Q_{dch}(nT_s)$, thus

$$(C_P + C_{out}) \cdot V_{out}(nT_s) = 2C_P \cdot V_{in}(n - 1)T_s + (C_{out} - 2C_P) \cdot V_{out}(n - 1)T_s. \tag{7.58}$$

Applying the z-transform to Eq. (7.58) gives

$$(C_P + C_{out}) \cdot V_{out} = 2C_P \cdot V_{in} \cdot z^{-1} + (C_{out} - 2C_P) \cdot V_{out} \cdot z^{-1}. \tag{7.59}$$

Equation (7.59) can be written in terms of V_{out} as

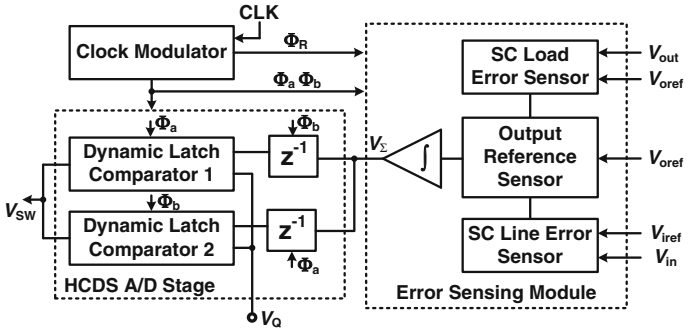

Fig. 7.17 Block diagram of the observation-based feedback controller

$$V_{\text{out}} = \frac{2C_{\text{P}}}{C_{\text{P}} + C_{\text{out}}} \cdot V_{\text{in}} \cdot z^{-1} + \frac{C_{\text{out}} - 2C_{\text{P}}}{C_{\text{out}} + C_{\text{P}}} \cdot V_{\text{out}} \cdot z^{-1}. \tag{7.60}$$

This can be written in the form of

$$V_{\text{out}} = a \cdot V_{\text{in}} \cdot z^{-1} + b \cdot V_{\text{out}} \cdot z^{-1}. \tag{7.61}$$

$$\text{where, } a = \frac{2C_{\text{P}}}{C_{\text{P}} + C_{\text{out}}} \text{ and } b = \frac{C_{\text{out}} - 2C_{\text{P}}}{C_{\text{P}} + C_{\text{out}}}.$$

From Eq. (7.61), the transfer function of the power stage can be obtained as

$$\frac{V_{\text{out}}}{V_{\text{in}}} = \frac{az^{-1}}{1 - bz^{-1}} = \frac{a}{z - b}. \tag{7.62}$$

From Eq. (7.62), it can be observed that the power stage is a single pole system. Moreover, since $b = (C_{\text{out}} - 2C_{\text{P}})/(C_{\text{P}} + C_{\text{out}}) < 1$, the pole lies within the unit circle in the z-domain.

7.2.3.2 Closed loop System Operation and Control Scheme

This section discusses the detailed control scheme and circuit implementation of the dual-loop OB feedback controller. The control scheme accurately regulates the output voltage, while the dual loop topology jointly ensures tight line and load regulation.

The block diagram of the OB feedback controller is illustrated in Fig. 7.17 and consists of the error sensing module, a half-clock double-sampling (HCDS) A/D stage, and a clock modulator. The basic operation of the controller is as follows. Firstly, the error sensing module samples the error present in the input power source V_{in}, and the output voltage V_{out}, by comparing them with their corresponding input reference V_{iref} and the output reference voltage V_{oref}, respectively.

The error sensing module then generates an integration signal V_{Σ}, which contains the sensed error information present in both the line and load voltages. V_{Σ} is then sent to the HCDS A/D stage and is further processed into a digital signal V_{sw}. This digital output signal then controls the switches in the charge pump, in order to provide the desired voltage regulation.

From Fig. 7.17, it can be observed that the error sensing module and the HCDS A/D converter both employ non-overlapping clock signals Φ_a and Φ_b, in order to sample the error voltage and convert them into corresponding digital signals. These oversampling clocks are generated by the clock modulator and sent to the overall system. The clock modulator also generates a reset clock Φ_R, which sets the switching frequency of the power stage by resetting the V_{Σ} signal in the OB error sensing module. The circuit design and theoretical analysis of the proposed OB based error sensing module is explained next.

The circuit diagram of the error sensing module in the OB feedback controller is shown in Fig. 7.18. The circuit design is implemented only with switched-capacitor circuits. The SC load error sensor, the output reference sensor and the SC line error sensor are implemented with three non-inverting double-sampled SC integrators. The output of all the three sensors are then combined with the aid of one output block, which consists of an op-amp, the integration capacitor C_{Σ} and the reset switch.

The operation of the OB error sensing module is as follows. Firstly, the output reference voltage V_{oref} sets the nominal slope of the output V_{Σ}, in the output reference sensor. If a voltage regulation error exists in either V_{in} or V_{out}, these errors are immediately sampled by the SC line and load error sensors and is then propagated to the output V_{Σ}. The amount of voltage error will change the nominal integration slope and will generate the appropriate switching activity in the power stage. The theoretical analysis of the OB error sensing is given as follows.

As illustrated in Fig. 7.18, the fundamental circuit of the OB error sensing module is the double-sampled SC integrator. To understand its operation and derive its transfer function, first consider the operation of a basic non-inverting integrator illustrated in Fig. 7.19. From the circuit schematic of the integrator, it can be observed that it consists of two major blocks. The first is an input block that is responsible to sample input voltage levels, followed by the output block that transfers the sampled voltage to the output load capacitor. To derive the z-domain transfer function of the complete system, the voltage to charge transfer function of the input block, in the form of Q/V_{in}, is initially derived. Second, the charge to voltage transfer function, V_{out}/Q, for the output block is derived. Then, by multiplying the two transfer functions, the transfer function of the entire system is obtained as

$$\left(\frac{Q}{V_{in}}\right) \cdot \left(\frac{V_{out}}{Q}\right) = \frac{V_{out}}{V_{in}}. \tag{7.63}$$

Thus, to obtain the transfer function of the input block, consider Fig. 7.20, which illustrates the input block for the non-inverting SC integrator. Node X is the

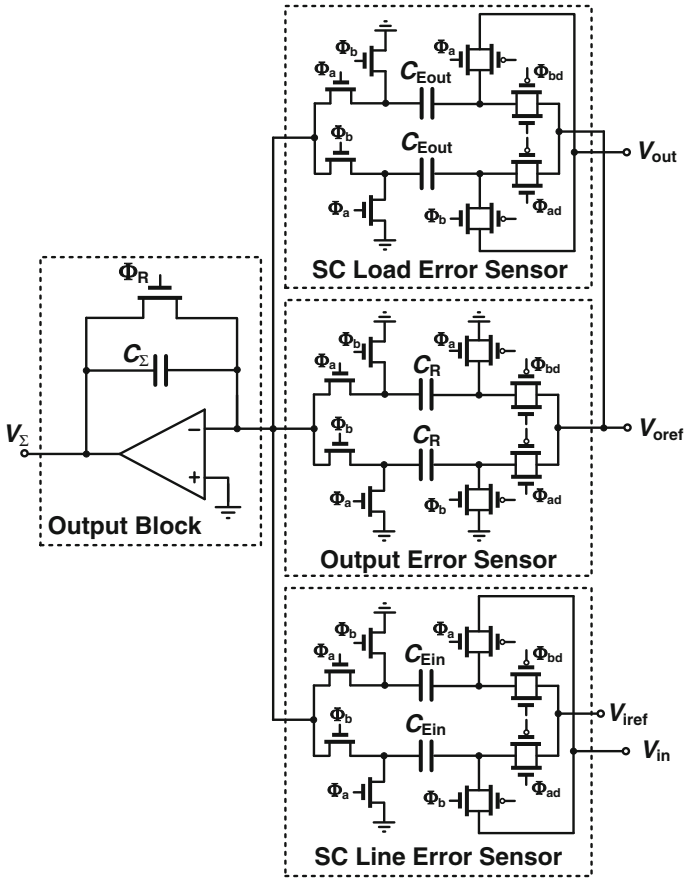

Fig. 7.18 Circuit implementation of the OB error sensing module

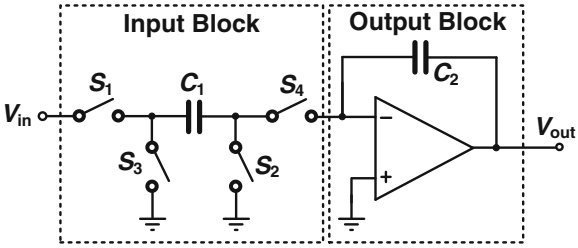

Fig. 7.19 Circuit schematic of a traditional non-inverting SC integrator

input node, while node Y is the output node and voltages V_X and V_Y are their corresponding node voltages. It can be observed that during the sampling phase, Φ_1 is high. Thus, the switches S_1 and S_2 are turned on, allowing the capacitor C_1 to charge up to the voltage V_X. During the transfer period, Φ_1 is low and Φ_2 is high.

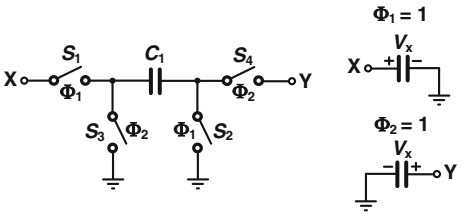

Fig. 7.20 Operation of the input block of the non-inverting SC integrator

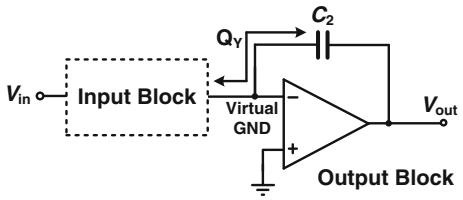

Fig. 7.21 Output block of the non-inverting SC integrator

This turns off the switches S_1 and S_2 and turns on the switches S_3 and S_4. As a result, the bottom plate of the capacitor is grounded. However, C_1 still holds the voltage V_X, thereby generating negative charge on the top plate of the capacitor. Since the capacitor plate at node Y produces negative charge, the charge equation Q/V_{in} should be positive since the input block will subsequently transfer the charge to the output with charge conservation nature. Hence, the charge equation for the input node can be written as

$$\frac{Q}{V_{in}} = \frac{Q_Y}{V_X} = C_1 \cdot z^{-1}. \tag{7.64}$$

The term z^{-1} in Eq. (7.64) is present since a delay of one clock cycle is generated due to the sampling action.

As illustrated in Fig. 7.21, the output stage of a SC circuit is typically realized by an op-amp with a negative feedback capacitance. Assuming the ideal behavior of the op-amp, its input impedance is infinite, so all the current from the input block flows to the feedback capacitor C_2. The discrete-time charge transfer model can be expressed as a difference equation given by

$$Q_{out}(nT_s) = Q_{out}(n-1)T_s + Q_Y(nT_s). \tag{7.65}$$

Q_{out} is the charge stored at the output and Q_Y is the amount charge transferred from the input block to the output stage. Applying the z-transform to Eq. (7.65) gives

$$Q_{out} = Q_{out} \cdot z^{-1} + Q_Y. \tag{7.66}$$

The voltage-charge equation can thus be obtained as

$$C_2 V_{out} = C_2 V_{out} \cdot z^{-1} + Q_Y. \tag{7.67}$$

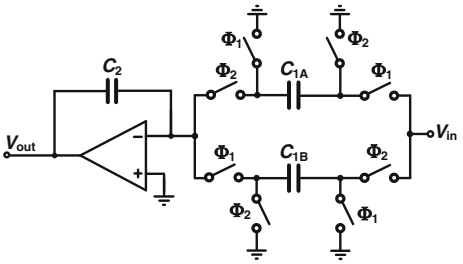

Fig. 7.22 Circuit implementation of the double-sampling SC integrator

As a result, V_{out}/Q_Y is given by

$$\frac{V_{out}}{Q_Y} = \frac{1}{C_2(1 - z^{-1})}. \tag{7.68}$$

Therefore, the transfer function of the non-inverting SC integrator can be written as

$$\frac{V_{out}}{V_X} = \frac{Q_Y}{V_Y} \cdot \frac{V_{out}}{Q_Y} = \left(C_1 \cdot z^{-1}\right) \cdot \frac{1}{C_2(1 - z^{-1})} = \frac{C_1}{C_2} \cdot \frac{z^{-1}}{(1 - z^{-1})}. \tag{7.69}$$

Based on the operation of the traditional non-inverting SC integrator, the operation of the double-sampling SC integrator can be realized. From Fig. 7.22, it can be observed that the input sampling stage of the integrator is very similar to that of the traditional non-inverting SC integrator. However, it contains two charge transfer paths that are connected in parallel and are operated in a complementary manner with respect to each other. For example, when the signal Φ_1 is high, the capacitor C_{1A} is charged to input V_{in}, while the capacitor C_{1B} transfers the charge stored from the previous phase to the output capacitor C_2. Correspondingly, when Φ_2 is high, C_{1A} transfers the stored charge to C_2, while C_{1B} is charged to V_{in}. In this manner, it can be observed that during each clock cycle, the input voltage V_{in} is effectively sampled twice. Moreover, a delay of half clock cycle exists due to the sampling nature of the circuit. Therefore, if $C_{1A} = C_{1B} = C_1$, the z-domain transfer function for the double-sampling SC integrator can be written based on Eq. (7.69) as

$$\frac{V_{out}}{V_{in}} = \frac{C_1}{C_2} \cdot \frac{z^{-1/2}}{(1 - z^{-1/2})}. \tag{7.70}$$

In Eq. (7.70), it can be observed that the unit delay term z^{-1} is modified to $z^{-1/2}$ due to the half clock cycle delay, as a result of the double sampling nature of the SC integrator.

Based on the fundamental understanding of the double-sampling SC integrator, the transfer function of the OB error sensing module can now be obtained. First consider the output reference sensor, which samples the voltage V_{oref}. This circuit employs a sampling capacitor C_R and a feedback capacitor C_Σ, as illustrated in

Fig. 7.18. Hence, the expression for the output voltage that is contributed by the output reference sensor is given as

$$V_{\Sigma \text{out\_ref}}(z) = \frac{C_R}{C_\Sigma} \cdot \frac{z^{-1/2}}{(1 - z^{-1/2})} V_{\text{oref}}. \tag{7.71}$$

Similarly, the z-domain expression for the SC load error sensor is given as

$$V_{\Sigma \text{load\_error}}(z) = \frac{C_{\text{Eout}}}{C_\Sigma} \cdot \frac{z^{-1/2}}{(1 - z^{-1/2})} (V_{\text{oref}} - V_{\text{out}}). \tag{7.72}$$

It can be observed that the effective input voltage for the load error sensor is $V_{\text{oref}} - V_{\text{out}}$, since the voltage V_{oref} is sampled during the sampling phase, while V_{out} is sampled during the transfer phase of the SC integrator. Lastly, the z-domain expression for the SC line error sensor is given as

$$V_{\Sigma \text{line\_error}}(z) = \frac{C_{\text{Ein}}}{C_\Sigma} \cdot \frac{z^{-1/2}}{(1 - z^{-1/2})} (V_{\text{iref}} - V_{\text{in}}). \tag{7.73}$$

When the Eqs. (7.71), (7.72) and (7.73) are combined, the total integration output $V_\Sigma(z)$ can be obtained as

$$V_\Sigma(z) = \frac{C_{\text{Eout}}}{C_\Sigma} \cdot \frac{z^{-1/2}}{(1 - z^{-1/2})} (V_{\text{oref}} - V_{\text{out}}) + \frac{C_R}{C_\Sigma} \cdot \frac{z^{-1/2}}{(1 - z^{-1/2})} V_{\text{oref}} + \frac{C_{\text{Ein}}}{C_\Sigma} \cdot \frac{z^{-1/2}}{(1 - z^{-1/2})} (V_{\text{iref}} - V_{\text{in}}). \tag{7.74}$$

If the voltage error $V_{\text{oref}} - V_{\text{out}}$ is represented as V_{Eout} and $V_{\text{iref}} - V_{\text{in}}$ is represented as V_{Ein}, Eq. (7.74) can be expressed as

$$V_\Sigma(z) = \frac{C_R}{C_\Sigma} \cdot \left(\frac{C_{\text{Eout}}}{C_R} V_{\text{Eout}} + V_{\text{oref}} \right) \cdot \frac{z^{-1/2}}{(1 - z^{-1/2})} + \frac{C_{\text{Ein}}}{C_\Sigma} \cdot \frac{z^{-1/2}}{(1 - z^{-1/2})} V_{\text{Ein}}. \tag{7.75}$$

Equation (7.75) can be re-written as

$$V_\Sigma(z) = \frac{C_R}{C_\Sigma} \cdot (G_{\text{DC}} V_{\text{Eout}} + V_{\text{oref}}) \cdot \frac{z^{-1/2}}{(1 - z^{-1/2})} + G_{\text{line}} V_{\text{Ein}} \cdot \frac{z^{-1/2}}{(1 - z^{-1/2})}. \tag{7.76}$$

G_{DC} is the DC gain of the feedback load regulation loop and G_{line} is feed-forward line regulation gain. When no error exists, $V_{\text{Eout}} = V_{\text{Ein}} = 0$. Then, Eq. (7.66) becomes

$$V_\Sigma(z) = \frac{C_R}{C_\Sigma} \cdot V_{\text{oref}} \cdot \frac{z^{-1/2}}{(1 - z^{-1/2})}. \tag{7.77}$$

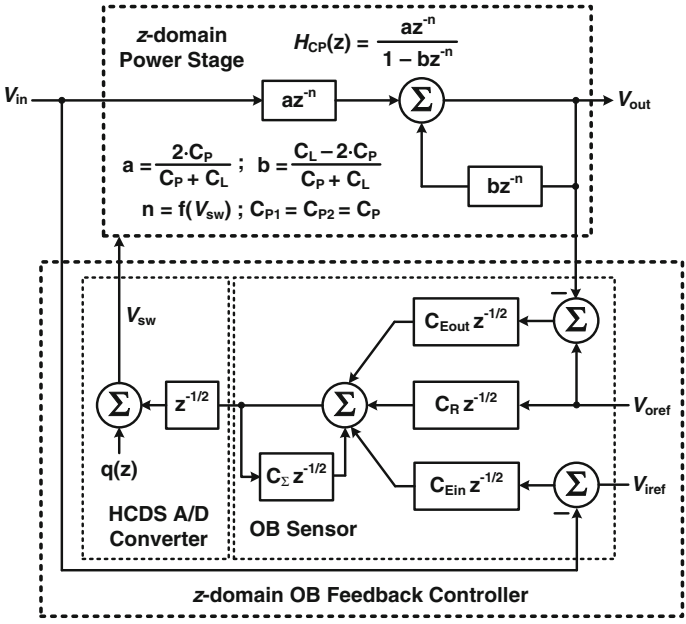

Fig. 7.23 z-domain model of the SC power converter with the OB feedback controller

Since V_{oref} is a fixed value, the integrator slope is determined only by a capacitor ratio of C_R/C_Σ. Thus, C_R/C_Σ is the nominal gain of the integrator, H. Finally, using all the derived and defined terms, the analysis is summarized as follows.

$$V_\Sigma(z) = H \cdot \left(G_{DC} V_{Eout} + V_{oref} + G_{line} V_{Ein}\right) \cdot \frac{z^{-1/2}}{\left(1 - z^{-1/2}\right)}, \tag{7.78}$$

where $H = C_R/C_\Sigma$, $G_{DC} = C_{Eout}/C_R$ and $G_{line} = C_{Ein}/C_\Sigma$. All the z^{-1} delay terms are reformed to $z^{-1/2}$ due to the double-sampling architecture. Equation (7.78) shows that the OB error sensing module provides the integration output V_Σ, which contains the error information related to the line and load signals. This integration signal is then reset by the reset clock Φ_R, which also determines the switching frequency of the power stage. The reset is achieved by connecting the integrator's output node to the virtual ground, as shown in Fig. 7.18. Moreover, the sampling frequency of Φ_a and Φ_b of the OB error sensor module is much higher than the switching frequency f_s of the converter. As a result, it allows the OB error senor module to respond to variations faster and with higher resolution.

Based on Eqs. (7.77) and (7.78) the complete z-domain model of the SC power converter is illustrated in Fig. 7.23 and is used to design the OB feedback controller. The OB feedback controller takes V_{in} and V_{out} as inputs for line and load regulation error generation. The generated errors $C_{Ein} \cdot z^{-1/2} \cdot (V_{iref} - V_{in})$, $C_{Eout} \cdot z^{-1/2} \cdot (V_{oref} - V_{out})$ and the reference signal $C_R \cdot z^{-1/2} \cdot V_{oref}$ are then weighted,

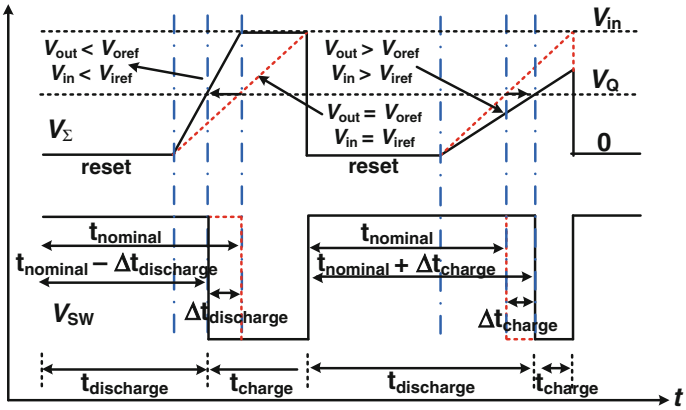

Fig. 7.24 Operation waveforms of the OB feedback controller

summed and integrated by the summing integrator. The output voltage of the integrator V_Σ is then digitized by a SC HCDS A/D converter, with a reference quantization voltage V_Q.

Figure 7.24 shows the operation waveforms of the OB feedback controller, which achieves dual loop voltage regulation in the SC power converter. Its detailed operation is as follows. The operation of the controller is separated into two 'reset' and 'sensing' states. The SC charge pump mainly has two operating phases, the charge phase and the discharge phase. In the charge phase, the pumping capacitor is charged based on the amount of energy that should be delivered to the output. In the discharge phase, the pumping capacitor must be fully discharged in order to transfer all the energy to the output. If any charge remains on the capacitor during the discharge phase, then it is lost. This will result in a reduced efficiency of the SC converter. As a result, the charge period of the converter is equal to 50 % of the switching period. If the charge period exceeds 50 % of one switching cycle, the capacitor cannot be fully discharged since the charge time exceeds the discharge time. As a result the reset period is set to 50 %, which is the minimum period required in the discharge phase.

As illustrated in Fig. 7.24, the operation point that determines the switching actions in the charge pump is set by the voltage V_Q. During the steady state, without any errors in the input power source or the regulated output voltage, V_Σ takes 25 % of the clock period $T_{nominal}$ to reach the quantization level V_Q. As a result, the length of the discharge period is $0.75T_{nominal}$, while the charge period lasts for $0.25T_{nomimal}$. Thus, the 25 % duty ratio that is applied to the power stage performs the required voltage regulation. Secondly, consider the case where line and load variations exist in the system. Line and load errors have a negative coefficient. As a result, when $V_{in} > V_{iref}$ and when $V_{out} > V_{oref}$, the integration slope is decreased. Hence, it takes a longer time for V_Σ to reach the quantization level, which leads to a smaller duty ratio ("0" effective). When $V_{in} < V_{iref}$ or when

$V_{out} < V_{oref}$, the integration slope is increased. Thus, it takes shorter time for V_{Σ} to reach the quantization level, thereby generating a larger duty ratio. Lastly, if the voltage level at V_{in} or V_{out} is too high in comparison to their reference values, the controller generates a 0 % duty ratio to discharge the output at the fastest rate. Similarly, if V_{in} or V_{out} is too low, the controller generates a 50 % duty ratio to charge the output quickly, in order to achieve a fast transient response. Compared to the traditional designs that require multiple amplifiers, comparators and voltage references for dual loop line and load error sensing, this design requires just a single amplifier, two reference voltages, along with a few switches and capacitors to realize dual loop regulations. This provides a significant benefit in terms of saving power and silicon area.

7.3 Conclusions

This chapter presents the design of SC power converters in z-domain, which aim to improve various performance parameters such as efficiency, line and load transient response, on-chip silicon area requirements, cost and so on. This is implemented through the use of various innovative charge pump topologies, control schemes and efficient circuit design techniques.

The chapter first introduces the concept of z-domain analysis of switches and capacitor in SC networks. It presents the link two-port representation for charge pumps, which is based on the charge–voltage relationship for each pumping capacitor. The chapter then investigates three case studies, which discuss the design of practical SC power converters. The first SC power converter presented was an interleaved cross-coupled SC voltage doubler. This power converter is regulated using an analog PWM control scheme. The accurate design of the closed loop system is presented by modeling both the power stage and the feedback controller in the z-domain. The interleaving charge pump topology provides a cost-effective solution with low output voltage ripple and fast transient response.

The second converter to be discussed in this chapter is a monolithic step-down SC power converter design. The power converter employs a subthreshold operated controller and frequency programmable DPWM regulation scheme. This significantly reduces the power consumption and improves signal processing speed of the power supply. The fully on-chip implementation significantly reduces system volume and switching noises. The number of I/O pins and on-chip bonding pads as well as parasitic components is significantly reduced. Thus, this design provides an effective solution for new generation, monolithic power supplies for self-powered devices.

Lastly, the third power converter to be discussed in this chapter is an adaptive SC power converter with a dual-loop observation-based line/load regulation scheme. The power stage is a step-down charge pump, which efficiently achieves a 2/3 voltage regulation. In order to achieve closed loop feedback control, the converter employs a cost-effective OB controller, which is developed with the use

of only switched-capacitor circuits. Through the use of a double-sampling technique, the controller is capable of quickly identifying and responding to line and load variations in a very power-efficient manner. Hence, each of the three converters discussed employs various unique features that enhance their operating performance. This makes these power supplies highly suitable for emerging low-power VLSI applications.

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