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Valentijn De Smedt
Georges Gielen
Wim Dehaene

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Valentijn De Smedt
Georges Gielen
Wim Dehaene
ESAT-MICAS
University of Leuven
Heverlee
Belgium

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The only reason for time is so that everything doesn't happen at once.

–A. Einstein

Preface

"Most of what makes a book 'good' is that we are reading it at the right moment for us" is a quote from the Swiss-British philosopher Alain De Botton. The quote is right on top for a book where timing is the central given. Read this book about timing if at this moment your design is in need of an accurate yet efficient timing reference!

The book you are holding is the result of several years of Ph.D. research that started with the ambition to set important steps toward the implementation of batteryless wireless sensor nodes. Relatively soon it became clear that accurate timing is one of the key points in realizing this. Therefore the focus shifted to the construction of a low power, supply, and/or temperature independent timing reference. This topic in its turn surpasses the world of wireless sensor networks as it is much wider applicable.

We are convinced that the results we present here can help you in several ways. You can have a look at the circuits and concepts and adapt them for your system. More importantly the book can act as a source of inspiration for all those that are involved in sensor network design and the hardware for the Internet of Things. We dare to hope that the book brings you as much research inspiration as it brought us research joy while creating it.

Leuven, September 2014

Valentijn De Smedt
Georges Gielen
Wim Dehaene

Contents

Abstract

Back in 2000, the Nobel prize committee recognized the invention of the integrated circuit in 1958 by Jack Kilby as one of the most far-reaching steps forward in modern technology. Today, almost 60 years after this invention, electronics are found everywhere in our society. This is mainly caused by the characteristic exponential growth factors in the electronics industry (Moore's law), which result in an exponential miniaturization and cost decrease. This evolution goes hand in hand with a similar growth of wireless communication technology: devices become smaller, frequencies and data rates higher. As a result, the wearability and functionality of wireless electronic devices drastically increase.

This ongoing technological progress is a direct cause of the appearance of Wireless Sensor Networks (WSN). An increasing number of autonomously operating devices is wirelessly connected to a network and/or to the Internet, an evolution which will eventually result in the so-called Internet of Things. Since both the miniaturization as well as the cost decrease of these wireless sensor nodes is necessary to become economically feasible, a growing need for fully-integrated, single-chip wireless devices is observed. The use of modern deep-submicron CMOS technologies in analog electronics, however, has several drawbacks in terms of temperature sensitivity and linearity.

This work elaborately investigates the possible circuit techniques to overcome the temperature and supply voltage sensitivity of fully integrated time references for ultra-low-power wireless communication in WSN. In a first step, the basic needs to build a frequency reference are studied. Furthermore, a closer look at the short-term as well as the long-term frequency stability of integrated oscillators is taken. This results in a design strategy, which is applied to six different oscillator design cases. All six implementations are subject to a study of phase noise and long-term frequency stability.

The first two implementations are respectively a temperature- and a supply voltage-independent Wien bridge oscillator. The temperature independence is obtained by using a novel feedback amplifier topology of which the output resistance only depends on a temperature stable resistor. This requires advanced circuit techniques and a highly-stable amplitude regulation circuit. The second Wien

bridge implementation makes use of two nested regulators, resulting in an ultra-high supply voltage stability over a wide voltage range.

The third design case makes use of a high-quality bondwire LC tank. A novel pulsed driving technique is developed to decrease the power consumption of the high-frequency oscillator circuit. This driving technique reduces the impact of the oscillator circuitry on the output frequency and therefore also on the temperature- and supply voltage stability of the oscillator. To better understand the application field of the pulsed oscillator topology, the noise performance is analyzed as well. The processed implementation is a unique combination of power consumption and long-term frequency stability.

Next, two injection-locked oscillator implementations are discussed. Apart from a stable output frequency, a high absolute accuracy is also obtained due to the locking to a wirelessly received RF signal. The first design uses the received 2.4 GHz carrier frequency as a time reference. Despite its simple system topology, this approach has several drawbacks in terms of selectivity and power consumption. The second implementation locks to the envelope of the received RF signal. Therefore, the oscillator can run at a low frequency, drastically diminishing the power consumption. A second improvement is the addition of a network coordination receiver. For this purpose, a novel ultra-low-power receiver topology and demodulation technique are developed. As a result of the addressability, the overall power consumption in the network is reduced.

The last design case is a temperature- and supply voltage-independent oscillator-based sensor interface. Since the challenge in this design is rather the stability of the output value than the frequency stability, a different design strategy is used. It is shown that the matching of different oscillator delay stages can be applied to obtain a stable and highly-linear digitalization of a sensor input.

The wirelessly injection-locked oscillator, the coordination receiver, the sensor interface, and a transmitter are combined into one highly-flexible wireless tag. The content, the scrambling code, and the length of the transmitted data burst can be adapted freely, depending on the application. The developed tag can therefore be used in a wide range of applications, with different accuracy requirements and energy constraints.

Finally, an elaborate comparison between the developed oscillator designs and the state of the art is performed. It is shown that the free-running implementations as well as the injection-locked designs improve the state of the art. This discussion results in several suggestions for possible future work.

About the Authors

Valentijn De Smedt (S'08) was born in Lubbeek, Belgium, in 1984. He received the M.Sc. degree in electrical engineering from the Katholieke Universiteit Leuven in 2007. The subject of his Master thesis was the design of an accurate integrated frequency reference. From 2007 to 2014 he was working as a research assistant at the MICAS laboratories of the Katholieke Universiteit Leuven towards a Ph.D. degree on the design of ultra-low-power time-based building blocks for wireless sensor networks, which he received in April 2014. At KU Leuven, he was involved in and has set up several extra-curricular educational projects, some of them in co-operation with the IEEE Student Branch of Leuven.

He has been vice-chair technical activities of the IEEE student branch of Leuven between 2009 and 2013 and chaired the IEEE Student Branch and GOLD congress 2010 (SBC 2010). Since 2011, he is IEEE Benelux GOLD (Young Professionals) chair and co-chair of the IEEE SSCS Benelux chapter. Since 2009 he is a guest lecturer at ACE Group-T on UWB standards and Zigbee.

Georges G.E. Gielen received the M.Sc. and Ph.D. degrees in Electrical Engineering from the Katholieke Universiteit Leuven (KU Leuven), Belgium, in 1986 and 1990, respectively. He is a full professor at the Department of Electrical Engineering (ESAT). From August 2013, Georges Gielen is also appointed as vice-rector for the Group Science, Engineering and Technology and Academic Personnel of the KU Leuven.

His research interests are in the design of analog and mixed-signal integrated circuits, and especially in analog and mixed-signal CAD tools and design automation. He is a coordinator or partner of several (industrial) research projects in this area, including several European projects. He has authored or coauthored seven books and more than 450 papers in edited books, international journals, and conference proceedings. He is a Fellow of the IEEE since 2002.

Wim Dehaene was born in Nijmegen, The Netherlands, in 1967. He received the M.Sc. degree in electrical and mechanical engineering in 1991 from the Katholieke Universiteit Leuven. In November 1996, he received the Ph.D. degree at the Katholieke Universiteit Leuven. His thesis is entitled "CMOS integrated circuits for analog signal processing in hard disk systems."

After receiving the M.Sc. Degree, Wim Dehaene was a research assistant at the ESAT-MICAS Laboratory of the Katholieke Universiteit Leuven. His research involved the design of novel CMOS building blocks for hard disk systems. The research was first sponsored by the IWONL (Belgian Institute for Science and Research in Industry and Agriculture) and later by the IWT (the Flemish institute for Scientific Research in the Industry). In November 1996, Wim Dehaene joined Alcatel Microelectronics, Belgium. There he was a senior project leader for the feasibility, design and development of mixed mode systems on chip. The application domains were telephony, xDSL, and high-speed wireless LAN. In July 2002, Wim Dehaene joined the staff of the ESAT-MICAS Laboratory of the Katholieke Universiteit Leuven where he is now a full professor. His research domain is circuit level design of digital circuits. The current focus is on ultra low power signal processing and memories in advanced CMOS technologies. Part of this research is performed in cooperation with IMEC, Belgium where he is also a part-time principal scientist.

Wim Dehaene is teaching several classes on electrical engineering and digital circuit and system design. He is also very interested in the didactics of engineering. As such, he is guiding several projects aiming to bring engineering to youngsters and he is a teacher in the teacher education program of the KU Leuven.

Wim Dehaene is a senior member of the IEEE. Wim Dehaene is a member of the technical program committee of ESSCIRC and ISSCC.

Abbreviations

A-ISF	Amplitude Impulse Sensitivity Function
AC	Alternating Current
AM	Amplitude Modulation
BBPLL	Bang–Bang Phase-Locked Loop
BER	Bit Error Rate
BJT	Bipolar Junction Transistor
CMB	Cosmic Microwave Background
DAC	Digital-to-Analog Converter
EEF	Energy Enhancement Factor
ELP	Extremely-Low Power
ENOB	Effective Number of Bits
ETF	Electro-Thermal Filter
FET	Field-Effect Transistor
FLL	Frequency-Locked Loop
FoM	Figure of Merit
FRS	Fellow of the Royal Society
FSM	Finite State Machine
IFF	Identification Friend or Foe
IoT	Internet of Things
IR-UWB	Impulse Radio Ultra-Wideband
ISF	Impulse Sensitivity Function
JFET	Junction Field-Effect Transistor
LDO	Low-DropOut
LFSR	Linear Feedback Shift Register
LTI	Linear Time-Invariant
LTV	Linear Time-Variant
MEMS	Microelectromechanical systems
MiM	Metal-insulator-Metal

MoI	Moment of Impact
MoM	Metal-oxide-Metal
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
OCXO	Oven-Compensated Crystal Oscillator
P-UWB	Pulsed Ultra-Wideband
PC	Personal Computer
pcb	Printed Circuit Board
PDF	Probability Density Function
ppb	Parts per billion
ppm	Parts per million
PSD	Power Spectral Density
PVT	Process, Temperature and (Supply) Voltage
PW	Pulse Width
RF	Radio Frequency
RFID	Radio Frequency Identification
rms	Root mean square
SNDR	Signal to Noise and Distortion Ratio
SNR	Signal to Noise Ratio
TANSTAAFL	There Ain't No Such Thing As A Free Lunch
TCXO	Temperature-Compensated Crystal Oscillator
ULP	Ultra-Low Power
VCO	Voltage-Controlled Oscillator
VCXO	Voltage-Controlled Crystal Oscillator
WSN	Wireless Sensor Network
XO	Crystal Oscillator

Symbols

$\alpha(\omega \cdot t)$	Deterministic, periodic function with period 2π
α_k	Phase shift of the k-th harmonic of a voltage oscillator signal
α_{μ_n}	Temperature coefficient of the electron mobility
$\alpha_{V_{th}}$	Temperature coefficient of the transistor threshold voltage
β	Phase modulation index
β_k	Phase shift of the k-th harmonic of a voltage oscillator signal
$\Delta\omega_{3dB}$	−3 dB width of a resonant peak in a transfer function
Δf_{-3dB}	Half-power width of an oscillator output spectrum
ΔT_n	Delay error induced by noise
ΔV_n	Output voltage error induced by noise
ΔV_{rel}	Relative supply voltage span, as defined in Sect. 4.3.2
$\mathscr{A}(\Delta\omega)$	Amplitude noise density at frequency offset $\Delta\omega$, relative to the carrier
$\Delta\omega_0$	Difference between the fundamental frequency ω_0 and the natural frequency ω_n of the tuned network
$\Delta\omega_n$	Angular frequency difference between the natural oscillator frequency ω_n and the frequency of an injected signal ω_i
$\Delta\omega_{inj}$	Frequency perturbation on the injected signal i_{inj}, equal to $d\phi_{inj}(t)/dt$
$\Delta\omega_{nn}$	Frequency perturbation on the free-running oscillator signal (not the injection-locked oscillator signal), equal to $d\phi_{nn}(t)/dt$
$\Delta\phi_i(t)$	Perturbation of the phase shift between an oscillator current and an injected current (due to noise), equal to $\Delta\phi_{inj}(t) - \Delta\phi_{osc}$
$\Delta\phi_{inj}(t)$	Perturbation on the phase of the injected signal i_{inj}
$\Delta\phi_{osc}$	Perturbation on the phase of the (locked) oscillator signal

δ_k	Relative amplitude of the k-th harmonic of the voltage waveform, compared to the amplitude of the fundamental frequency
δ_{Xx}	Skin-depth of a conducting material Xx (for instance Silver, Ag)
ε	Parameter equal to A_{inj}/A_{osc}
$\varepsilon(t)$	Random amplitude variation of an oscillator signal
γ	Constant parameter used to determine the bandwidth of a Lorentzian spectrum, equal to $\pi \cdot f_0^2 \cdot c$
$\Gamma(x)$	The Impulse Sensitivity Function (ISF) with period $2 \cdot \pi$
$\Gamma_i(x)$	Impulse Sensitivity Function (ISF) on node i with period $2 \cdot \pi$
γ_k	Relative amplitude of the k-th harmonic of the voltage waveform, compared to the amplitude of the fundamental frequency
$\Gamma_{eff}(x)$	Effective Impulse Sensitivity Function (ISF), taking cyclostationary noise sources into account
Γ_{rms}	Root mean square (rms) value of the Impulse Sensitivity Function (ISF)
$\Lambda(x)$	Amplitude Impulse Sensitivity function (A-ISF), with period $2 \cdot \pi$
λ_i	Eigenvalue with corresponding eigenvector $\mathbf{u_i}$
$\Lambda_i(x)$	Amplitude Impulse Sensitivity function (A-ISF) on node i, with period $2 \cdot \pi$
$\boldsymbol{\rho}$	Generalized eigenvector with corresponding eigenvalue λ
μ	Scalar nonlinearity parameter in the *van der Pol* equation
μ_{Xx}	Magnetic permeability of a conducting material Xx (for instance Silver, Ag)
Ω	Unit of electrical resistance
ω	Instantaneous angular frequency, pulsation, $2\pi f$
$\omega(t)$	Instantaneous angular frequency over time
ω_0	Constant mean angular frequency of an oscillator, often used as the angular frequency in standard conditions
ω_B	Beating frequency of an injected oscillator
ω_i	Angular frequency of an injected signal
ω_L	One-sided lock range of an injection-locked oscillator
ω_m	Angular frequency of a motor
ω_n	Natural angular frequency of an electrical (tuned) network, natural angular frequency of an oscillator, $2\pi f_n$
Φ	magnetic flux due to the magnetic poles in a motor
$\Phi(t)$	Instantaneous phase of an oscillator signal
$\phi(t)$	Random variations of noise in the phase function, also called excess phase function
ϕ_∞	Steady-state phase shift between the oscillator current and the injected current

$\phi_i(t)$	Phase shift between the oscillator current and the injected current
ϕ_{ETF}	Phase shift of an Electro-Thermal Filter
$\phi_{i,0}$	Initial phase shift between the oscillator current and the injected current
$\phi_{inj}(s)$	Phase shift of the injected signal in the frequency domain
$\phi_{nn}(s)$	Phase shift of the free-running oscillator signal in the frequency domain
$\phi_{nn}(t)$	Phase shift of the free-running oscillator signal (not the injection-locked oscillator signal)
$\phi_{osc}(s)$	Phase shift of the locked oscillator signal in the frequency domain
ψ	Phase shift between the injected signal and the relaxation oscillator current
$\Psi(t)$	Systematic or deterministic variations in the phase function
ρ_{Xx}	Conductivity of a conducting material Xx (for instance Silver, Ag)
$\sigma(A,f,\tau)$	Allan variance of the output of a function f with dead time τ between the subsequent samples
$\sigma(T_h,T_l)$	Covariance between two stochastic periods
σ_c	Cycle-to-cycle jitter of an oscillator output signal
$\sigma_{A,h,l}$	Allan covariance between two variables T_h and T_l (with dead time τ)
$\sigma_{abs}(t = N \cdot \tau_{avg})$	Standard deviation of the absolute jitter after N oscillation cycles, sometimes also called the absolute jitter
σ_{cc}	Alternative definition of the cycle-to-cycle jitter, calculated using the difference between subsequent periods
$\sigma_{LC,Cte}$	Average cycle-to-cycle jitter of the output waveform of a resonant tank with constant output amplitude
$\sigma_{LC,Pulsed,N}$	Standard deviation of the length of the pulsed period of an LC tank, normalized to $T_{LC}/2$
σ_{LC}	Average cycle-to-cycle jitter of the output waveform of a resonant tank with decaying output amplitude
σ_{T_n}	Standard deviation (rms) of the time noise on a stage delay
σ_{V_n}	Standard deviation (rms) of the voltage noise
τ	An arbitrary moment in time
τ_i	Period of the i-th oscillation cycle
τ_{avg}	Average period of an oscillator output signal
$\theta(t)$	Phase shift of an oscillation over time (compared to $\omega_n \cdot t$)
θ_0	Initial phase shift of an oscillation
θ_i	Phase shift induced by a small injected signal in the oscillator, angle between the oscillator signal and the resulting signal
θ_n	Phase shift of a tuned network at $\omega \neq \omega_n$

$\Upsilon(t)$	Deterministic and systematic amplitude variations of an oscillator signal
A	Voltage gain of a generic amplifier
A_0	Ideal constant amplitude of an oscillator signal
A_1	Linear gain of a voltage dependent transconductance amplifier
A	Ampère, unit of electrical current
A_D	Area or size of a diode junction
A_{ds}	Amplitude of the drain-source current in an oscillator
$A_{env,DC}$	DC approximation of the complex envelope of an oscillator output signal
$A_{env}(t)$	Complex envelope of an oscillator output signal
A_i	i-th-order gain of a voltage dependent transconductance amplifier
A_{inj}	Amplitude of a signal injected in an oscillator
A_{osc}	Amplitude of an oscillator signal current
A_R	Area or size of a resistor
A_r	Amplitude of the resulting oscillator signal, sum of the injected current and the oscillator current
$A(t)$	Instantaneous amplitude of an oscillator signal
A_t	Minimum attenuation of a feedback network
A_v	Voltage gain of an amplifier
B	Bandwidth of a modulating signal
C	Capacitance, a capacitor
c	Motor constant, speed of light
c	Constant parameter used to determine the bandwidth of a Lorentzian spectrum
C_{ds}	Drain-source capacitor of a MOS transistor
C_{gd}	Gate-drain capacitor of a MOS transistor
C_{gs}	Gate-source capacitor of a MOS transistor
c_i	Complex i-th pole frequency
C_{ox}	Gate-oxide capacitance per unit area of a MOS transistor
C_p	Parallel capacitor in the equivalent quartz crystal model
C_s	Series capacitor in the equivalent quartz crystal model
DC	Duty cycle of a digital signal
e	Euler's constant
$E_{Decay}(N)$	Energy loss over N oscillation cycles in a resonant tank with exponentially decaying output amplitude
E_M	Back electromotive force
$E_{Osc}(N)$	Energy loss over N oscillation cycles in a resonant tank with constant output amplitude
$f(\Phi(t))$	Periodic function of $\Phi(t)$ with period $2 \cdot \pi$
F	Device excess noise factor
F_{amp}	Noise factor of an amplifier

F	Farad, unit of electrical capacitance
f_i	State variable of an oscillation on node i, normalized to amplitude and frequency
$f_i(x_1, \ldots, x_n)$	A smooth real-valued function of $x_1, \ldots, x_n$
FoM_{AD}	Figure of Merit for Analog to Digital converters
FoM_{JT}	Jitter and Temperature-dependency Figure of Merit (FoM) of an oscillator
FoM_{PN}	Phase noise Figure of Merit (FoM) of an oscillator
$FoM_{PN,tuned}$	Phase noise Figure of Merit (FoM) of an oscillator, taking the tuning sensitivity into account
FoM_{PNT}	Phase noise and Temperature-dependency Figure of Merit (FoM) of an oscillator
FoM_{PNTV}	Phase noise, Temperature-dependency and Voltage-dependency Figure of Merit (FoM) of an oscillator
FoM_{TV}	Temperature- and Voltage-dependency Figure of Merit (FoM) of an oscillator
FoM_V	Voltage-dependency Figure of Merit (FoM) of an oscillator
G	Transconductance of a generic amplifier
g_m	Transconductance of a transistor
g_{mb}	Transconductance of the bulk of a transistor
$G_m(v)$	Gain of a nonlinear negative resistance or amplifier
$g_{m,wi}$	Transconductance of a MOS transistor in weak-inversion
$G(s)$	Transconductance of a generic amplifier, dependent on the Laplace variable (representing the frequency)
$G(v)$	Input-amplitude-dependent transconductance of a generic amplifier
$h_\phi(t, \tau)$	Unit impulse response for the excess phase for a charge injected at time τ
$h_A(t, \tau)$	Unit amplitude impulse response for a charge injected at time τ
H	Henry, unit of electrical inductance
$H_{inj}(j \cdot \Delta\omega)$	Transfer function of the phase perturbations on the injected signal i_{inj} to the injection-locked oscillator output
$H_n(j \cdot \Delta\omega)$	Transfer function of the phase perturbations on the free-running oscillator signal i_{osc} to the injection-locked oscillator output
$h_n(t)$	Normalized impulse response of a resonant network
$H(s)$	Transfer function of a linear system or network
$h(t)$	Impulse response of a linear system or network
I	Unity matrix, symbol of electrical current, mechanical moment of inertia
I_A	Current amplitude through an inductor
I_b	Biasing current of an oscillator or an oscillator stage

I_{D0}	Technology dependent parameter determining the weak-inversion current of a MOS transistor
$i_{d,n}(t)$	Small-signal differential noise current
I_{ds}	Large-signal drain-source current of a MOS transistor
i_{ds}	Small-signal drain-source current of a MOS transistor
$I_{ds,f}$	Zero-temperature-coefficient DC biasing current of a transistor
$I_{ds,wi}$	Large-signal drain-source current of a MOS transistor in weak-inversion
$i_{inj}(t)$	Injected current in an oscillator
$I_{i,reg}$	Regulated output current of a current regulation circuit
$I_{i,reg,rep}$	Regulated output current through the oscillator replica when the regulator is loaded with a resistor
I_k	Fourier coefficient of a current oscillator signal
$\Im(x)$	The imaginary part of x
I_n	Amplitude of a noise current
$i_{n0}(t)$	Stationary current noise source
$i_n(t)$	Injected small-signal noise current
i_{osc}	Oscillator signal current
$i_r(t)$	Resulting current in an oscillator, sum of the injected current and the oscillator current
$I(s)$	Laplace transform of a current waveform
$i(t)$	Small-signal current
j	Imaginary unit, $\sqrt{-1}$
$j_{abs}(t = N \cdot \tau_{avg})$	Absolute jitter after N oscillation cycles
$J(d)$	Current density in a conductor, depending on the distance d from the surface
J	Joule, unit of energy
J_s	Current density in a conductor at the surface
k	The Boltzmann constant, approximately equal to $1.38\ \mathrm{m}^2 \cdot \mathrm{kg} \cdot \mathrm{s}^{-1} \cdot \mathrm{K}^{-1}$
k_{100}	Conversion gain of an envelope detector for an input signal with 100 % modulation depth
k_{30}	Conversion gain of an envelope detector for an input signal with 30 % modulation depth
k_{DC}	Conversion gain of an envelope detector for a DC (low-frequency) input signal
K_{fD}	Technology dependent $1/f$ noise fitting parameter of a diode
K_{fR}	Technology dependent $1/f$ noise fitting parameter of a resistor
K_{fT}	Technology dependent $1/f$ noise fitting parameter of a transistor
K_{ij}	Residue of a partial fraction corresponding to real pole i with j-th degree denominator

K_{ILO}	Injection-locked oscillator gain
K_{mix}	Mixing gain of a mixer circuit
K_{VCO}	Integration constant or sensitivity of a VCO to its control voltage v_c
L	Inductance, an inductor
L	Length of a MOS transistor
$\mathscr{L}(\Delta\omega)$	Phase noise density at frequency offset $\Delta\omega$, relative to the carrier
L_{ij}	Residue of a partial fraction corresponding to complex pole i with j-th degree denominator
$\mathscr{L}_{total}(\Delta\omega)$	Total noise power density at frequency offset $\Delta\omega$, relative to the carrier
MoI	Moment of Impact of a pulse applied to a resonant tank
MoI_N	Moment of Impact of a pulse applied to a resonant tank, normalized to $T_{LC}/2$
N	Number of free-running periods in a Pulsed-Harmonic oscillator
NF_{amp}	Noise figure of an amplifier
N_{LF}	Noise spectral density of the low-frequency noise at an amplifier output (expressed in V^2/Hz)
$N_{o,ED}$	Noise spectral density of the noise at the output of an envelope detector (expressed in V^2/Hz)
N_{src}	Noise spectral density of an input source (expressed in V^2/Hz)
p	Frequency of a single pole
p_i	Real i-th pole frequency
$P(s)$	Numerator of a transfer function $H(s)$
P_s	Average power dissipated in a resonant tank
$P_{sbc}(\Delta\omega)$	Single-sideband noise power at offset frequency $\Delta\omega$, relative to the carrier
$\mathscr{P}_{side}(f_0 + \Delta f, 1\text{ Hz})$	Single-sideband noise power in a 1 Hz interval at a frequency offset Δf from the carrier
PW	Pulse width of a pulse applied to a resonant tank
PW_N	Pulse width of a pulse applied to a resonant tank, normalized to $T_{LC}/2$
Q	Quality factor of a resonant (second order) network
q	Unit charge of a single charge carrier (electron or hole)
Q_C	Quality factor of a capacitor C
q_{Cte}	Maximum charge displacement (compared to equilibrium) in a resonant network with constant output amplitude during one period
q_{Decay}	Maximum charge displacement (compared to equilibrium) in a resonant network with exponentially decaying output amplitude during one period

Q_G	Generalized Q factor
Q_L	Quality factor of an inductor L
q_{max}	Maximum charge displacement from the equilibrium state on the output node of a resonant tank during one oscillation cycle
$Q(s)$	Denominator of a transfer function $H(s)$
R	Resistance, a resistor
r_0	Small signal output (drain) impedance of a MOS transistor (also called r_{ds})
R_B	Bulk resistance of a transistor
R_D	Drain resistance of a transistor
r_{ds}	Small signal output (drain) impedance of a MOS transistor (also called r_0)
R_{eff}	Effective noise resistance of a transistor
$\Re(x)$	The real part of x
R_G	Gate resistance of a transistor
R_p	Equivalent parallel resistance of an RLC network
R_S	Source resistance of a transistor
R_s	Series resistance of an inductor
s	Laplace variable, equal to $\sigma + j \cdot \omega$, in steady-state equal to $j \cdot \omega$
s	Second, unit of time
$S_{\phi,f}(f)$	Power Spectral Density of the phase fluctuations as a result of the $1/f$ noise component
$S_a(f)$	Power Spectral Density of a waveform a
$S_{i_n}(f)$	Power Spectral Density of a current noise source i_n
$S_{inj}(\omega)$	Power spectral density of the injected signal i_{inj}
$S_{nn}(\omega)$	Power spectral density of the free-running oscillator signal
$S_{osc}(\omega)$	Power spectral density of the locked oscillator signal i_{osc}
$S_{RF}(f)$	Power Spectral Density of a general RF signal
$S_{V_n}(f)$	Power Spectral Density of the voltage noise on a capacitor
$S_{v_n}(f)$	Power Spectral Density of a voltage noise source v_n
$S_x(f)$	Power Spectral Density of phase time fluctuations
$S_y(f)$	Power Spectral Density of fractional frequency fluctuations
$S_\phi(f)$	Power Spectral Density of phase fluctuations
$S_{\Delta f}(f)$	Power Spectral Density of frequency fluctuations
$S_{\Delta\omega}(f)$	Power Spectral Density of angular frequency fluctuations
T	Absolute temperature, expressed in Kelvin [K] or (depending on the context), the oscillation period
t	Time variable
T_0	Period of an oscillator
T_D	Delay of an oscillator stage
t_d	Delay of an inverter

T_h	Time span that a digital oscillator output is high during one period
$T_{h,0}$	Time span that a digital oscillator output is high during one period with a sensor input signal equal to zero
t_{hl}	Input-output delay of an amplifier for a falling edge at the output
$T_{i,reg}$	Loopgain of a current regulation circuit
T_l	Time span that a digital oscillator output is low during one period
t_L	Time needed for an injection-locked oscillator to lock, lock time of an injection-locked oscillator
$T_{l,0}$	Time span that a digital oscillator output is low during one period with a sensor input signal equal to zero
T_{LC}	Period of a free-running LC tank
t_{lh}	Input-output delay of an amplifier for a rising edge at the output
T_M	Motor torque
T_{Osc}	Complete period of a multi-stage oscillator
$T(s)$	Frequency dependent loopgain of a feedback system
T_{Sens}	Sensitivity of the output frequency f_0 to temperature
T_{Switch}	Time interval needed for a differential oscillator stage to switch
$T(t)$	Phase time
$T_{v,reg}$	Loopgain of a voltage regulation circuit
U	Symbol of electrical tension
$\mathbf{u_i}$	Eigenvector with corresponding eigenvalue λ_i
$u(t)$	The Heaviside function
V_A	Voltage amplitude over a capacitor
V_{bs}	Large-signal bulk-source voltage of a MOS transistor
v_{bs}	Small-signal bulk-source voltage of a MOS transistor
$v_c(t)$	Control voltage of a VCO
V_{Cte}	Constant input voltage
V_{ctrl}	Control voltage to control the gain of an amplifier
V_d	Differential voltage applied to the input of a differential pair
V_{dd}	Supply voltage
V_{ds}	Large-signal drain-source voltage of a MOS transistor
v_{ds}	Small-signal drain-source voltage of a MOS transistor
V_E	Early-voltage of a MOS transistor
V_{gs}	Large-signal gate-source voltage of a MOS transistor
v_{gs}	Small-signal gate-source voltage of a MOS transistor
$V_{gs,f}$	Zero-temperature-coefficient DC biasing voltage of a transistor
V_{gt}	Overdrive voltage of a MOS transistor, equal to $V_{gs} - V_{th}$
V_i	Output voltage of the i-th oscillator stage

$V_{i,reg}$	Regulated output voltage of a current regulation circuit
V_k	Fourier coefficient of a voltage oscillator signal
V_{max}	Maximum supply voltage at which a circuit can properly operate
v_{max}	Maximum output voltage (compared to equilibrium) of a resonant tank during one oscillation cycle
V_{min}	Minimum supply voltage at which a circuit can properly operate
$v_{n,diff}$	Differential noise voltage
$v_n(t)$	Small-signal noise voltage
V_{ref}	Output voltage of a voltage reference
V_{reg}	Output voltage of a voltage regulator
V_{rep}	Output biasing voltage coming from a replica circuit
$V(s)$	Laplace transform of a voltage waveform
V_S	Output voltage of a sensor, input voltage of a sensor interface
$V_{S,DC}$	DC value of the sensor output voltage
V_{Sens}	Sensitivity of the output frequency f_0 to the supply voltage
V_{S-}	Negative voltage output of a differential sensor
V_{S+}	Positive voltage output of a differential sensor
$v(t)$	Small-signal voltage
$v(t-\tau)$	Decay function of the excess amplitude
V_T	Threshold voltage of a relaxation oscillator
V_t	Thermal voltage, equal to $k \cdot T/q = 26$ mV at room temperature
V_{th}	Threshold voltage of a MOS transistor
V	Volt, unit of electrical tension
$V_{v,reg}$	Regulated output voltage of a voltage regulation circuit
$V_{v,reg,rep}$	Regulated output voltage over the oscillator replica when the regulator is loaded with a resistor
$V_{v,reg,res}$	Regulated output voltage of a voltage regulation circuit loaded with a resistor
W	Width of a MOS transistor
x	Normalized variable of the ISF $\Gamma(x)$, typically equal to $\omega_n \cdot t$
$\dot{x}_i$	Time-derivative of x_i
$x_i(t)$	A real-valued function of t
$x(t)$	Random instantaneous phase time variation, $\phi(t)/\omega_0$
$y(t)$	Instantaneous fractional frequency variation, $dx(t)/dt$
Z	Complex impedance
z	Scalar for which $z \in \mathbb{Z}$
Z_k	Impedance of a resonant network, seen by the k-th harmonic

Figures

Tables

Chapter 1
Introduction

The purpose of this work is to provide a comprehensive overview on timing issues and the development of timing references for Wireless Sensor Networks (WSN). The goal of this first chapter is to introduce the reader to the field of WSN. The issues faced to obtain a stable time reference are identified, which finally results in a motivation for this work.

This introduction starts with a historical overview of the evolution of wireless and chip technology in general. Both wireless data and energy transmission are addressed. Afterwards, the field of WSN is roughly sketched in Sect. 1.2 with a focus on the Pinballs platform, developed in the MICAS group at KU Leuven. From this discussion, the power and design constraints as well as the timing problems are derived. In Sect. 1.3 the motivation, the goals and an overview of this work are found.

1.1 Historical Introduction

A Wireless Sensor Network consists of a set of spatially distributed autonomous sensors [73, 314]. The size of this set can be fixed or can be changing dynamically, depending on the application. This will also have its repercussion on the network topology and power consumption of the different nodes. The function of a WSN is to monitor different environmental parameters such as temperature, position, pressure, humidity or force, collecting these data and transmitting it to a base station. Instead of only sensing the environmental data, the network can also be used to adaptively control or actuate some variables, for example the control of a heating system.

Most WSN nodes facilitate the possibility of wireless identification, often called Radio Frequency Identification or RFID. This means, by definition, that a contactless system using radio-frequency (RF) electromagnetic fields is used to transfer data from a tag, attached to an object, to the system [306]. In this way a wireless tag or an attached object can be identified. RFID tags can be passive, only reflecting modulated radio signals, or can have a small energy reservoir such as a battery or a capacitor. The very first RFID tag, named *The Thing* or *Great Seal bug*, was invented

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by the Soviet inventor Léon Theremin in the early 1940s as an espionage tool, see Fig. 1.1 [292]. Although this device does not allow remote identification as such, it modulates and reflects an incident wave in a similar way as modern, passive RFIDs.

★ Léon Theremin °1896–†1993
Lev Sergeyevich Termen (Лéв Сергéевич Тéрмен) was a Soviet and Russian inventor [290]. He is most famous for his invention of the *Theremin*, the first mass-produced electronic musical instrument. Apart from this, he was also the inventor of the predecessor of RFID technology [292]. After his return to the Soviet Union in 1938, Theremin was put to work in a sharashka (a secret laboratory in the Gulag camp system), together with Andrei Tupolev (Андреи Николаыевич Туполев, a Soviet aircraft designer) and other Soviet scientists. There he created the Buran eavesdropping system, a precursor of the modern laser microphone. The working principle was based on the reflection of infrared radiation to detect sound vibrations in glass windows from a distance. Another listening device he invented was called *The Thing*. In 1945 Soviet school children presented a replica of the Great Seal of the United States to the U.S. Ambassador as a gesture of friendship. This present, in which *The Thing* was disguised, hung in the ambassador's residential office and intercepted confidential conversations during the first 7 years of the cold war. In 1952 it was accidentally discovered and removed. For his work in Soviet espionage technology Theremin was awarded the Stalin Price.

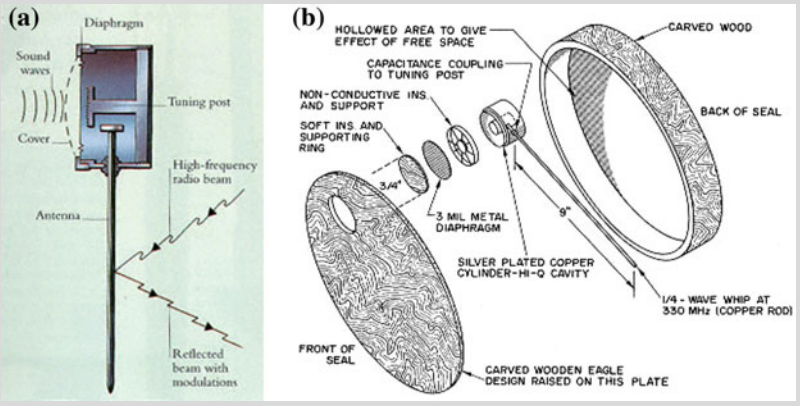

Fig. 1.1 a Schematic drawing of *The Thing*. The working principle is based on the reflection of an RF signal by the antenna. The load impedance of the antenna is changing as a function of the sound pressure. **b** *The Thing* was hidden in a replica of the Great Seal [292]

The use of RF waves for identification dates back to the same period, the start of the second world war. With the invention of the Radar by the German inventor Christian

Hülsmeyer in 1911, the first RF detection system was born [20]. The device was used to avoid collisions between ships in fog. Many scientists immediately recognized the incredibly high strategic value of such a device. As a result, in the 1934–1939 period eight nations independently developed similar systems to detect enemy airplanes from a considerable distance [289]. However, when warfare became more airborne, it was increasingly important to distinguish friends from foes [95]. Around 1939 the first 'identification friend or foe (IFF)' system was used; a transponder was installed in air fighters to 'answer' the radar pulses, facilitating wireless RF identification. The first Radio Frequency localization and Identification system, called *IFF Mark I*, was born [51].

1.1.1 Electromagnetic Transmission

Obviously, these early RFID systems are in no sense comparable to modern electronic systems. Due to the development and evolution of two main technologies, radio communication and electronic miniaturization, the economic interest in this kind of systems has increased drastically during the last decades. The evolution of both technologies goes hand in hand from the early beginning.

1.1.1.1 Wireless Energy Transmission

The very first experiments and developments in electromagnetism were done by Hans Christian Ørsted and Michael Faraday in 1821 [15]. Shortly after Ørsted discovered the electromagnetic interaction between a current conducting wire and a magnetic needle of a compass, different scientists attempted to build an electric motor. It was, however, Michael Faraday who succeeded firstly to cause an 'electromagnetic rotation' [304]. André-Marie Ampère in 1826 formalized these experiments in *Ampère's circuital law* describing the generation of the magnetic field around a current conducting wire. Another 5 years later, in 1831, Michael Faraday discovered the inverse law, describing the electromagnetic force induced in an inductor caused by a changing magnetic flux, see Fig. 1.2b. In the same period also Carl Friedrich Gauss was working on electromagnetism [297]. He defines two laws, one concerning electric fields, another describing magnetic fields. Around 1865 James Clerk Maxwell synthesized the previous observations, experiments and equations into a consistent theory. He translated Faraday's, Ampère's and Gauss's laws into a set of 4 differential equations (20 equations with 20 variables without using vector notation). This mathematical model not only describes the behavior of electromagnetic radiation but also forms the basis of the complete classical theory of electromagnetism [15, 313, 315].

The existence of this radiation was proven experimentally 13 years later by Heinrich Rudolf Hertz [313]. To do so, he built a spark-gap transmitter to generate electromagnetic waves. Nikola Tesla was the first looking for some practical

applications of electromagnetic waves [291, 300]. One of his main ideas was to use electromagnetic waves for wireless energy transmission. In this context he invented a device to efficiently generate RF currents [248]. 2 years later, he demonstrated the

★ Michael Faraday °1791–†1867
Michael Faraday was an English scientist who is considered as one of the co-founders of modern electronics [304]. His most famous discoveries are electromagnetic induction and electrolysis. He is a Fellow of the Royal Society (FRS). In 1821 he built a device to show electromagnetic rotation, nowadays known as a homopolar motor (Fig. 1.2a). The basin of mercury on the right acts as a conductor and contains a permanent magnet. By forcing a current through the vertical rod, it will start rotating around the magnet. The working principle was based on the discovery of electromagnetic force on moving charges, also called the Lorentz force, which was only formalized in 1891.

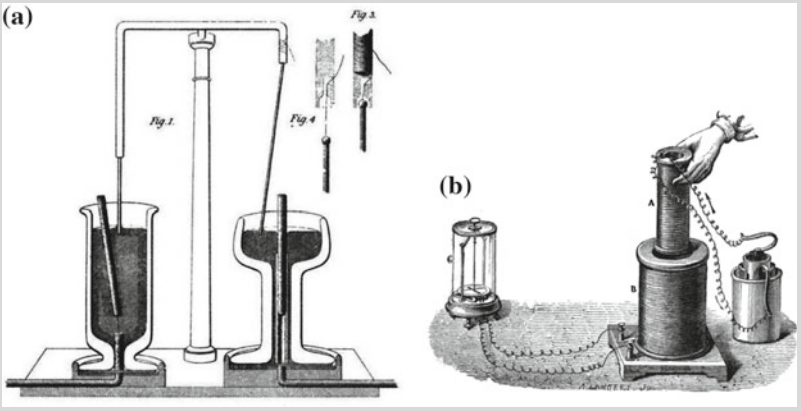

Fig. 1.2 a Schematic drawing on the electromagnetic rotation experiment or homopolar motor. **b** Schematic drawing of an induction experiment [304]

Ten years later, Michael Faraday discovered the generation of an electromagnetic force in an inductor caused by a changing magnetic flux. Although he proved this effect, called mutual induction, with different experiments (Fig. 1.2b), he did not realize that the induction ring he designed, would in 1836 be used by Nicholas Callan as the first voltage transformer [313]. By moving a small inductor A in or out of the large inductor B, the induced electromagnetic force causes a current, which is measured by a galvanometer.

wireless illumination of phosphorescent lamps at the World's Columbian Exposition in Chicago. That same year, in 1893, Nikola Tesla demonstrated publicly wireless

power transmission and also proposed the use of electromagnetic waves for signal transmission.

★ James Clerk Maxwell °1831–†1879
James Clerk Maxwell was a Scottish mathematician and physicist who is most famous for the formulation of the so-called Maxwell equations [315]. These equations, which describe the interaction between electric and magnetic fields, form the basis of the complete classical electromagnetic theory. He demonstrated that electric and magnetic fields travel through space as waves moving at the speed of light, which was a unification of light and electric phenomena and a first prediction of the existence of radio waves. Apart from this, he also contributed to the kinetic theory of gases by formulating the Maxwell-Boltzmann statistical distribution. His discoveries opened the door to the era of modern physics, laying the foundation for special relativity and quantum mechanics. Together with Albert Einstein and Isaac Newton he is considered to be one of the three most prominent physicists of all time (Fig. 1.3).

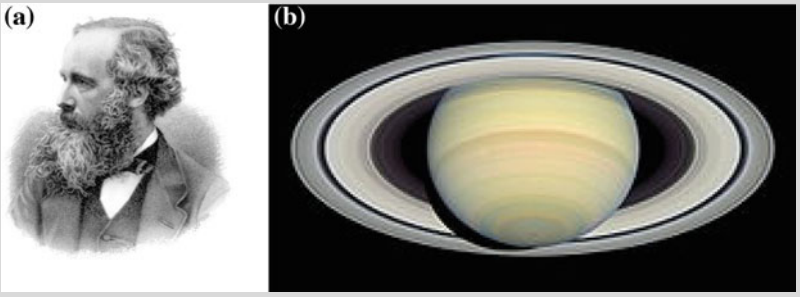

Fig. 1.3 James Clerk Maxwell proved mathematically that the rings of Saturn consist of numerous small particles [315]

In 1857 the topic of the Adams Prize was chosen to be the nature of the rings of Saturn. Maxwell devoted 2 years to studying the problem and proved that the rings must consist of numerous small particles he called *brick-bats*. A fluid ring would be forced by wave action to break into blobs, a solid ring also could not be stable. In 1859 he was awarded the Adams Prize for his essay *On the stability of Saturn's Rings*. Only in 1981 his predictions were confirmed by direct observations by the Voyager 1 space probe.

★ Nikola Tesla °1856–†1943
Nikola Tesla was a Serbian-American inventor, electrical and mechanical engineer and futurist [291]. He is most famous for his work on alternating current and wireless energy transmission. He was already working in a Serbian telephone company before immigrating in 1884 to the United States. There he started working for Thomas Edison. Soon, however, he set up his own laboratories and invented a wide variety of electrical instruments. Some of his patented inventions (induction motor and transformer) were licensed to Westinghouse which tried to develop a complete alternating current (AC) system. In his Wardenclyffe plant he tried to do trans-Atlantic energy transmission. He is seen as one of the greatest inventors of all time (Fig. 1.4).

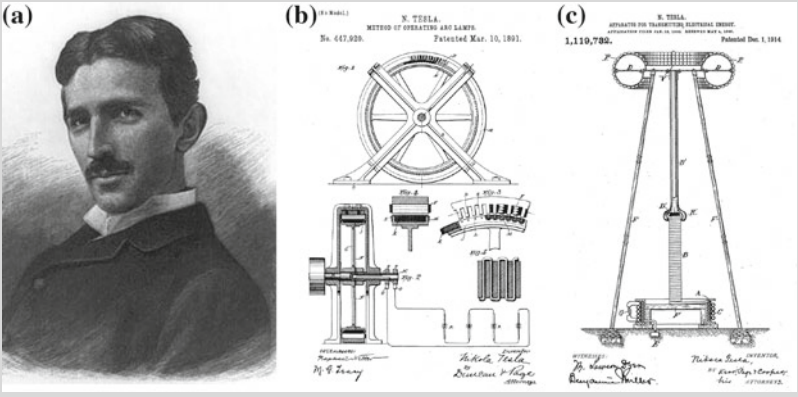

Fig. 1.4 Nikola Tesla aged 36 [291] and two of his patents, one for the efficient generation of RF power, a second for his Tesla transformer [248, 249]

1.1.1.2 This Rings a Bell

One year later, Jagdish Chandra Bose, an Indian scientist, succeeded to ring a bell from a distance [313]. He also showed that gun powder can be ignited from a distance. At this time neither the transistor nor the vacuum tube were invented; the first receivers made use of a *coherer* instead [86]. This device, which consisted of a glass tube with two contacts and filled with iron powder, acted as an RF-activated relay. When switched off, the coherer has a high impedance. Under influence of an RF wave coming from the antenna, small sparks appear between the iron particles, making them stick together. This causes a huge drop in series resistance, which switched on Bose's bell or another relay. If a small mechanical pulse is applied to the coherer, the iron particles lose their connection and the device is reset. One year later, the Italian scientist Guglielmo Marconi constructed a wireless link over 1.5 miles using a spark-gap transmitter and a coherer [298, 300, 309].

★ Guglielmo Marconi °1874–†1934
Guglielmo Marconi was an Italian physicist and inventor, known as the father of long-distance wireless transmission. He is often referred to as the inventor of radio and shared the 1909 Nobel Prize in Physics with Carl Ferdinant Braun. He was the inventor of the wireless telegraph. In order to improve the sensitivity of wireless receivers (which was necessary to facilitate long-distance wireless transmission), he invented a Magnetic Detector [298, 302]. The working principle is based on a rotating iron wire which is magnetized by two fixed magnets. The wire is continuously fed through 2 inductors. A first one is connected to the antenna. In case of an RF signal it magnetizes the iron wire. When this magnetized wire passes through the second inductor, which is connected to an ear phone, it causes a click, allowing telegraphy.

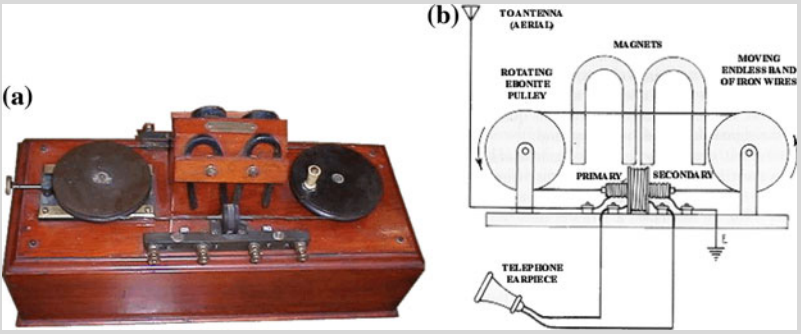

Fig. 1.5 a Photograph of Marconi's Magnetic Detector. **b** Schematic drawing of the Magnetic Detector [237, 302]

During the following years, Marconi as well as Tesla did experiments to transmit over larger distances. To improve the sensitivity at the receiver side, Marconi developed the *Maggie* or *Magnetic Detector*, see Fig. 1.5 [302]. This detector was an enormous step forward and proved the high engineering skills of Marconi. Although this device was used as the standard detector on shipboard receivers between 1902 and 1914, it took another 20 years before scientists were able to accurately understand the working principle [237].

The first semiconductor detector was developed around 1906 by Jagdish Chandra Bose and Greenleaf Whittier Pickard. This detector consisted of a metal needle which was put into contact with a crystal, often galena (Lead-Sulfide), creating a diode junction. This junction, nowadays known as a Schottky diode, created the ability to detect amplitude-modulated signals accurately. The device was often called a *crystal detector* or a *cat's whisker*, and was used in the first crystal radios [287]. It, however, did not make Marconi's detector obsolete due to its low robustness; every few days the junction needed to be re-established [86]. A photograph is shown in Fig. 1.6. At that time, the era of the vacuum tube still had to start.

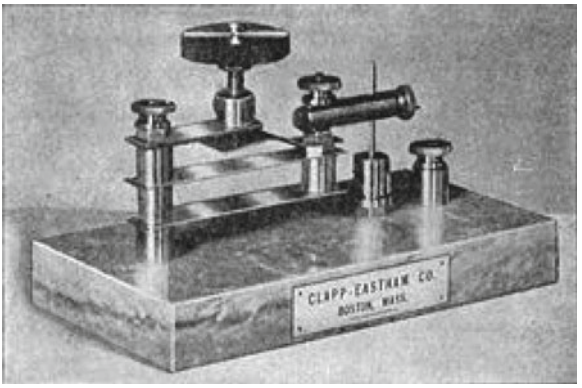

Fig. 1.6 Photograph of a crystal detector or cat's whisker. The metal-semiconductor junction which was created is nowadays known as a Schottky diode [287]

1.1.2 The Vacuum Tube

The phenomenon of *thermionic emission* was firstly reported by Frederick Guthrie around 1874 [293]. This effect was further investigated by Thomas Edison, who decided to patent his observations in 1884 without understanding the underlying physics. He also did not have any clue of the huge potential of this discovery, nowadays called the Edison effect. The English physicist John Ambrose Fleming developed the first rectifying vacuum tube, the *oscillation valve* or *Fleming valve*. This tube contained a heated filament, or cathode, which had thermionic emission of electrons that would flow to the anode. The electron current could therefore only flow in one direction, from cathode to anode. The device was used as a rectifier and greatly improved the *cat's whisker*. The main reason was its immunity to external vibrations, which made it superior on shipboard duty. On navy ships the shock of weapon fire commonly shook the sensitive galena off its sensitive point. It was only in the 1960s that they were replaced by silicon rectifiers.

Originally, vacuum tubes were only used for rectification, not amplification. In 1906, Robert von Lieben, an Austrian scientist, filed a patent for a cathode ray tube using magnetic deflection. This tube was intended for telephony and could be used for the amplification of audio signals. The real triode tube was invented by Lee de Forest by adding a grid between the cathode and the anode of his previously invented Audion rectifier tube, patented in 1907 [293]. At this moment 3 different detector technologies for radio reception were available. For example, all of them were present on the RMS Titanic.

★ The RMS Titanic †1912

At the time the RMS Titanic was built, three technologies were available for on-board radio reception [86]. All three of them were available at the Titanic. The first was the Maggie Detector, which was obliged on every ship. Although one needed to have some experience to operate this device, it had a huge benefit of robustness. The second technology was the cat's whisker, which was easier to operate and more sensitive. Its drawback was the sensitivity to vibrations, which made it useless in case of emergencies. The third technology was the Fleming valve detector, with its superior sensitivity.

Other ships from that time period were only equipped with the Maggie detector. At the time the Titanic was transmitting its emergency signals (CQD, calling all operators, distress), the ship closest by was the SS Californian. Although an officer was present in the radio room while the radio operator was sleeping, he simply was not able to operate the complex Maggie detector and therefore could not receive any signals. Afterwards this officer blamed himself for the fact the SS Californian was not able to help the sinking RMS Titanic (Fig. 1.7).

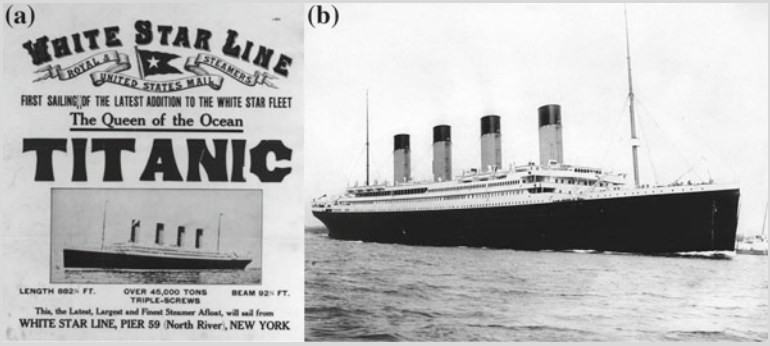

Fig. 1.7 The RMS Titanic was believed to be unsinkable [308]

With the invention of the triode vacuum tube, also at the transmitter side improvements could be made. The development of Amplitude Modulation (AM) made the replacement of spark-gap transmitters possible [294]. As opposed to spark-gap transmitters that covered the entire bandwidth of spectra, AM transmission allows that different channels in the same frequency band can be used at the same time. The invention of the regenerative circuit by Edwin Howard Armstrong in 1914, enabled the proper reception of AM signals [307]. This circuit, which delivered a high gain out of one single vacuum tube, drastically improved the sensitivity of the receiver. A single triode vacuum tube served as a gain element as well as a detector. Spark-gap telegraphy was completely stopped in 1920 [311]. The regenerative circuit was cheap and was therefore heavily used until the second world war.

★ Edwin Howard Armstrong °1890–†1954
Edwin Howard Armstrong was an American electrical engineer and inventor. He was the inventor of the regenerative circuit or autodyne receiver (1914), the super heterodyne receiver (1918) and FM modulation (1935). He is often referred to as the most productive and influential inventor of radio history [296]. A schematic of the autodyne receiver is shown in Fig. 1.8. The working principle is based on the fact that the input signal is amplified several times by the same amplifying element, in this case a vacuum tube. This is done by feeding back a small part of the output to the input by a Tickler coil. The feedback gain can be controlled to prevent the circuit against instability or, oppositely, to make it unstable. To receive an AM signal, the amplifier is tuned close to instability. The benefit of the circuit is now that the gain of the amplifier is very high only around the desired carrier frequency, tuned by the input filter. When a Morse signal is received (carrier on-off keying), the amplifier is used as an oscillator (unstable feedback) and tuned slightly at one side of the input carrier frequency. In this way the carrier is mixed with the oscillator frequency and the Morse signal is demodulated to a 'beep' in the audio output. Also single-sideband signals can be received, using the circuit as an oscillator. In this case the oscillator signal acts as the missing carrier which is needed for demodulation. In all cases the triode vacuum tube is used as an amplifier as well as a demodulator or detector of the RF signal. The most important drawback of this circuit is the leakage of the feedback signal to the antenna.

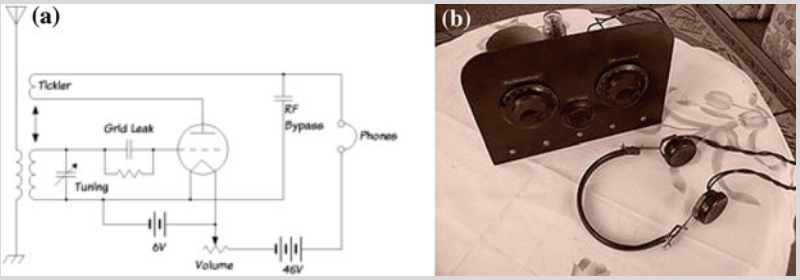

Fig. 1.8 Schematic of the autodyne or regenerative receiver. The photo *on the right* shows the simplicity of this circuit [307]

Vacuum tubes were also used for digital computers. The problem here, however, was their high cost and low reliability. The first electronic computer, called *ENIAC*, was built in 1947 and consisted of 17,468 vacuum tubes. When continuously switched on, on average every two days a vacuum tube was broken. It took over 15 minutes to repair this. The *ENIAC* consumed around 150 kW of power and did around 5,000 operations on 10-bit numbers or 386 multiplications each second [288].

1.1.3 The Invention of the Transistor

The first real step towards the scaling of all electronic devices came with the invention of the transistor. In 1925, the Austrian-Hungarian physicist Julius Edgar Lilienfeld filed the first patent for the field-effect transistor principle [160, 161]. Unfortunately, no evidence exists that this device was ever built. However, later work in the 1990s shows that one of Lilienfeld's designs worked and delivered substantial gain. The real invention and commercial usage of the transistor emerged from efforts to produce extremely pure germanium mixer diodes for use in microwave radar units during the war.

★ The Junction Field-Effect Transistor—JFET

The Junction Field-Effect Transistor or JFET was already predicted and patented around 1925 by Julius Lilienfeld. It was, however, impossible to produce this device for many years. The attempts to do so ended in the invention of the first point-contact transistor and BJT. After that, it still took several decades before the first practical JFETs were successfully produced.

A cross section of an idealized JFET is shown in Fig. 1.9. The main difference compared to the BJT is that the JFET is voltage controlled instead of current controlled. By applying a voltage to the gate, the *pn* junction between the gate and the channel is reversely biased and majority carriers in the channel are displaced. This effect, which is shown in grey on Fig. 1.9, will narrow down and at a certain voltage even pinch off the channel at the pinch-off voltage V_P. In this way, the JFET can be used as an amplifying device. Note that no current is drawn through the gate. When V_{DS} is low compared to $V_{GS} - V_P$, the JFET behaves as a voltage-controlled resistor. For a higher V_{DS}, the JFET behaves more as a current source. This is comparable to the behavior of other field-effect transistors (FET). For a more detailed description, see [97].

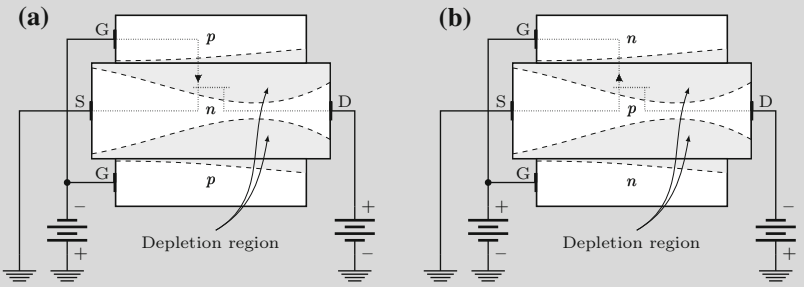

Fig. 1.9 Idealized cross-section of an *n*-channel (*left*) and *p*-channel (*right*) JFET. By reversely biasing the *pn* junction at the gate, the conducting channel is pinched off [97]

At Bell labs, William Shockley, John Bardeen and Walter Brattain tried to design a similar device as was predicted by Lilienfeld with the functionality of a triode [299]. During their experiments to control the current through a semiconductor crystal using

a third connection, Bardeen and Brattain discovered that the key to implement this was putting the input and output contacts very close to each other. When trying to build this, they obtained a device which could amplify an input signal towards its output. William Shockley immediately understood the high potential of this device, the first point-contact transistor. In 1956, the three shared the Nobel Prize in Physics for their invention.

★ The Bipolar Junction Transistor—BJT

The bipolar junction transistor (BJT) is probably the oldest transistor topology which is still commonly used. Two different polarities exist of the BJT, the *npn* and *pnp* BJT, based on the doping of the used semiconductor layers. A BJT has three terminals, base, emitter and collector.

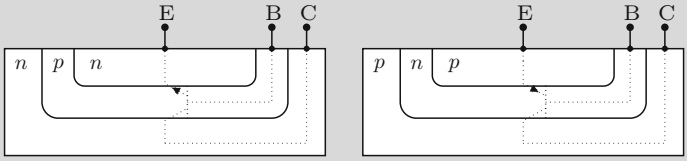

Fig. 1.10 Cross section of a typical *npn* (*left*) and *pnp* (*right*) transistor structure

The working principle of the BJT can be understood by taking a look at the cross section on Fig. 1.10. When a positive voltage is applied between the base and the emitter, the base-emitter *pn* junction will be positively biased and a current will flow from the base to the emitter. At the same moment, the emitter will inject some minority carriers (electrons in this case) into the base region which are attracted and collected by the collector. This causes a current flowing from the collector to the emitter. When the base region is small, most injected carriers are captured by the collector. The collector-emitter current will in this case be many times higher than the base-emitter current. The relation between both currents is then given by:

$$I_C = \beta \cdot I_B \tag{1.1}$$

where β is the current gain of the bipolar transistor. If an input voltage is applied at the input, the base-emitter junction behaves as a diode and the current through this junction is equal to:

$$I_B = I_S \cdot \left(e^{\left(\frac{V_{BE}}{nV_t}\right)} - 1 \right) \tag{1.2}$$

where I_S is the saturation current, $V_t = kT/q$ is called the thermal voltage, equal to 26 mV at room temperature, and n is the ideality factor, somewhere in between 1 and 2. This indicates that the bipolar transistor is a current-steered

device. Even when the BJT is used as a static switch, a constant current is flowing through the base-emitter junction. This is an important drawback of the BJT in integrated circuits, especially for low-power and for highly-integrated circuits.

Bell Labs immediately put this transistor in production. During the following years the first transistor radios were demonstrated. They, however, never made it towards production due to the low reliability of the point-contact transistor. The contacts to the germanium crystal were fragile and they were sensitive to moisture. In 1950, William Shockley developed a totally new type of transistor, called the bipolar junction transistor (BJT). It is this transistor which is nowadays referred to as a standard transistor [299].

The first all-transistor radio, the TR-1, was announced on October 18, 1954 and put on sale in November 1954 for $49.95 (the equivalent of about $361 in year-2005 dollars) [312]. About 150,000 units were sold of this device, which contained four Texas Instruments NPN transistors. The TR-1 had to be powered by a 22.5 V battery, which made it very expensive in use. It was far more popular due to its novelty than for its actual performance. In 1957 Sony launched their first transistor radio, the TR-63, which was small enough to fit in a pocket and was powered by a small battery. Between 1960 and 1980, transistors displaced tubes almost completely, except in high-power or high-frequency applications.

★ The Metal-Oxide-Semiconductor Field-Effect Transistor—MOSFET
The Metal-Oxide-Semiconductor Field-Effect Transistor or MOSFET was invented in 1959 by Dawon Kahng and Martin Atalla at Bell Labs as an offshoot to the patented FET design [122, 161]. The MOSFET was fundamentally different from the BJT and the JFET in the sense that it made use of a thermally grown oxide as an insulating layer separating the gate and the conducting channel. On top of that, a metallic gate electrode was placed. Earlier field-effect transistors making use of a deposited insulating layer suffered strongly from the trapping and scattering of carriers at the semiconductor-insulator interface which impeded their performance. Using the native semiconductor oxide instead, appeared to be the solution to these problems [9]. Similar to other transistors, two MOSFET polarities exist, called NMOS and PMOS transistors. A simplified structure is shown in Fig. 1.11.

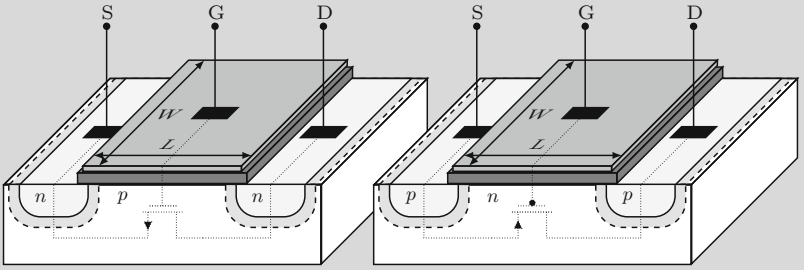

Fig. 1.11 Cross-section of an NMOS (*left*) and PMOS (*right*) transistor. Even in unbiased condition a depletion region is present surrounding the source and drain doping implant

Following the development of clean rooms and photo lithography and due to the planar structure, the Si–SiO_2 system possessed technical attractions such as low cost of production and ease of integration. Additionally, the method of coupling two complementary MOSFETs (P-channel and N-channel) into one high/low switch, known as CMOS, means that digital circuits dissipate very little power except when actually switched. Largely because of these three factors, the MOSFET has become the most widely used type of transistor in integrated circuits.

1.1.3.1 Making More for Less

The integrated circuit was independently invented by two separate inventors at nearly the same time [16]. Both engineers, Jack Kilby (Texas Instruments) and Robert Noyce (Fairchild Semiconductor), were working at the same problem: how to make more for less? The main reason for their research was the observation that improving the performance of a discrete-component digital computer almost automatically implies that the number of components increases drastically, hence increasing cost. To overcome this drawback, both inventors tried to implement a complete circuit consisting of different components and their interconnect on the same piece of semiconductor. Jack Kilby used germanium, Robert Noyce was using silicon.

Although both engineers in 1959 applied for a patent, Jack Kilby is generally recognized as the inventor of the integrated circuit [129]. The circuit, which was implemented on a piece of crystalline germanium, is shown in Fig. 1.12 [130]. In 1961 Fairchild Semiconductor launched the first commercially available integrated circuits. Instead of using individual transistors, all computers now started to be made using chips. Texas Instruments used the first chips in Air Force Computers in 1962. Somewhat later chips were also used in portable calculators; quite remarkably, this was also an invention of Jack Kilby (1967).

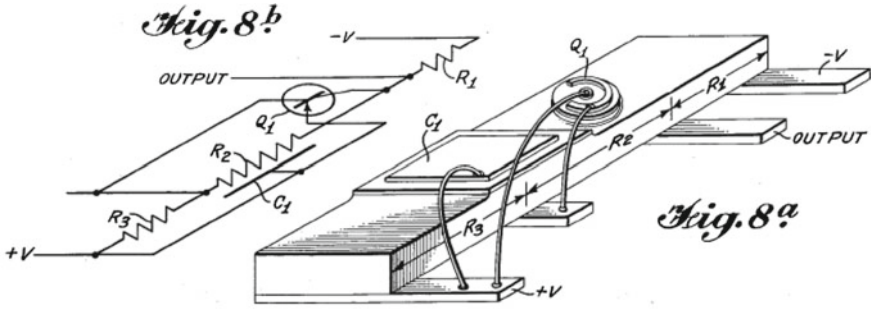

Fig. 1.12 One of the illustrations of Kilby's patent No. 3261081. This device is considered to be the first integrated circuit [130]

★ Moore's Law—19 April 1965
In the 19 April 1965 issue of Electronics magazine, Gordon E. Moore had been asked to predict what would happen over the next 10 years in the semiconductor industry. In his article he dreamed of the integration of 65,000 components on a single 6 mm^2 silicon die. He based his forecast on a log-linear plot of the first planar transistor IC in 1959 to a 32- and 64-transistor chip in 1964 and 1965 respectively. "The complexity for minimum component costs has increased at a rate of roughly a factor of two per year. Certainly over the short term this rate can be expected to continue, if not to increase. Over the long term, the rate of increase is a bit more uncertain, although there is no reason to believe it will not remain constant for at least 10 years." 10 years later, when he was president and CEO of Intel, he revisited this forecast: a memory with a 65,000-transistor density was in production at Intel [222].

Jack Kilby received the 2000 Nobel prize in Physics for his co-invention of the integrated circuit [301]. Robert Noyce co-founded Intel, the company responsible for the invention of the microprocessor (the Intel 4004) in 1968, together with Gordon Moore and Andrew Grove. For Noyce and Kilby, the invention of the integrated circuit is one of the most important innovations of mankind: today all electronic products use IC technology. Jack Kilby told about this: "*What we didn't realize then was that the integrated circuit would reduce the cost of electronic functions by a factor of a million to one, nothing had ever done that for anything before*" [16]. With this invention, the era of scaling was ready to start: while the first IC was about the size of an adult's pinkie finger and had only one transistor, three resistors and one capacitor, an IC today can contain over 2 billion transistors. In Fig. 1.13 the evolution of the number of calculations per second for an investment of $1,000 is shown over the years, from the early beginning of electronics industry an exponential growth is observed.

The driving force behind the ever increasing integration, is the resulting cost and power reduction. When a circuit can completely be produced as an IC, without any (or with less) external components, the production cost is decreased drastically. Especially for high-frequency applications (for which small passives are needed), integration and miniaturization can provide a cost as well as a power benefit. This opens the possibility to make technologies such as WiFi, GPS and GSM radios available in almost every portable device. Software-defined radios are coming into the picture quickly and form the currently highest possible level of integration, i.e. all wireless technologies and functions are available in the same chip package [255].

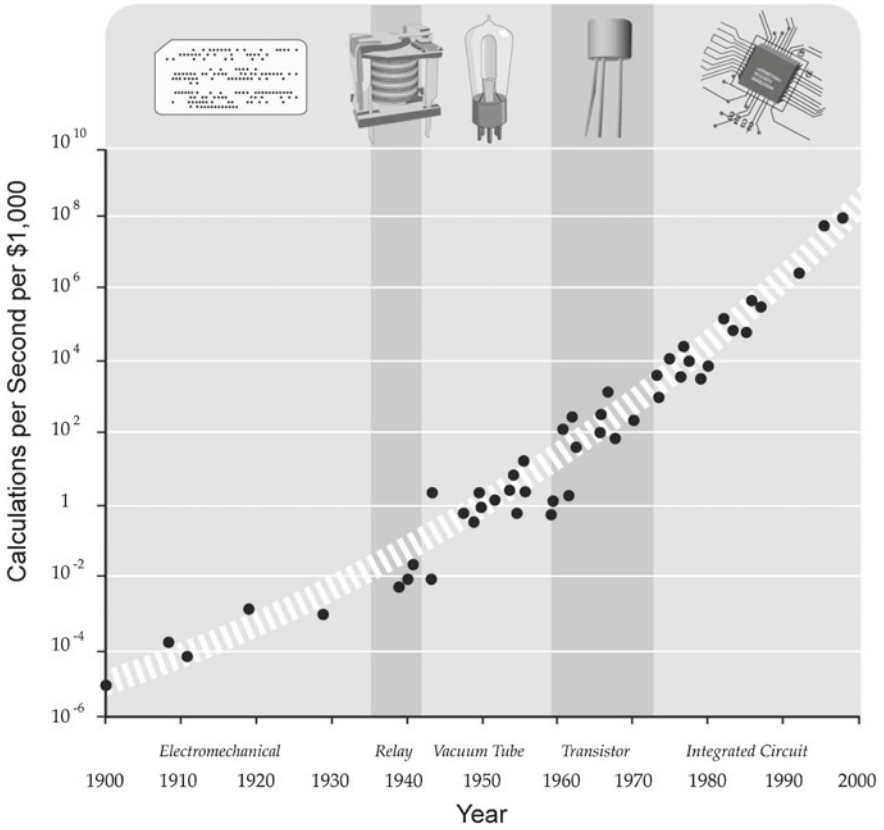

Fig. 1.13 Logarithmic plot of the number of calculations per second per $1,000. From the early beginning, this curve increases exponentially [233]

1.2 Wireless Sensor Networks

Due to the scaling and therefore the ever increasing functionality of single-chip devices, RFIDs and wireless sensor nodes will be increasingly complex and able to perform difficult tasks. Although the higher level of integration poses several accuracy problems for analog circuitry, it is the only way to make RFID technology an affordable and therefore a promising and feasible technology [66, 215]. Moreover, when talking about wirelessly powered devices, an ultra-low power (ULP) consumption is of great importance [51, 52]. In [107, 206] it is stated that the gate capacitance of a switching device decreases linearly with the minimum gate length. This results in a decrease of the power consumption for doing the same operations in a scaled technology. It is, however, also shown that the role of the interconnect and gate leakage and channel leakage in the active devices becomes dominant, which increases the static power consumption dramatically [115]. Alternative transistor topologies, and the use of high-k gate materials try to reverse this performance decrease in future IC generations [132, 235, 240]. Moreover, an increasing number of foundries offer technology nodes with sub-nodes for low-power design. In [111] it is shown that these low-power nodes facilitate the production of ULP sensor nodes in deep-submicron CMOS. Typically, in return for a decreased leakage power, these technologies have a higher V_{th} and decreased mobility, resulting in slower transistor-behavior.

Another concern is the ever increasing cost of the next technology generation; due to the advanced lithography techniques as well as the increasing number of chemicals and materials needed [8]. The only way to overcome this is by economies of scale: the increasing fixed cost asks for an increasing number of chips sold. Therefore, an increasing market penetration is crucial for further developments in RFID technology [241].

1.2.1 RFID Adoption

Since many years, forecasts are made on the adoption of WSNs and RFIDs in our daily environment [24, 66]. Making use of this technology, in 2012 over 15 billion devices were connected, directly or indirectly to the Internet of Things (IoT), whereas this number was around 4 billion in 2010. Since RFID devices are needed to communicate with objects, it is believed that this number will increase further exponentially up to 50 billion in 2020 [24, 276]. Everyday new applications of WSN and RFIDs are identified [159]. In [221], the evolution of RFIDs is compared to that of the bar code. Although the bar code increased the sales with 10–12 % due to an increased counting efficiency, RFIDs can be far more significant in the value chain. The accuracy of inventory can be increased to 99.5 %, whereas nowadays this drops often down below 75 %. RFIDs are applicable in almost every market since they can avoid order problems, out of stocks, mishandled luggage, wrong medication, tracking the cold chain of food, etc. This drastically improves the total efficiency, productivity, cost

and accuracy. This makes the adoption of RFIDs in our daily environment and their connection to the IoT to create an intelligent and responsive world, an unstoppable process [66, 145, 221, 276].

1.2.2 Challenges in RFID Design

Many challenges exist in the further development of RFIDs [318]. Examples are (improved) standards and patents to create a unified, affordable, infrastructure, regulatory issues, cost-related issues, etc. Apart from this, also the technological requirements for RFID systems can be very diverse. Specifications such as the form factor, mechanical robustness, dust and moisture protection are in most applications equally important as the radio range and the energy consumption [51, 66]. In this PhD thesis, a few of these challenges are addressed. As will be seen, however, to keep track of the global picture and to identify the main technological challenges, the Pinballs framework was set up.[1]

1.2.3 The Pinballs Framework

The Pinballs system was developed to deliver a low-power platform to industry for automated product identification, localization and monitoring [51, 66]. Typically envisioned applications of this platform include:

- A tracking system for books in a library. When every book in a library is equipped with a small wireless device, they are not only protected against theft but misplaced books can also be resolved easily by requesting the location of a certain device on a central computer. Since providing a battery in every book is an impossible quest (moreover because these batteries need to be changed or charged every once in a while), a battery-less device is preferred for this application.
- Tracking of goods in a warehouse and protecting the cold chain. Similar to the previous application, by using localization techniques, this greatly reduces the effort needed for stock management. Here, depending on the size of the food packages, devices can be equipped with a small battery to prevent blind spots in the measured temperature data. When every bottle of shampoo needs to be equipped with a tag, wirelessly powered systems are preferred.
- Safety issues on production floors. When objects and persons can be located within a factory mall, a central computer or an operator can detect possible hazards. With the tag localization technology, it is easy to bridge the gap towards a wireless warning system.
- Measuring of data on moving objects. Even within a machine, the wear-out of some parts can be interesting to measure proactively. Often these parts are rotating

[1] Pinballs was the name of the IWT-SBO project on ULP WSN circuits.

or on unreachable locations, which makes a wired measurement impossible. A single-chip wireless sensor can then provide a suitable solution.

To address all such applications, a 3-layer wireless sensor network architecture has been developed [156, 158].

1.2.3.1 Network System Overview

To increase the flexibility of the platform, the Pinballs system in the general sense consists of 3 hierarchical system layers. The difference between these layers is mainly in the energy needs and consequently also their functionality in the network. In Fig. 1.14 a schematic overview of the different layers is shown. As a result of the energy constraints in the different levels, the system is designed to push the functionality and complexity as much as possible upwards on the hierarchical ladder [51, 157]. Note that this model corresponds well to the swarm model of Jan Rabaey [205].

The lowest level in the network are the wirelessly powered tags. These tags scavenge energy (RF energy in the case of the Pinballs project) to charge a small on-board energy reservoir and are considered to be pin-less chips without any external components. The only functionality here is the possibility to measure and possibly process a physical quantity which is transmitted to the hubs together with some identification data. The wireless protocol used is pulsed ultra-wideband (P-UWB) (also called Impulse Radio Ultra-Wideband, IR-UWB). As shown in [271], this protocol can be implemented using a very basic end therefore low-power transmitter topology; in return, the corresponding receiver is a much more complex system [274]. This is

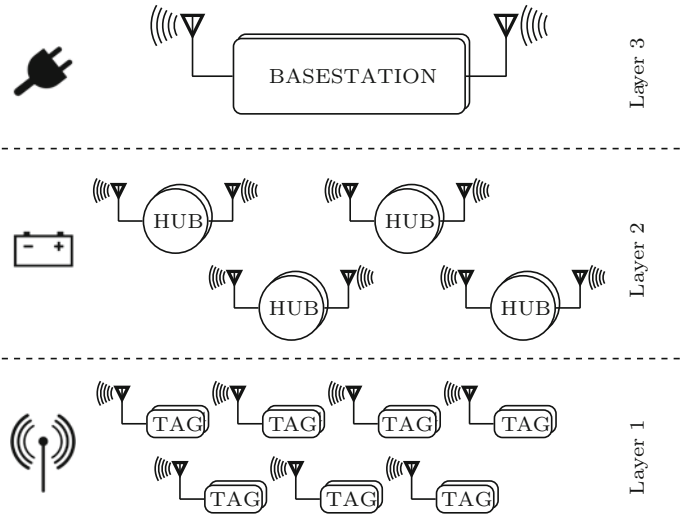

Fig. 1.14 System overview of the three hierarchical layers in the Pinballs platform

important to reduce the complexity and power consumption in the tag as much as possible, especially in case of unidirectional links only. Another benefit of using UWB pulses is the possibility of measuring an accurate time of arrival, which facilitates localization, i.e. the large frequency bandwidth results in a high time resolution.

The data from the tags are received in the second level, called the HUBs. These HUBs are battery powered and receive data from all tags within their range. By correlating a template of the UWB pulses to the received signal, the pulses can be discovered, even under the noise floor. To increase the sensitivity of the receiver (for a given bit error rate), a scrambling code is multiplied with the transmitted bits, representing each bit by several pulses. These codes can also be used to make a difference between the tags or to recover data from collisions by using orthogonal codes [156]. At reception, also a time stamp is added to each data package, which is afterwards transmitted to the base station where it is compared with other time stamps of the same package. From the moment four different HUBs receive the same UWB data burst, the transmitting tag can be located in a relative sense compared to the HUBs by solving the inverse GPS equations triangulation [158]. If desired, also HUBs can be loaded with more complex measuring systems, with an increased power consumption compared to the tags. Note that the energy availability is limited, even when a battery is used. Although the number of HUBs in the system is much lower than tags, it is still a costly operation to change batteries too often. Therefore, also here, low-power design is required to increase the battery lifetime as much as possible.[2]

The highest level is the base station, which can best be compared to a mains-powered computer or server. Here, all information collected by the tags and HUBs is gathered. Using the timing information, the location of the different tags and/or HUBs can be resolved.[3] Furthermore the data can be saved, analyzed or connected to the so-called internet of things (IoT).

In this work, the focus is on the lowest level, the tags, requiring the highest level of integration and the lowest power consumption. This results in several design challenges.

1.2.3.2 Challenges in the Pinballs Framework

From the system design of the Pinballs framework, different design challenges can already be identified. Here, the main items related to the tag design are listed. They will all have an impact on the system design of the wireless tag, as discussed further on.

- Since the tag is a completely integrated system with no external battery, scavenging is used as a power supply. In the case of the Pinballs platform this is RF energy

[2] The goal is to have a 6 to 12 months autonomy with a single AA battery [273].

[3] Note that in most cases also some extra information can be used such as an approximate or previous location to unveil the location unambiguously. Also the time stamp of a fifth or more HUBs can be used, resulting in a least-squares optimization problem.

scavenging. This results in an extremely low power source (1–5 nW) of which the output energy needs to be accumulated for several minutes before any operation can be performed [51]. In [243] different other energy harvesting methods are discussed. It appears that RF energy is one of the most limited energy sources compared to others such as solar, wind, breathing, vibrations, body heat, etc.

- The size of the available on-chip energy reservoirs is extremely limited. The goal is to use a 100 nF capacitor, which can be charged to around 1 V, containing 50 nJ of energy. This results in a typical charge and discharge cycle, shown in Fig. 1.15. The circuits therefore need to work over a very wide supply range (if no power-hungry regulator is used). Moreover, the capacitor will only be discharged down to the minimum voltage over which the circuitry can operate V_{min}, putting a maximum to the amount of energy on the capacitor that effectively can be used.
- Since the tags can be positioned in very diverse and harsh environments, apart from supply-voltage dependency, also robustness against temperature changes is an important specification.
- Network coordination is a major issue. Since over hundreds or thousands of tags can be present in the same room, a methodology is needed to avoid data collisions [66]. This has been investigated in [156]. In [51] different extremely low power (ELP) circuits are studied to generate random time offsets, to detect the voltage threshold level on the capacitor and to receive data pulses in the RF power signals.
- Energy in both the bottom and middle layer is very limited. Low-power electronic design and a high level of power management are therefore crucial.
- Timing of the UWB pulses. The pulse width of the transmitted pulses is 1.5–3 ns; one pulse every 30 ns. This means that, when the receiver discovers the first pulse (by correlating the received waveform at different time offsets with the pulse template), it makes an estimate of the position of the next pulse. When the frequency offset in the transmitter is too high, the receiver cannot compensate this, resulting in data loss. In the Pinballs receiver design presented in [261, 273], an absolute accuracy of around 1 % is required between different bursts, and a clock deviation below ± 0.01 % is required within one data burst.
- Measuring a physical quantity under changing temperature and supply voltage conditions is needed. Different topologies using the relative rather than the absolute accuracy of electrical and time-based quantities to obtain accurate measurements are presented in [43, 263].
- Especially the tags need to be extremely cheap when manufactured in large quantities. This drastically limits the possibility of using external components as well as trimming. Absolute accuracy or self-calibrating circuits are therefore a must.

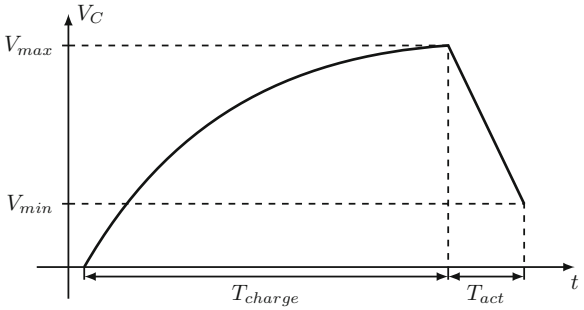

Fig. 1.15 Typical charge and discharge characteristic of the supply curve on an RFID tag. Most often the scavenging mechanism is rather slow, which results in a T_{charge} in the order of minutes. Depending on the load current and the size of the capacitor, T_{act} typically varies between 1 ms and several seconds. The higher V_{max} and the lower V_{min}, the longer the tag circuitry can be active without interruptions (one burst operation)

★ The use of an on-chip DC–DC Converter

One possibility to overcome the unstable supply voltage on a wireless tag, is using an on-chip DC–DC converter. To do so, two common topologies exist: inductive converters and capacitive converters. As shown in [284], as a result of their low efficiency in the low-power range, inductor-based converters are mainly suitable for high-power applications (typically in the order of a few hundreds of milliwatts). Capacitive converters on the other hand can also reach a high efficiency (or EEF) at lower output powers. The efficiency typically is around 80–85 % for a load of around 100 µW in their optimal operating point [260]. However, when the voltage conversion ratio changes as a result of the decreasing input voltage (Fig. 1.15), the efficiency drops quickly. Moreover, a more complex control circuit and switching scheme is needed to adapt the conversion ratio (so-called gearboxing), which is a severe drawback of capacitor-based converters, certainly in ultra-low-power applications. Apart from this, switched converters generate switching noise and have a ripple on their output voltage. Evidently, these noise sources have a negative impact on the other circuitry on the tag. Since the focus of this work is on sub-100 µW oscillators, the use of DC–DC converters is not further investigated. In Chap. 5 a linear regulator is used to overcome the supply voltage change, in Chap. 6 a supply voltage resilient oscillator topology is developed.

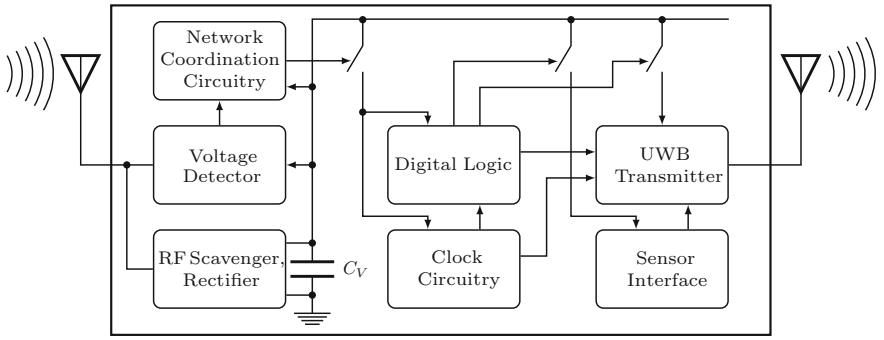

Fig. 1.16 Architecture of a wireless RF-powered tag

1.2.4 Architecture of an RFID Tag

The architecture of the proposed wireless tag is shown in Fig. 1.16. On the left hand side the RF scavenging antenna is seen, which can be either an on-chip or an off-chip antenna. The three blocks on the left are responsible for the energy harvesting and the detection if enough energy is available and whether the tag can be switched on. These blocks are elaborately discussed in [51] and are out of the scope of this thesis.

The other four blocks are important at the moment the tag is active. When a burst starts, the digital logic and the clock are switched on by the Network Coordination Circuitry after initiating the different other blocks; the digital logic will decide when the transmitter and the sensor interface need to be switched on. Since both blocks are power hungry, they only need to be active when they are used effectively. Typically, a data burst contains four steps: initiation, transmission of the preamble, transmission of the data (tag-ID), transmission of the measured sensor value. The transfer between these steps as well as the scrambling of the data is performed by the digital logic. Before starting a burst, one has to make sure that sufficient energy is available to complete all of the requested operations.

1.2.4.1 The UWB Transmitter

The ultra-wideband transmitter is the most essential block of the tag. Without this transmitter no uplink is available and there is no way of transferring information towards the HUBs or base station. As previously mentioned, an IR-UWB protocol is used. Different transmitter topologies are available, depending on the used frequency band [13, 183]. The receiver designed in the Pinballs project has a front-end designed for the lower band, 0–960 MHz [261, 273]. A low-band UWB transmitter typically consists of a pulse generator and an antenna front-end. To make sure that the pulses are transmitted at the correct frequency, to assure a proper reception of the transmitted data burst, an accurate clock reference is needed. The spectrum of the pulses itself

is mostly controlled by the pulse generator and/or front-end circuit. In this PhD, the main focus is on timing issues, however, in Chap. 9 the design of an integrated pulse generator itself is briefly discussed.

1.2.4.2 The Sensor Interface

The sensor interface and the sensor on the tag are needed to gain some information from the environment. This can be a physical quantity, such as local temperature, pressure, humidity, but also the presence of a person, sunlight or movement. In most cases the sensor interface converts an analog sensor signal into a digital number. In literature, different solutions can be found to implement this conversion [43]. Here, only time-based solutions are discussed. The sensor interface of the tag is also connected to the supply rail. Therefore, it needs to be robust against temperature as well as supply voltage variations. The use of a voltage regulator is avoided for energy reasons and, as explained in Chap. 5 and especially for low-power regulators, have an impact on the circuitry due to their limited output resistance. Instead of using the absolute frequency accuracy of an oscillator [268], the relative frequency or time deviations can be used to increase the process, voltage and temperature (PVT) independence. This can be the frequency difference between two oscillators or two delay lines [43, 266] or can be a time ratio within one oscillator [58]. In Chap. 8, a low-power, flexible, highly temperature- and voltage-independent time-based sensor interface is discussed.

1.2.4.3 The Clock Reference

To control the synchronization of the different blocks, a clock reference is needed on the tag. This reference has to clock the digital logic, as well as the UWB transmitter. In some cases, depending on the architecture of the sensor interface, it can also be used as a sample clock. The oscillator also plays a crucial role in the communication between the different nodes. It has to be highly-accurate and PVT-independent, which makes it, next to the powering of the tag, one of the major challenges in a wireless sensor network. Moreover, since the power budget and production cost for the tag are very limited, the use of external components such as a quartz crystal, must be avoided. Typically, a pulse clock of 20–100 MHz is required in the presented applications. Therefore, the main focus of this PhD is on the low-power PVT-independent clock references.

A summary of the target specifications of this time reference is shown in Table 1.1. The specifications are mainly extracted from the receiver design presented in [262, 274]. The receiver is able to compensate for a clock drift of 25–100 ppm depending on the pulse rate. The maximum power consumption of the circuitry depends on the size of the energy reservoir and the voltage range over which the circuitry can operate. Here, the 100 nF capacitor contains 50 nJ when charged to 1 V. This means, when the total average power consumption of the tag is 100 μW, it can operate for

Table 1.1 Summary of the target specifications

Frequency	20–50 MHz
Absolute accuracy	$<\pm 1$ %
Clock drift (within one burst)	$<\pm 25 - 100$ ppm
Temperature range	-20 – 100 °C
Voltage range	$\geqslant 1$ V
Power consumption	<100 μW
Jitter	$\leqslant 25$ ps
Trimming	No

0.5 ms, which corresponds to a burst of 15,000 pulses at a pulse rate of 30 MHz. At the moment it is assumed that half of the energy consumption is dissipated in the oscillator. In practice, the energy reservoir can of course not be discharged down to $V_{min} = 0$ V, however, the initial voltage V_{max} can be assumed to be a little bit higher. A 1.5–0.5 V discharge of a 100 nF capacitor results in a total energy of 100 nJ. The jitter is assumed to be non-important: the time window over which the pulses are correlated at the receiver side is 2.5 ns, which makes an estimated rms energy loss of 1 % (25 ps jitter) acceptable (see also grey inset).

★ Clock drift versus Jitter

As will be discussed elaborately in Chap. 3, the noise in an oscillator causes jitter. This jitter, although unpredictable, can result in a random clock drift. In Sect. 3.6 it will be explained that the uncertainty on a clock edge after n periods σ_n, is the accumulation of the uncertainty on all the previous periods:

$$\sigma_n^2 = n \cdot \sigma_1^2 \tag{1.3}$$

This means, when a period jitter (σ_1) of 25 ps is assumed, after 100 periods, the rms time shift (σ_n) is 250 ps. As a result, 10 % of the received pulse falls out of the correlating window of the receiver (an energy loss <10 %). After 1,000 periods, this is equal to 790 ps or 31 %, which is already a significant energy loss. The receiver, however, also contains a compensation mechanism, which is able to compensate up to 100 ppm clock drift over one burst. When assuming a 30 MHz pulse clock, the rms clock drift as a result of the jitter after 1,000 periods is calculated to be 790 ps/33 μs = 24 ppm. After a complete burst (10,000 pulses), rms time shift is 2.5 ns which results in a complete data loss if no compensation mechanism is available. The rms clock drift as a result of the jitter, however, is then equal to 7.6 ppm, which can easily be compensated.

1.2.4.4 The Antennas

In Fig. 1.16 both antennas are drawn externally to the tag. This, however, is not always the case. In [51, 208] it is shown that the RF scavenging antenna can be an on-chip as well as an externally (bonded) antenna. It must be noted, however, that the antenna is the only component of the wireless tag which is bound to physical dimensions. The size of an optimal antenna is strictly connected to the wavelength of the signal it has to transmit and/or receive. Decreasing the size of the antenna (which is wanted in order to miniaturize the wireless tags), results in a reactive antenna impedance and therefore drastically decreases its performance. Although the best way to decrease the antenna size is by increasing the used frequencies, this strategy also increases the power consumption. These constraints therefore limit the miniaturization of an autonomous sensor node, a limit which is difficult or even impossible to overcome.

Not surprisingly, the use of an integrated antenna poses several problems such as directivity, sensitivity and substrate losses [207, 208]. Furthermore, the physical dimensions of an on-chip antenna are extremely limited, which makes them unusable for low-frequency applications. An external antenna therefore often results in an increased performance, in return of its size and production cost. The UWB antenna has to operate in the sub-GHz frequency range which typically results in dimensions in the order of tens of centimeters. The antenna used in this work (Chap. 9) is discussed more elaborately in [209].

1.3 Focus and Outline of this Work

This chapter has started with a historical introduction on wireless sensor networks and RFIDs. It has been shown that, due to the progress in wireless as well as CMOS technology during the last decades, the step towards fully integrated sensor network nodes can be taken. Furthermore, due to the ever decreasing cost of integrated circuits, the number of possible applications of WSNs and RFIDs is exploding. However, starting from the network architecture used in the Pinballs framework, also the difficulties and challenges for the design of these nodes have been identified.

This dissertation focuses on timing and synchronization issues in WSNs. Using several design cases, different architectures of PVT-independent fully-integrated time references are explored. In each design case, the possible problems are identified and the trade-offs that surface when solving them are investigated.

To improve the readability of this work, it is divided in three major parts. The first part of this work discusses the theoretical background of time references and oscillators as needed to fully understand the design trade-offs of the discussed implementations. Depending on the background and experience of the reader, some of the introduced principles will be basic and can be skipped. Obviously, in the remaining chapters the discussed principles are often referred to. This first part is divided in three different chapters:

- Chapter 2 discusses the basic principles of an oscillator. Starting from the state-space description of an autonomous system, the requirements to obtain a time reference and an oscillator are identified. These minimum requirements are translated to the field of electrical oscillators. Furthermore, the representation of an oscillator signal in the time domain and the frequency domain are unambiguously defined. Finally, also the main properties and parameters of an oscillator are investigated. A difference is made between short-term and long-term frequency stability.
- Chapter 3 focuses on oscillator phase noise and jitter. Although the phase noise requirements of the presented application are rather low, it is important in other RF applications. Therefore, the phase noise of an oscillator, especially for novel oscillator architectures, is important to investigate. Different noise theories are discussed; the Linear Time-Invariant theory of Leeson, the Linear Time-Variant noise model of Hajimiri, but also nonlinear noise models. In the remainder of this work, the applicability and use of the different theories will be demonstrated.
- Chapter 4 is involved with the discussion on PVT-independent oscillators. The different building blocks of an oscillator are discussed and the different sources of inaccuracy are identified. From this discussion the field of integrated oscillators available in literature is explored. The discussed implementations are evaluated with respect to different criteria, with the main focus on low-power and frequency-stable oscillators for wireless sensor networks [63].

Part II of this thesis then will discuss 6 different oscillator implementations in 4 chapters. The presented designs are subjected to an elaborate power, frequency stability and noise study.

- Chapter 5 introduces two RC Wien bridge oscillators. In the first design, a novel Wien bridge topology is developed to obtain temperature independence. By increasing the output resistance of the feedback amplifier using gain-boosted cascode transistors, the output frequency only depends on the components in the feedback network. The noise model of Leeson and the Hajimiri method are both applied to this first implementation. The second implementation is an ultra-low-voltage supply-independent Wien bridge oscillator. In order to do so, two fully-integrated voltage regulators are used [53–55].
- Chapter 6 discusses a newly developed pulsed-harmonic oscillator topology. The output frequency is determined by a high quality (low losses) temperature-independent bondwire LC tank. Because of the pulsed driving technique the power consumption of the oscillator circuitry is lowered and a low-frequency output can easily be obtained. Also the impact of temperature and supply voltage is diminished drastically in this uncommon architecture. The phase noise of this oscillator is elaborately investigated using the noise model of Hajimiri [56, 62].
- Chapter 7 uses a different strategy. Instead of relying on free-running oscillators, two injection-locked oscillators are introduced. The first oscillator, designed in a 130 nm CMOS technology, locks on the carrier of the 2.4 GHz RF power signal. This, however, has a severe power drawback due to the high oscillator frequency. Therefore, also a second (40 nm) injection-locked oscillator is presented, locking

to an AM-modulated clock signal on the RF carrier. This results in an almost 50 % power reduction. Moreover, by using injection locking, this circuit can also be used as a low-power AM-PSK receiver. The exact output frequency of both designs has huge benefits for the power consumption of the UWB link at both the transmitter and receiver side [57, 60].

- Chapter 8 focuses on the design of a time-based sensor interface. By using the ratio of two time values within a ring oscillator, the impact of temperature and supply voltage variations on the digital output value is lowered drastically. Furthermore, by the use of a low-noise oscillator with high control linearity, the SNR and the SNDR at the output and the power-efficiency are comparable to other state of the art implementations [58, 59, 61, 263–265, 279].

The last part of this thesis, part III, contains only one chapter, Chap. 9, describing the development of a complete wireless tag, using the building blocks discussed in part II. By adding a custom-made digital controller, a highly-flexible, programmable RFID tag is obtained. It will be shown that, depending on the application, the data burst can be modified into detail and also the resolution of the sensor interface can be adapted. As a result, the tag is able to perform in different environments with different temperature, voltage and energy constraints [46].

Finally, in Chap. 10, the major conclusions and achievements of this work are restated and summarized. Using the different measures for oscillator stability (defined in Chaps. 2 and 4), the designed circuits are elaborately compared to the state of the art. To conclude, also some suggestions for future research are provided.

Part I
Theoretical Background on Oscillators and Time References

In this Part I, the theoretical concepts are discussed, needed to build and to better understand the principles behind time references. Some of the introduced concepts are rather basic, others are more advanced. Depending on the experience and background of the reader, some parts of this elaborate theoretical introduction can be skipped. However, in Part II of this thesis, where different oscillator implementations are discussed, this theory will extensively be used. Evidently, where applicable, the used formulas and principles are referenced.

In Chap. 2 the basic principles are discussed to obtain a time reference. Starting from the state space description of an autonomous system, the minimum requirements or components of an oscillator are derived. Afterwards, different categories of oscillators and their properties are discussed. Commonly used parameters to characterize an oscillator, such as the Q factor, are introduced.

The next chapter, Chap. 3, focuses on oscillator noise. Different noise sources are identified. Afterwards, an overview is given of the different noise theories developed over the years. Starting from the basic noise model of Leeson, the Linear Time-Variant noise theory of Hajimiri is explained after which also several non-linear theories are briefly introduced. Finally, the relation between the phase noise spectrum and the jitter of the oscillator output is discussed.

The last chapter in this part, Chap. 4, focuses on the most important properties of an oscillator for Wireless Sensor Networks: the long-term frequency stability. In practice, this corresponds to the process, temperature, and supply voltage (PVT) dependency of the output frequency. The quality of the available components in standard CMOS is discussed and their linearity and temperature behavior is analyzed. Finally, an overview is given of different integrated oscillator topologies. The trade-offs between the different design parameters are discussed, starting from the state of the art found in the literature.

Chapter 2
Oscillators and Time References

The word oscillator *originates from the verb* to oscillate *which in its turn originates from the Latin word* oscillātus *(past participle of* oscillāre*, to swing). In English the word can be understood as 'any instrument for producing oscillations, a person or thing that oscillates'. Although the use of electrical oscillators has only started in the twentieth century, the word* oscillator *nowadays mostly refers to an electrical oscillator* [74].

2.1 Introduction

The application field of oscillators is wide and contains many applications such as clock for digital logic, watches, motor controllers, audio applications and even cruise controls or autopilots. Moreover, oscillators are an essential part of both wired and wireless communication systems. Obviously, the requirements regarding oscillator specifications such as power, frequency accuracy and phase noise, are different in each application. In order to develop an efficient strategy in designing an oscillator with the right specifications, the trade-offs and the relation between the design parameters and these specifications need to be examined. A good insight in these principles is essential to understand the observed behavior and the design choices made in the following chapters.

This chapter handles about oscillators and time references in general and is organized as follows. In Sect. 2.2 it will be shown that some basic requirements need to be fulfilled to obtain an oscillation. Next, in Sect. 2.3, oscillators will be divided in two main categories; harmonic and relaxation oscillators. This categorization will have an impact on the generated output waveforms as well as the circuit topology. Although the circuit components used are equal in both cases, a difference is seen in temperature- and supply-voltage-dependency (Chap. 4) but also in the phase noise behavior (Chap. 3). Afterwards, in Sect. 2.4, different representations of an oscillator signal will be introduced. In Sect. 2.5, the main properties of an oscillator will be discussed. Section 2.6 concludes.

V. De Smedt et al., *Temperature- and Supply Voltage-Independent Time References for Wireless Sensor Networks*, Analog Circuits and Signal Processing 128,
DOI 10.1007/978-3-319-09003-0_2

2.2 The Phase Space Description of an Oscillator

Oscillators are observed everywhere in nature: the leaves of a tree waving in the wind, the waves on the ocean, the noise of a waterfall, etc. All of these oscillators can be isolated from their (endless) environment and described as an autonomous system. No influence from outside the system is allowed, i.e. one has to make sure that, after simplification, the environmental parameters with a considerable influence are still present inside the system. This results in a system, which can be described by a finite set of equations and variables. If the system is simplified in the right way, it is still oscillating. The question is how complex a system must be to obtain an oscillation. To answer this, a closer look at the phase space description of a system is required [242].

2.2.1 The Phase Space Description

The phase space description of a system is the mathematical space in which all possible states of a system are represented. Each possible state corresponds to one unique point in the phase space. To obtain the phase space, one must identify the degrees of freedom or free (independent) parameters x_i of the system. A complete set of parameter values gives a complete description of a system at a certain moment. When putting all these variables on a separate axis in an n-dimensional space, the phase space is obtained. To describe the behavior of the system over time, i.e. to be able to predict the state of the system in (near) future, the relation between these parameters and a time variable is needed. This relationship looks as follows:

$$\begin{cases} \dot{x}_1 = f_1(x_1, \ldots, x_n) \\ \quad \vdots \\ \dot{x}_n = f_n(x_1, \ldots, x_n) \end{cases} \tag{2.1}$$

where $x_i(t)$ is a real-valued function of time t, and $f_i(x_1, \ldots, x_n)$ is a smooth, real-valued function of $x_1, \ldots, x_n$ and not a function of time. Any n-th order system (described by an n-th order differential equation) can be transformed to a system similar to (2.1), a set of n first-order differential equations. Even when this set of equations can be solved in a closed form, it is often difficult to truly understand the behavior of the system. One of the most basic techniques in dynamic system analysis is to interpret a differential equation as a vector field in the n-dimensional phase space. This graphical interpretation will be used often throughout this work.

2.2.2 One-Dimensional Systems

One-dimensional systems only have one parameter x_1 and are described using one differential equation:

$$\left\{ \dot{x}_1 = f_1(x_1) \right. \tag{2.2}$$

when $f_1(x_1)$ is a function of time, the system must be described as a higher-order system. The phase space of this first-order system (2.2) is one-dimensional, which means that all possible states of the system are located on a single line.

Example 2.1 Suppose the following system:

$$\begin{cases} \dot{x}_1 = x_1^2 - 1 \end{cases} \tag{2.3}$$

This equation has a closed form solution equal to:

$$t = -\text{arctanh}(x_1) + C \tag{2.4}$$

In which C is a constant depending on the start conditions. Suppose $x_1 = x_{1,0}$ at $t = 0$, then (2.4) this simplifies to:

$$t = -\text{arctanh}(x_1) + \text{arctanh}(x_{1,0}) \tag{2.5}$$

The interpretation of this solution is much easier when using the graphical representation of Fig. 2.1: the horizontal axis represents the 1-dimensional phase space, on the vertical axis $\dot{x}_1$ is drawn. The state of the system is completely defined by its point on the horizontal axis. The arrows on the horizontal axis show for each value of x_1 the direction in which the system will evolve. The velocity of this evolution is proportional to the y-value of the parabolic curve. At points where $\dot{x}_1 = 0$ the system is static. Such points are therefore called *fixed points*. The solid black point is a *stable* fixed point or an *attractor* or *sink*; the open circle represents an *unstable* fixed point or *repeller* or *source*. For a starting point $x_{1,0} < 1$, the system will evolve to $x_1 = -1$; for $x_{1,0} > 1$, x_1 will go to infinity. A picture showing the different trajectories of the system is called a *phase portrait* (see Fig. 2.1).

It is clear from the phase portrait in Fig. 2.1 that a 1-dimensional system can only evolve linearly, in one direction. The evolution of the system is dominated by fixed

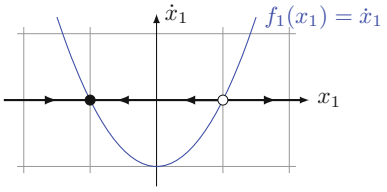

Fig. 2.1 The graphical representation of the 1-dimensional phase space gives a good insight in the first-order system's behavior. All the possible states of the system are represented by unique points on the *horizontal axis*. The *vertical axis* is only added for better understanding

points. All the possible trajectories start and end in a fixed point or diverge to $\pm\infty$. Overshoot or (damped) oscillations are therefore not possible in first-order systems. This corresponds to the fact that a first-order equation has no periodic solutions.

★ **1-Dimensional Oscillations** When x_1 is interpreted as an angle, a first kind of oscillation is possible because the output variable 'wraps around'. This, however, is a mathematical artifact which does not *define* a time reference as such: since there is only one parameter allowed, the resulting oscillation does not have an amplitude. Furthermore, in every physical system which can be described by a 1-dimensional flow on a circle, the oscillation frequency (in this case it's preferred to use *repetition* frequency instead) depends on other time constants, starting conditions or are defined by a higher-order system. This discrepancy between theory and practice comes forth from the wrapping of the state variable, which is a purely mathematical operation.

2.2.3 Two-Dimensional Systems

A second-order or 2-dimensional system is described by two first-order time-invariant equations:

$$\begin{cases} \dot{x}_1 = f_1(x_1, x_2) \\ \dot{x}_2 = f_2(x_1, x_2) \end{cases} \tag{2.6}$$

In the best case these equations have a closed-form solution; most often, however, this is not the case. The use of a phase portrait also helps here to explain the different properties of the system, for instance an oscillator. A distinction is made between two cases: linear and nonlinear systems. For a linear system, Eq. (2.6) simplifies to:

$$\begin{cases} \dot{x}_1 = a \cdot x_1 + b \cdot x_2 \\ \dot{x}_2 = c \cdot x_1 + d \cdot x_2 \end{cases} \tag{2.7}$$

Note that every linear combination of the solutions of this system, will also be a solution. This system can be written as:

$$\dot{\mathbf{x}} = A \cdot \mathbf{x} \tag{2.8}$$

where $\mathbf{x} = \begin{bmatrix} x_1 \\ x_2 \end{bmatrix}$ and $A = \begin{bmatrix} a & b \\ b & c \end{bmatrix}$. The general solution of this set of equations is equal to:

$$\mathbf{x(t)} = c_1 \cdot e^{\lambda_1 \cdot t} \cdot \mathbf{u_1} + c_2 \cdot e^{\lambda_2 \cdot t} \cdot \mathbf{u_2} \tag{2.9}$$

where $\mathbf{u_i}$ are the eigenvectors of matrix A, λ_i are the corresponding eigenvalues, and c_i are coefficients depending on the starting conditions. If the two corresponding eigenvectors are linearly independent, a unique combination of c_1 and c_2 can be found for any start condition $\mathbf{x_0} = \begin{bmatrix} x_{1,0} \\ x_{2,0} \end{bmatrix}$. When the eigenvectors $\mathbf{u}$ are linearly dependent, however, the eigenspace corresponding to λ is only 1-dimensional. The general solution (2.9) in this case only represents the solution for start conditions on this line. The complete solution makes use of a generalized eigenvector $\boldsymbol{\rho}$ for which:

$$(A - \lambda \cdot I) \cdot \boldsymbol{\rho} = \mathbf{u} \text{ and } (A - \lambda \cdot I)^2 \cdot \boldsymbol{\rho} = 0 \tag{2.10}$$

The general solution to the differential equation is then written as:

$$\mathbf{x(t)} = c_1 \cdot e^{\lambda \cdot t} \cdot \mathbf{u} + c_2 \cdot (t \cdot e^{\lambda \cdot t} \cdot \mathbf{u} + e^{\lambda \cdot t} \cdot \boldsymbol{\rho}) \tag{2.11}$$

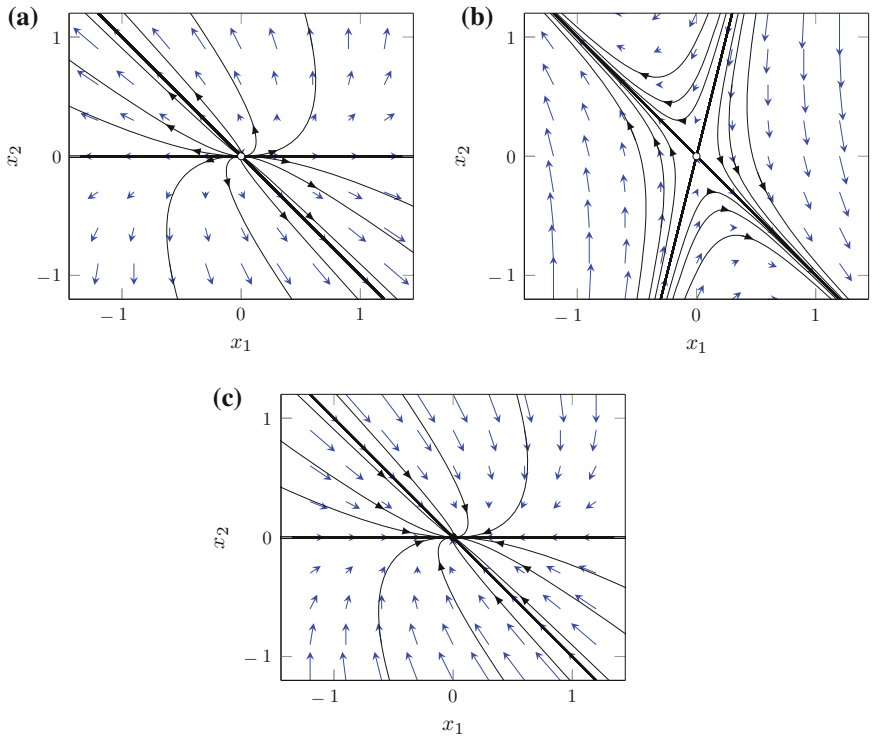

Fig. 2.2 Phase portraits of different linear second-order systems with **a** two positive eigenvalues, **b** a positive and a negative eigenvalue, **c** two negative eigenvalues. **a** and **b** are both called unstable systems, **c** is a stable system

which spans the entire plane. The fixed point at (0, 0) is called a degenerate node. Interesting is to take a closer look at the resulting phase portrait for different eigenvalues λ. Figure 2.2 shows the phase portrait for 3 different systems. The vector field as well as some trajectories are plotted to show the behavior of the system. The matrix, eigenvalues and eigenvectors of the corresponding systems are respectively:

$$\begin{aligned}
&(a)\ A = \begin{bmatrix} 1 & -1 \\ 0 & 2 \end{bmatrix} \quad \lambda_1 = 1,\ \lambda_2 = 2 \quad \boldsymbol{u}_1 = \begin{bmatrix} 1 \\ 0 \end{bmatrix} \boldsymbol{u}_2 = \begin{bmatrix} -1 \\ 1 \end{bmatrix} \\
&(b)\ A = \begin{bmatrix} 1 & -1 \\ -4 & -2 \end{bmatrix} \quad \lambda_1 = -3,\ \lambda_2 = 2 \quad \boldsymbol{u}_1 = \begin{bmatrix} 1 \\ 4 \end{bmatrix} \boldsymbol{u}_2 = \begin{bmatrix} -1 \\ 1 \end{bmatrix} \\
&(c)\ A = \begin{bmatrix} -1 & 1 \\ 0 & -2 \end{bmatrix} \quad \lambda_1 = -1,\ \lambda_2 = -2 \quad \boldsymbol{u}_1 = \begin{bmatrix} 1 \\ 0 \end{bmatrix} \boldsymbol{u}_2 = \begin{bmatrix} -1 \\ 1 \end{bmatrix}
\end{aligned} \tag{2.12}$$

It is easy to see in these graphs that all trajectories are starting and ending in a fixed point or at $\pm\infty$. This means that there is no return path available to accommodate any oscillations. The situation, however, is more interesting when taking a look at systems with two complex conjugate eigenvalues (for a real matrix this means the eigenvectors are also complex conjugate). Again three systems are observed: the main difference between them is the sign of the real part of the eigenvalue. The properties of the systems are:

$$\begin{aligned}
&(a)\ A = \begin{bmatrix} 1 & 1 \\ -1 & 1 \end{bmatrix} \quad \lambda_1 = 1 - j,\ \lambda_2 = 1 + j \quad \boldsymbol{u}_1 = \begin{bmatrix} 1 \\ -j \end{bmatrix} \quad \boldsymbol{u}_2 = \begin{bmatrix} 1 \\ j \end{bmatrix} \\
&(b)\ A = \begin{bmatrix} 1 & -2 \\ 1 & -1 \end{bmatrix} \quad \lambda_1 = -j,\ \lambda_2 = j \quad \boldsymbol{u}_1 = \begin{bmatrix} 2 \\ 1 + j \end{bmatrix} \boldsymbol{u}_2 = \begin{bmatrix} 2 \\ 1 - j \end{bmatrix} \\
&(c)\ A = \begin{bmatrix} -1 & -1 \\ 1 & -1 \end{bmatrix} \quad \lambda_1 = -1 - j,\ \lambda_2 = -1 + j \quad \boldsymbol{u}_1 = \begin{bmatrix} 1 \\ j \end{bmatrix} \quad \boldsymbol{u}_2 = \begin{bmatrix} 1 \\ -j \end{bmatrix}
\end{aligned} \tag{2.13}$$

As can be seen in Fig. 2.3, this results in an oscillator. In (a) the real part of the eigenvalues is positive, which means the amplitude of the oscillation is increasing. In (b) the real part is equal to zero and a stable oscillation will exist (at any amplitude). In (c) the amplitude is decreasing due to the negative real part of the eigenvalue. An important observation is that the amplitude of a linear, oscillating system is undefined. When it is increasing (decreasing), it will be increasing (decreasing) forever. Therefore, a nonlinear component is essential to control the oscillation amplitude and to force the system to a so-called limit cycle. Small amplitudes will increase until this limit cycle is reached; larger amplitudes will decrease to finally reach the same limit cycle. Nonlinear second-order systems can contain zero, one or more limit cycles, depending on the topology. Every real oscillator will contain at least one stable (which means the limit cycle attracts other trajectories) limit cycle. The shift from a linear oscillator to a nonlinear oscillator can be demonstrated using the *van der Pol* oscillator.

2.2.4 The van der Pol Oscillator

The van der Pol oscillator is a second-order system, which is described by the following equation:

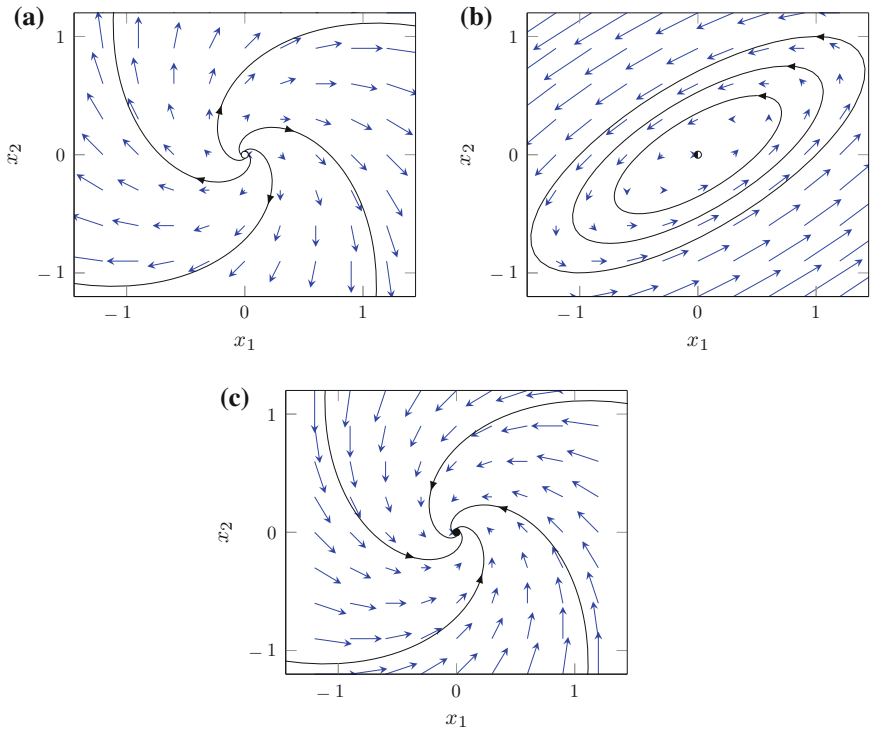

Fig. 2.3 Phase portraits of different linear second-order systems with two complex conjugate eigenvalues. The real part has **a** a positive sign, **b** a value equal to zero, **c** a negative real part. **a** is called an unstable system, **b** is marginally stable and **c** is a stable system

$$\ddot{x}_1 - \mu \cdot (1 - x_1^2) \cdot \dot{x}_1 + x_1 = 0 \tag{2.14}$$

where $\mu > 0$ is a scalar parameter indicating the nonlinearity and the strength of the damping. Using the *Liénard* transformation $x_2 = \mu \cdot (x_1 - x_1^3/3) - \dot{x_1}$, this equation can be written in its familiar second-order form [242]:

$$\begin{cases} \dot{x}_1 = \mu \cdot (x_1 - x_1^3/3) - x_2 \\ \dot{x}_2 = x_1 \end{cases} \tag{2.15}$$

when $\mu = 0$, no damping is present in the equation and the system is a linear oscillator similar to Fig. 2.3b. When μ is slightly increased, after some transient effects, the system will enter a limit cycle. The higher the nonlinearity factor, the more the oscillator will move from a linear and 'soft' behavior towards a nonlinear 'switched' oscillator, as shown in Fig. 2.4.

For low μ, the two state variables are continuously changing or interacting. For higher values of μ, however, this is not the case: on the left hand side the system

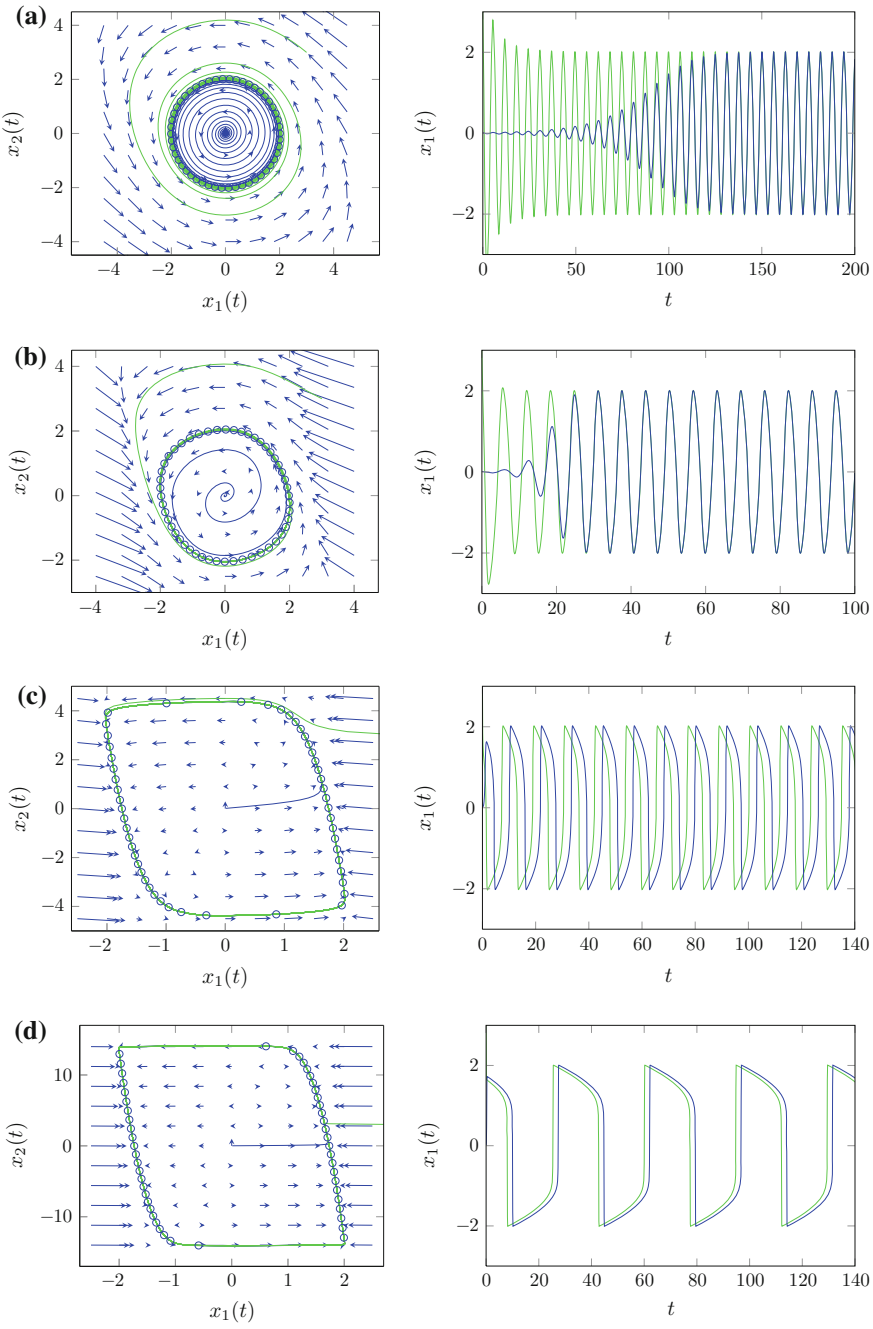

Fig. 2.4 Phase portraits and output signal of the van der Pol oscillator for different values of μ. The initial value for the *blue curve* is (0.01, 0.01), for the *green curve* this is (3, 3). On each phase portrait the 50 *blue circles* are equidistant in time to show the behavior of the oscillator during the limit cycle. **a** $\mu = 0.1$, **b** $\mu = 0.5$, **c** $\mu = 5$, **d** $\mu = 20$

is moving downward; at a certain level it will suddenly switch to the right, where it will move slowly upward, suddenly switch to the left and so on. The period of the oscillator is then mainly determined by the phases where the oscillator is moving upward or downward and not by the switching. For high values of μ the first state of the oscillator can even be considered to be discrete (*left* or *right*) and determines the evolution in the second state in a discrete way (*move downward* or *move upward*). The switch between these states happens when x_2 reaches a certain threshold.

Since a phase portrait shows every possible state of a system, the amplitude of a second-order system with an attracting limit cycle cannot overshoot, neither oscillate. This is because the trajectories in the phase portrait can never cross, they always (exponentially) reach the limit cycle. Once the state of the system is on its limit cycle, it will stay there. As a result, to study the stability of an amplitude regulator, the order of the mathematical model (which is often a reduction of the real system) must always be higher or equal to 3. More in general, for a second-order system, this is described by the *Poincaré-Bendixson Theorem* [242]:

Theorem 2.1 *Suppose that:*

- *R is a closed bounded subset of the plane;*
- $\dot{\boldsymbol{x}} = \boldsymbol{f}(\boldsymbol{x})$ *is a continuously differentiable vector field on an open set containing R;*
- *R does not contain any fixed points;*
- *There exists a trajectory C that is "confined" in R, in the sense that it starts in R and stays in R for all future time.*

Then either C is a closed orbit or spirals towards a closed orbit when $t \to \infty$. *In either case R contains a closed orbit.*

To prove that the van der Pol oscillator has a limit cycle, it is sufficient to construct a ring-shaped trapping region around the fixed point at the origin for which, at every border of the region, the vector field is pointing inward. Furthermore, this theorem implies that there is no chaos in a second-order system; a system evolving within a limited sub plane will have a predictable behavior.

2.2.5 n-Dimensional Systems

Most practical systems have an order higher than two. An example is the instability of an amplitude regulation [270], which can only occur in higher-order systems. Without going into detail, two examples are briefly discussed. The first example is a van der Pol oscillator with an unstable amplitude control; the second example shows chaotic behavior in the three-dimensional phase space.

Example 2.2 The van der Pol equation (2.14) has a damping which is proportional to the squared value of the output waveform. However, it is often not feasible to implement an amplitude control which exactly follows this

behavior. Furthermore, the amplitude will often be limited or clipped due to the limited output swing of the oscillator circuit, which introduces hard distortion. A better solution is to use an average or rms value of the output signal in the feedback circuit. The adapted van der Pol equation looks like this:

$$\ddot{x}_1 - \mu \cdot (1 - x_1^2) \cdot \dot{x}_1 - \eta \int (A - x_1^2) dt + x_1 = 0 \tag{2.16}$$

where η determines the integration speed of the amplitude control and A is the desired rms output of the circuit. To transform this system to its autonomous equations, three state variables are needed. A possible set of equations is:

$$\begin{cases} \dot{x}_1 = x_2 \\ \dot{x}_2 = x_2 \cdot x_3 - x_1 \\ \dot{x}_3 = -2 \cdot \mu \cdot x_1 \cdot x_2 + \eta \cdot (A - x_1^2) \end{cases} \tag{2.17}$$

The behavior of this system can be compared to the working principle of a PI regulator on the squared value of the output signal. The proportional path is determined by μ; the integrating path is determined by the value of η. When η is equal to zero, the equation simplifies to (2.14) and the amplitude regulation is perfectly stable for $\mu > 0$. However, with a proportional regulator, the error on the amplitude can only be decreased by increasing μ which increases the nonlinearity of the circuit. By slightly increasing η, the resulting rms amplitude error is integrated and the damping of the oscillator is adapted. An example for $A = 1/\sqrt{2}$, $\mu = 0.05$ and $\eta = 0.01$ is shown in Fig. 2.5. Although the oscillator converges to a limit cycle, the amplitude regulator is under-damped and overshoots several times before converging to its final value. When $\mu = 0$, the amplitude overshoot is not damped at all.

Example 2.3 The second example is to show the more unpredictable behavior in a third-order system compared to a second-order system, called chaos. This odd behavior can be observed in the forced van der Pol equation and was already noticed by Balthasar van der Pol himself. However, other researchers [256] classified these phenomena as quasi-periodic but non-chaotic. At the same moment they proposed a modified van der Pol equation [139] which *has* chaotic behavior:

$$\ddot{x}_1 - \mu \cdot (1 - x_1^2) \cdot \dot{x}_1 + x_1^3 = B \cdot \cos(t) \tag{2.18}$$

Again, μ is a nonlinearity parameter, B determines the amplitude of the applied signal which forces the van der Pol equation. An autonomous set of equations is equal to:

$$\begin{cases} \dot{x}_1 = \mu \cdot (x_1 - x_1^3/3) - x_2 \\ \dot{x}_2 = x_1^3 - B \cdot \sin(x_3) \\ \dot{x}_3 = 1 \end{cases} \tag{2.19}$$

Chaotic behavior means that, although the behavior of the system is deterministic, it is unpredictable and never repeats itself. Chaotic systems are therefore very sensitive to the initial conditions and to minor numerical errors during calculation. Since chaotic systems can perfectly occur within a bounded volume within phase space, the periodic (or quasi-periodic) trajectories are very dense. Figure 2.6 pictures the evolution of 32 start conditions over time. The initial distance between these points is equal to 0.01. To show the overall behavior and the density of the trajectories, one trajectory is plotted too. For this simulation $\mu = 0.1$ and $B = 1$. A more quantitative way to characterize the sensitivity to initial conditions is the use of Lyapunov exponents, which falls beyond the scope of this work [139, 242]. An example application is estimating the reliability of a weather forecast (which is an extremely complex dynamical system) [84].

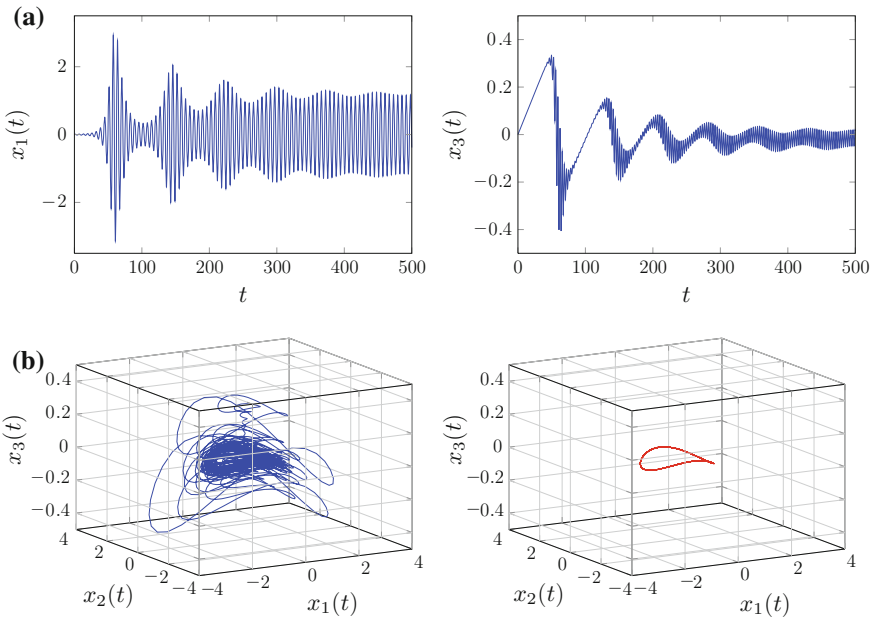

Fig. 2.5 Behavior of the van der Pol oscillator with a PI amplitude regulator, $A = 1/\sqrt{2}$, $\mu = 0.05$ and $\eta = 0.01$. **a** Shows the behavior in the time domain. The output signal $x_1(t)$ is shown *on the left*. *On the right* $x_3(t)$ is plotted, which corresponds to the resulting output signal of the amplitude regulator. **b** Shows the behavior in the phase plane/space; the overshoot of the amplitude is clearly visible. It takes a lot of periods before the limit cycle (*on the right*) is reached

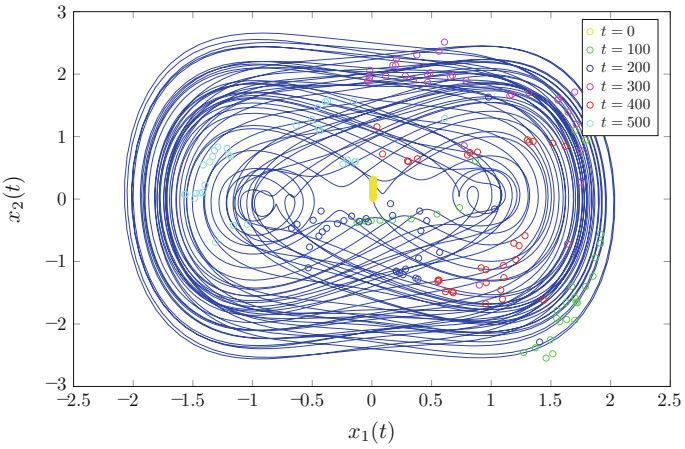

Fig. 2.6 Chaotic behavior of the forced modified van der Pol equation. The *circles* show the evolution of 32 near start conditions over time. The *blue line* is an $x_1 - x_2$ plot of one of the trajectories

2.3 Minimum Requirements for a Time Reference

What are the minimum requirements to define a time reference? This question is different from the discussion in the previous section: in this case it is acceptable that the system starts at its starting condition and evolves to another state *after a certain time*. No repetition of this process is needed.

A difference can be made between state variables which are connected to an energy level (the voltage over a capacitor, the speed of a moving object, the water level in a tank, etc.) and state variables which are not related to an energy level (position of an object on an equipotential surface, angular position of a carousel, etc.). The first category of state variables all have a connection to time, or are dependent on the definition of one second. This corresponds to the physical principle that the evolution of the energy level of a system will always be downwards. Otherwise, there is no driving force and the state variable or energy level will be static. Hence, to define a time reference, at least one energy tank is needed. Of course, since the unit of energy is not equal to *one second*, also another component is needed. The evolution of the system is the exchange of energy between these components, which can happen in two different manners.

★ **Definition of time**
The unit of time, one second, is one of the 7 SI base units. Moreover, it is next to Kelvin the only SI base unit of which the definition does not depend on any other SI base units. Originally, one second was defined as $1/(24 \cdot 60 \cdot 60)$ of the

day, but since the rotation speed of the earth is slowly decreasing this definition had to be adapted. Since 1967, one second is 'autonomously' defined as *"the duration of 9.192.631.770 periods of the radiation corresponding to the transition between the two hyperfine levels of the ground state of the cesium-133 atom."* Recent research shows that even more accurate definitions of time are to be discovered [11]. Except from using an atomic clock, there are of course many other (and more affordable) ways to implement a time reference, be it less accurate. This can be done using components or devices which have a connection with time: their unit is dependent on the definition of one second [310].

2.3.1 An Energy Reservoir and a Resistor

The first possibility is that the energy is dissipated in a resistor. This resistor can be a resistor of any kind, electrical, mechanical, aerodynamical, hydromechanical, etc. It has to be a component or device that dissipates the energy of the energy reservoir. When bringing the focus on electrical components, the derived unit of resistance is ohm or Ω:

$$1\,\Omega = 1\frac{\mathrm{kg}\cdot\mathrm{m}^2}{\mathrm{s}^3\cdot\mathrm{A}^2} = 1\frac{\mathrm{J}}{\mathrm{A}\cdot\mathrm{s}} \tag{2.20}$$

It is the amount of energy consumed per second when a current of 1 A is flowing through the resistor; which dissipates the energy. On the other hand, there are 2 possible energy reservoirs in electronics: capacitors (to accumulate a charge or voltage) and inductors (to accumulate a magnetic charge or current). By definition their values are equal to:

$$L = U/\frac{dI}{dt} \quad \text{and} \quad C = I/\frac{dU}{dt} \tag{2.21}$$

which means that their units can be written as:

$$1\mathrm{H} = \frac{\mathrm{V}\cdot\mathrm{s}}{\mathrm{A}} = \frac{\mathrm{kg}\cdot\mathrm{m}^2}{\mathrm{s}^2\cdot\mathrm{A}^2} = \frac{\mathrm{J}}{\mathrm{A}^2} \tag{2.22}$$

$$1\mathrm{F} = \frac{\mathrm{A}\cdot\mathrm{s}}{\mathrm{V}} = \frac{\mathrm{s}^4\cdot\mathrm{A}^2}{\mathrm{kg}\cdot\mathrm{m}^2} = \frac{\mathrm{J}}{\mathrm{V}^2} \tag{2.23}$$

These units indicate the accumulation of energy. The energy is not dissipated; it simply depends on the current through the inductor or the voltage over the capacitor. When connecting one of these devices to a resistor, the energy will be consumed. The speed at which this happens depends on the value of the resistor as well as the

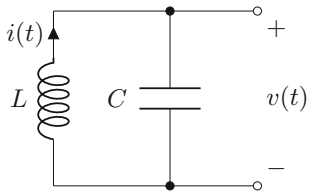

Fig. 2.7 Two coupled energy tanks, an inductor L and a capacitor C, forming an oscillator

energy reservoir. The time to empty the reservoir for 63 % is equal to:

$$\tau_L = L/R \tag{2.24}$$

$$\tau_C = R \cdot C \tag{2.25}$$

and indeed, the unit of the result is in both cases equal to seconds. The link between resistance, voltage and current is given by Ohm's law. Instead of a resistor, also a combination of a voltage and a current can be used, as is often the case in so-called relaxation oscillators.

2.3.2 Two Different Energy Reservoirs

The second possibility to create a time reference is by combining two energy reservoirs. Two identical energy reservoirs can only exchange energy in an infinitesimal short time span, which obviously does not result in a time value. By taking two different energy reservoirs, the exchange of energy will happen in a controlled manner. This means that *it takes some time* to exchange energy. In the case of an inductor and a capacitor, the current through the inductor slowly charges the capacitor. Afterwards, when the current is equal to zero, the capacitor is discharged while generating a current in the inductor. From (2.21) and the schematic in Fig. 2.7, it appears that the equation to describe the energy exchange between an inductor and a capacitor is equal to (using Kirchhoff's law):

$$-L \cdot \frac{di(t)}{dt} - \frac{1}{C} \int_{-\infty}^{t} i(t)dt = 0 \quad \text{or} \quad L \cdot \frac{d^2 i(t)}{dt^2} + \frac{i(t)}{C} = 0 \tag{2.26}$$

The solution to this differential equation is equal to:

$$i(t) = A \cdot e^{j \cdot \omega_n \cdot t + j \cdot \theta_0} \tag{2.27}$$

$$\Re(i(t)) = c_1 \cdot \cos(\omega_n \cdot t) + c_2 \cdot \sin(\omega_n \cdot t) \tag{2.28}$$

where Euler's formula and $\omega_n = 1/\sqrt{L \cdot C}$ are used to obtain (2.28). A and θ_0 or c_1 and c_2 are two constants depending on the start conditions. Again, the resulting unit of $\sqrt{L \cdot C}$ is seconds. The possibility to derive a time reference from the

energy exchange between two energy reservoirs does not only apply to electrical circuits but is also applicable in other branches of science. An important condition is the possibility to exchange energy between two energy tanks. With the necessary amount of engineering it is possible to build a system exchanging electrical and for instance mechanical energy. A simple example is a lossless DC motor connected to an inductor.

Example 2.4 A commonly used DC motor model is an inductor L_m in series with a resistor R_m and a so-called back electromotive force E_M. In this example the series resistor is equal to zero since we assume an ideal motor without any losses. Furthermore, the series inductance is lumped into the external inductor L_e, resulting in one inductor L. The following formulas complete the motor model [17]:

$$\begin{cases} T_M = c \cdot \Phi \cdot i(t) \\ E_M = c \cdot \Phi \cdot \omega_m \end{cases} \tag{2.29}$$

where T_M is the motor torque, ω_m is the angular frequency of the motor and c is a motor constant depending on the construction. Φ is the magnetic flux due to the magnetic poles, expressed in Weber (Wb). Applying Kirchhoff's law on the circuit of Fig. 2.8 leads to the following equation:

$$-\frac{di(t)}{dt} \cdot L = c \cdot \Phi \cdot \omega_m \tag{2.30}$$

$$= \frac{c^2 \cdot \Phi^2}{I} \cdot \int_{-\infty}^{t} i(t)dt \tag{2.31}$$

where I is the moment of inertia of the rotor (rotating part of the motor). The solution to this equation is equal to (2.27). However, in this case, ω_n (the angular frequency of the oscillation, not that of the rotor) is equal to:

$$\omega_n = \sqrt{\frac{c^2 \cdot \Phi^2}{I \cdot L}} \tag{2.32}$$

The unit of ω is, as expected, equal to $1/s$. The motor in this example acts as an energy converter between electrical energy and kinetic energy, whereas the inductor transfers electrical energy to magnetic energy.

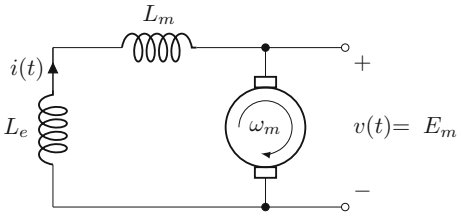

Fig. 2.8 An inductor can exchange its energy with a kinetic energy tank. A DC motor is needed to do the energy conversion

2.3.3 Harmonic Versus Relaxation Oscillators

The difference between a linear and a nonlinear oscillator was demonstrated in Sect. 2.2.4. Based on the linearity or nonlinearity and the necessary oscillator components, oscillators can be divided into two classes: harmonic and relaxation oscillators. The boundary between both categories is rather fuzzy, as previously shown.

2.3.3.1 Harmonic Oscillators

When building an oscillator using only linear components, two continuous state variables or energy reservoirs are needed. The frequency of the oscillator is then defined by the properties of the two reservoirs. But, what about the amplitude or startup behavior? A completely linear oscillator has an ever increasing, decreasing or perfectly constant amplitude. A nonlinear component is needed to control the amplitude. *Oscillators consisting of (mainly) linear components are therefore called harmonic oscillators.* Due to their linearity, the behavior of harmonic oscillators can be described in terms of transfer functions, loop gain and phase margin. An important criterion to have a working harmonic oscillator is the *Barkhausen Criterion*:

Theorem 2.2 *A feedback system will only generate a stable oscillation when the loop gain is equal to one and the complete phase shift is equal to* $z \cdot 2 \cdot \pi$ *where* $z \in \mathbb{Z}$.

$$\begin{cases} |H(s)| = 1 \\ \angle H(s) = z \cdot 2 \cdot \pi \end{cases} \quad \text{and } z \in \mathbb{Z} \tag{2.33}$$

where $H(s)$ *is the loop transfer function.*

The output waveform is a sine wave and only contains a limited amount of harmonics. In Sect. 4.4.1, some examples from literature will be discussed.

2.3.3.2 Relaxation Oscillators

When looking back to van der Pol's equation, it is observed that, when increasing the nonlinearity parameter μ, one of the states slowly converts from a continuous state towards a discrete state. The system slowly evolves over the continuous state and

then switches its discrete state, after which this process is repeated. Such oscillators can therefore be implemented using only one energy reservoir and a discrete memory element (a Schmitt trigger or a latch) to implement the discrete state. *An oscillator containing strongly nonlinear elements is called a relaxation oscillator.* The term relaxation oscillator was used by Balthasar van der Pol to express the period of 'building up a tension' in the continuous state and then suddenly relax by switching the discrete state. As a result, the output is non-sinusoidal and the first derivative of the output waveform is often not continuous.

Relaxation oscillators cannot be described using transfer functions. It is therefore difficult to mathematically predict their behavior. Often, a piecewise combination of (differential) equations is needed to describe the behavior. Typically, relaxation oscillators are oscillators where an energy tank is combined with a resistive element. However, in Chap. 6, a relaxation oscillator will be built using a harmonic LC tank. In Sect. 4.4.2, different examples found in literature will be discussed.

2.4 Representation of an Oscillator Signal

The output signal of an oscillator has a representation in the time domain as well as in the frequency domain. Different representations are discussed in this section. The introduced symbols will be used in the remainder of this work while discussing the frequency stability as well as the noise performance. The relationship between the measures in the frequency and the time domain will be discussed into more detail in Chap. 3, handling about phase noise and jitter.

2.4.1 Oscillator Signals in the Time Domain

The most basic representation of (the first harmonic of) an oscillator output signal can be written as [92]:

$$v(t) = A(t) \cdot \sin(\Phi(t)) \tag{2.34}$$

where $A(t)$ is the instantaneous amplitude and $\Phi(t)$ is the instantaneous phase of the oscillator signal. More in general, however, an oscillator signal can have a completely different, but periodic waveform:

$$v(t) = A(t) \cdot f(\Phi(t)) \tag{2.35}$$

where f is a periodic function with period $2 \cdot \pi$. Since this is an oscillator, an *almost cyclostationary* signal is expected,[1] which means that the instantaneous phase is

[1] As will be seen in Chap. 3, a real cyclostationary signal can only be expected from PLL output signals, which are corrected every cycle.

expected to increase linearly. The instantaneous angular frequency $\omega(t)$ is written as:

$$\omega(t) = \frac{d\Phi(t)}{dt} \tag{2.36}$$

and is expressed in *radians per second*. Hence, in an ideal oscillator $\omega(t)$ is constant. For a Voltage-Controlled Oscillator (VCO), $\omega(t)$ depends on the input control signal. When the relationship between the angular frequency and the control signal is linear:

$$\omega(t) = \omega_0 + K_{VCO} \cdot v_c(t) \tag{2.37}$$

which means that the VCO acts as an integrator for the control voltage $v_c(t)$, with integration constant K_{VCO} and the phase deviation (compared to an identical non-modulated VCO) as an output signal. Since the phase deviation is unbounded, a VCO can be considered to be an ideal integrator [92].

2.4.1.1 The Oscillator Phase

In a real oscillator, random as well as deterministic variations are observed in the phase of the oscillator output signal. In most cases the deterministic and the systematic variations are treated separately from the random fluctuations. This means:

$$\Phi(t) = \omega_0 \cdot t + \phi(t) + \Psi(t) \tag{2.38}$$

where ω_0 is the constant mean angular frequency, $\phi(t)$ represents the random phase variations or noise, and $\Psi(t)$ implements both the systematic and deterministic variations in the phase function. The function $T(t)$, often called the *phase-time*, is equal to the instantaneous phase divided by ω_0 and gives the time of a clock that is run by the oscillator:

$$T(t) = t + \frac{\phi(t)}{\omega_0} + \frac{\Psi(t)}{\omega_0} \tag{2.39}$$

For an ideal oscillator this is equal to t. When neglecting the systematic and deterministic phase variations, the random instantaneous phase-time fluctuation is defined as:

$$x(t) = \frac{\phi(t)}{\omega_0} \tag{2.40}$$

which can be understood as the time difference between corresponding zero crossings of a phase-noise-contaminated oscillator and its noise-free replica. The instantaneous fractional frequency deviation can be defined as:

$$y(t) = \frac{dx(t)}{dt} = \frac{\frac{d\phi(t)}{dt}}{\omega_0} = \frac{\Delta\omega(t)}{\omega_0} = \frac{\Delta f(t)}{f_0} \tag{2.41}$$

which allows to compare frequency fluctuations between oscillators at different frequencies. Furthermore, it is insensitive to frequency multiplication or division.

2.4.1.2 The Oscillator Amplitude

For the amplitude, similar equations can be used. Although it is not commonly used in literature, apart from the random amplitude variations (noise), also some systematic or deterministic amplitude variations can be identified:

$$A(t) = A_0 + \varepsilon(t) + \Upsilon(t) \tag{2.42}$$

where A_0 is the ideal amplitude, $\varepsilon(t)$ are the random amplitude variations and $\Upsilon(t)$ represents the deterministic or systematic amplitude errors. When talking about or when measuring amplitude noise, $\Upsilon(t)$ is mostly neglected. The first reason for this is that when measuring a signal, this mostly happens only over a short time which makes a measurement of the (slow) systematic amplitude variations impossible. The second reason is that in most applications, the amplitude of the clock signal is not important, certainly when it is used as a digital clock. The amplitude function of the oscillator does not affect the times of the zero crossings (or the noise on the zero crossings, called jitter) which is often used as a benchmark to evaluate the quality of an oscillator. However, when measuring the spectrum of an oscillator, both the phase noise $\phi(t)$ and the amplitude noise $\varepsilon(t)$ are measured. For a sinusoidal signal it is mostly assumed that the amplitude and phase noise each add one half of the noise spectrum. The phase noise spectrum is then 3 dB lower than the measured spectrum [38].

2.4.2 Oscillator Signals in the Frequency Domain

Oscillator signals also have a representation in the frequency domain. For an ideal sinusoidal oscillator (2.34) where $\Phi(t)$ increases linearly, the output spectrum results in two Dirac impulses $\pm\omega_0$. When the waveform is more irregular, harmonics are present in the output signal, represented in the spectrum by Dirac impulses at $\pm n \cdot \omega_0$. As previously shown, the frequency and the phase are closely connected:

$$\omega = \frac{d\Phi(t)}{dt} = \omega_0 + \frac{d\phi(t)}{dt} + \frac{d\Psi(t)}{dt} \tag{2.43}$$

of which the last term is supposed to be close to zero. The consequence of the time dependency of A and ϕ is a spectrum with sidebands around every harmonic. To characterize these frequency or phase deviations, the Power Spectral Density (PSD)

Table 2.1 Commonly used PSD functions to characterize the frequency stability of an oscillator signal

Symbol	Unit	Description
$S_{\Delta f}(f)$	Hz	PSD of frequency fluctuations
$S_{\Delta\omega}(f)$	$(\text{rad/s})^2/\text{Hz}$	PSD of angular frequency fluctuations
$S_y(f)$	1/Hz	PSD of fractional frequency fluctuations
$S_\phi(f)$	rad^2/Hz	PSD of phase fluctuations
$S_x(f)$	s^2/Hz	PSD of phase time fluctuations

is used, as defined in Appendix A.2.2. The PSD can be calculated for almost every time signal. Commonly used PSDs for oscillators are summarized in Table 2.1. From the previous sections it is clear that there are several relations between these PSD functions. From (2.41) it follows that:

$$S_\phi(f) = \frac{S_{\Delta\omega}(f)}{\omega^2} \tag{2.44}$$

From the linearity property of the Fourier transform, it follows that:

$$S_y(f) = \frac{S_{\Delta\omega}(f)}{\omega_0^2} = \frac{S_{\Delta f}(f)}{f_0^2} \tag{2.45}$$

Combining both relationships, it can be concluded that:

$$S_y(f) = \frac{f^2}{f_0^2} \cdot S_\phi(f) = \omega^2 \cdot S_x(f) \tag{2.46}$$

To obtain these relations, the properties from Appendix A.1 are used. From these relations, it is clear that the PSD of the phase and the frequency differ with a factor of f^2. As will be seen in Sect. 3.3, the oscillator spectrum is mostly divided into different sections, depending on the slope of the frequency spectrum. Using the power-law noise model, which describes the phase noise of an oscillator as a sum of different power law curves [92, 164], the (single-sided) PSD of $y(t)$ and $\phi(t)$ is typically written as:

$$S_y(f) = \sum_{\alpha=-2}^{+2} h_\alpha \cdot f^\alpha \tag{2.47}$$

$$S_\phi(f) = f_0^2 \cdot \sum_{\alpha=-2}^{+2} h_\alpha \cdot f^{\alpha-2} \tag{2.48}$$

The different power law curves all represent a type of noise, coming from different noise sources and being the result of different noise mechanisms. The interpretation of these power law terms will elaborately be discussed in Chap. 3. Although this is assumed to be rather uncommon, depending on the noise sources, also higher numbers for α are possible.

2.4.2.1 The Use of $\mathscr{L}(f)$ to Characterize the Phase Noise

A commonly used measure of phase noise is $\mathscr{L}(f)$, especially when measuring the phase noise. Several definitions of this measurement are possible. However, a generally accepted definition as used in [37, 101] is:

$$\mathscr{L}_{total}(\Delta\omega) = \frac{\mathscr{P}_{side}(f_0 + \Delta f, 1\text{ Hz})}{\mathscr{P}_{carrier}} \tag{2.49}$$

which is sometimes expressed in dB and in which $\mathscr{P}_{side}(f_0 + \Delta f, 1\text{ Hz})$ is the single-sideband noise power in a 1 Hz interval at a frequency offset Δf from the carrier frequency f_0. As mentioned earlier, the effect of both amplitude and phase noise is present in the noise spectrum. In Sect. 3.6, it will be shown that the sideband noise in many applications is dominated by phase noise since this part of the noise cannot be eliminated. When considering only the phase noise:

$$\mathscr{L}(\Delta\omega) = \frac{\mathscr{P}_{\phi-side}(f_0 + \Delta f, 1\text{ Hz})}{\mathscr{P}_{carrier}}, \tag{2.50}$$

note that, when using a spectrum analyzer, this portion of the noise cannot be measured separately. As shown in [82], in fact the power of the total signal must be in the denominator of (2.49) and (2.50). However, because the replacement by the power of the carrier only introduces a small error and the entire signal power is much more difficult to measure, this error is in most cases neglected.

2.4.2.2 Relationship Between $\mathscr{L}(f)$ and $S_\phi(f)$

Up till now only the PSD of the phase fluctuations was discussed without taking the carrier signal into account. According to [217], the (single-sided) spectrum of the entire signal is approximated by:

$$S_{RF}(f) \approx \frac{A_0^2}{2} \cdot \left[\delta(f - f_0) + S_\phi(f - f_0)\right] \tag{2.51}$$

where $\delta(f)$ is the delta function or Dirac impulse, $S_\phi(f)$ is the (two-sided) power spectral density, $A_0^2/2$ equals the carrier power and f_0 is the carrier frequency. The

PSD of the phase fluctuations is multiplied by the carrier power to obtain the signal's sideband noise. Furthermore it is clear that this equation only holds for signals where the amplitude noise is negligible and the phase fluctuations are small. The assumption must hold that the spectrum of a phase-modulated signal is (linearly) approximated by the phase spectrum itself. This also means that the baseband PSD of the phase fluctuations is up-converted to the carrier frequency and therefore has the same frequency dependency:

$$\mathscr{P}_{\phi-side}(f_0 + \Delta f, 1\text{ Hz}) = \frac{A_0^2}{2} \cdot S_\phi(\Delta f) \tag{2.52}$$

As a result, the relationship between $\mathscr{L}(f)$ and $S_\phi(f)$ can be written as:

$$\mathscr{L}(\Delta f) = \frac{\mathscr{P}_{\phi-side}(f_0 + \Delta f, 1\text{ Hz})}{\mathscr{P}_{carrier}} \tag{2.53}$$

$$= \frac{\frac{A_0^2}{2} \cdot S_\phi(\Delta f)}{\frac{A_0^2}{2}} = S_\phi(\Delta f) \tag{2.54}$$

which is often used as an alternative definition of $\mathscr{L}(\Delta f)$ [82, 92]. In [92] a lower limit of the frequency offset is calculated down to which this approximation is valid; Δf must be large enough such that:

$$\int_{\Delta f}^{\infty} S_\phi(\Delta f) df \ll 1\ rad^2 \tag{2.55}$$

At small frequency offsets, the phase noise spectrum typically increases drastically, which makes the first-order Taylor approximation of the phase-modulated signal uncertain indeed.

2.5 Properties of an Oscillator

The properties of an oscillator can be described using several parameters, going from the quality of an energy tank to the short- and long-term frequency stability. In Chap. 6, where the focus is on pulsed resonant tanks, a more detailed discussion will be held on the properties of an nth-order energy tank. Often, a tight connection exists between all of these parameters. Theoretical parameters and properties can be interesting to use at design time, but only detailed circuit simulations or even better measurements show the real behavior of a circuit.

2.5.1 The Quality Factor

The quality factor or Q factor is a measure to characterize the quality of an energy tank or, more in general, a two-pole system. As will be shown, the Q factor almost completely determines the properties of the system, going from the filtering characteristics to the losses and the noise generation. Depending on the topology of the tank, a different method can be used to calculate it. Furthermore, for some tank topologies also the meaning and understanding of this factor is non-trivial and against every intuition. Even then, however, it is a useful figure to quantify for instance the noise generation in an oscillator. Four calculation methods are demonstrated, all of them are based on the tank schematics in Fig. 2.9.

Definition 2.1 The most basic definition of the Quality Factor or Q factor is based on the energy losses in the tank.

$$Q = 2 \cdot \pi \cdot \frac{E_{stored}}{E_{Loss-per-Cycle}} \tag{2.56}$$

The Q factor therefore quantifies the quality of a resonator.

For an inductor L with series resistance R_s (Fig. 2.9c), driven by a sine wave with amplitude I_A and angular frequency ω, this results in:

$$E_{stored} = \int_0^{T/4} P dt = \frac{L I_A^2}{2} \tag{2.57}$$

$$E_{Loss-per-Cycle} = 4 \int_0^{T/4} I^2 R_s dt = \frac{\pi I_A^2 R_s}{\omega} \tag{2.58}$$

$$\Rightarrow Q_L = \frac{L\omega}{R_s} \tag{2.59}$$

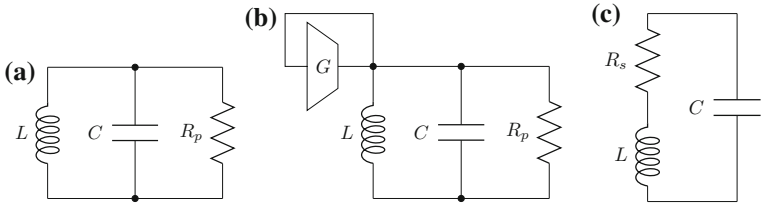

Fig. 2.9 Different RLC tanks. The *left* tank (**a**) is not driven and its losses are represented by the parallel resistor. In (**b**) the same tank is driven by a transconductance amplifier. In (**c**) the losses are represented by a series resistor in the inductor, which is the closest to the real situation

Since, for fully integrated LC tanks, the losses in the tank are dominated by the losses in the inductor, the capacitor is supposed to be ideal compared to the inductor. As a result, the Q factor of the inductor, Q_L, is equal to that of the complete tank. In (2.59), ω can be substituted by $\omega_n = 1/\sqrt{LC}$, the natural angular frequency of the LC tank.

$$Q = Q_L = \sqrt{\frac{L}{C}}\frac{1}{R_s} \tag{2.60}$$

A similar calculation can be made for the parallel RLC network in Fig. 2.9c. This time, the calculation is started from the charging of the capacitor using a sine wave:

$$E_{stored} = \int_0^{T/4} Pdt = \frac{CV_A^2}{2} \tag{2.61}$$

$$E_{Loss-per-Cycle} = 4\int_0^{T/4} V^2/R_p dt = \frac{\pi V_A^2}{R_p \omega} \tag{2.62}$$

$$\Rightarrow Q_C = C\omega/R_p \tag{2.63}$$

Also this time it is assumed that all the losses in the tank are lumped into the parallel resistor R_p. Using the same substitution for ω as in the previous example, the Q factor of the parallel network is equal to:

$$Q = Q_C = \sqrt{\frac{C}{L}}R_p \tag{2.64}$$

Although this parallel network is often not the real situation, it is commonly used for better understanding. In Fig. 2.9b, this parallel resistor is exactly compensated by the transconductance amplifier G and a stable oscillation is obtained. In the neighborhood of the natural angular frequency ω_n, the relation between R_p and R_s is given by:

$$R_p = \frac{1}{R_s}\frac{L}{C} \tag{2.65}$$

This equality and the reason why it is only valid in the neighborhood of ω_n, can be better understood when looking at the transfer functions of both networks. The current-voltage transfer functions of the parallel and series networks in Fig. 2.9a, c are respectively:

$$H_P(s) = \frac{\frac{s}{C}}{s^2 + \frac{1}{C\cdot R_p}\cdot s + \frac{1}{L\cdot C}} = \frac{\omega_n \cdot \sqrt{\frac{L}{C}}\cdot s}{s^2 + \frac{\omega_n}{Q}\cdot s + \omega_n^2} \tag{2.66}$$

$$H_S(s) = \frac{\frac{s}{C} + \frac{R_s}{L\cdot C}}{s^2 + \frac{R_s}{L}\cdot s + \frac{1}{L\cdot C}} = \frac{\omega_n \cdot \sqrt{\frac{L}{C}}\cdot s + \omega_n^2 \cdot R_s}{s^2 + \frac{\omega_n}{Q}\cdot s + \omega_n^2} \tag{2.67}$$

using (2.60), (2.64) and $\omega_n = 1/\sqrt{LC}$. Taking (2.60) into account, in the neighborhood of ω_n both the network with the parallel and series resistor are equivalent as long as $Q \gg 1$. For lower frequencies, however, the network with the series resistance will have a higher equivalent impedance compared to the parallel network. Writing the transfer function (more specifically the denominator) in its standard form (2.66) and (2.67), can be considered as an analytical method to calculate the Q factor. For higher-order systems each pair of (complex conjugate) poles has its own Q.

To explain the other two calculation methods, only the network with the parallel resistor is considered since this will simplify the calculations significantly. The third method to calculate Q is based on the sharpness of the peak in the transfer function. Consider the graph in Fig. 2.10.

Definition 2.2 For a 2-pole system showing a peak in its transfer function, the Q factor is equal to the center frequency ω_n divided by the -3 dB width $\Delta\omega_{3dB}$ of the resonant peak:

$$Q = \frac{\omega_n}{\Delta\omega_{3dB}} \tag{2.68}$$

The fourth and last calculation method is based on the steepness of the output phase of the resonant network. This is shown in Fig. 2.10, the Q factor is then defined as:

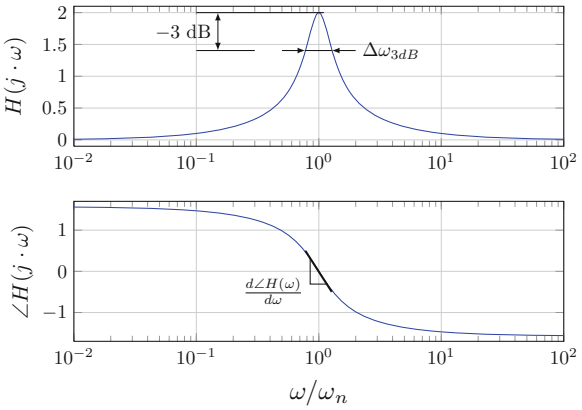

Fig. 2.10 Different definitions of the Q factor of a two-pole system, based on the width (bandwidth) of the resonant peak and based on the steepness of the phase shift of the feedback network

Definition 2.3 The Q factor of a resonant network with natural frequency ω_n is proportional to the steepness of the phase of the network gain at its zero-crossing:

$$Q = \frac{\omega_n}{2} \cdot \frac{d\angle H(j\omega)}{d\omega} \tag{2.69}$$

Depending on the topology, one or more definitions can be used to calculate the Q factor. It must, however, be clear that in the case of a nonlinear (relaxation) oscillator, the use of linear transfer functions does not make sense and only the basic definition (2.56) can be used.

2.5.1.1 Meaning of the Q factor

The meaning of the Q factor can be understood when translating the transfer function to the time domain. Since $H_P(s)$ and $H_S(s)$ are current-voltage transfer functions (or the impedance of the RLC network), $H(s) \cdot I(s) = V(s)$ in which $I(s)$ and $V(s)$ are the Laplace transform of the applied current and the resulting voltage output. If no external current is applied, (2.66) and (2.67) both result in the following differential equation:

$$\frac{d^2v(t)}{dt^2} + \omega_n \left(\frac{1}{Q}\right) \frac{dv(t)}{dt} + \omega_n^2 \cdot v(t) = 0 \tag{2.70}$$

where $v(t)$ is the voltage over the capacitor. The solution to this equation is equal to:

$$\begin{aligned} v(t) = A \cdot e^{\frac{-\omega_n \cdot t}{2Q}} \cdot e^{\frac{\sqrt{1-4Q^2}}{2Q}\omega_n t} \\ + B \cdot e^{\frac{-\omega_n \cdot t}{2Q}} \cdot e^{-\frac{\sqrt{1-4Q^2}}{2Q}\omega_n t} \end{aligned} \tag{2.71}$$

where A and B are constants depending on the initial conditions of the network. This proves that the network is completely characterized by the natural frequency ω_n and the Q factor. The behavior is not determined by the position of the parallel or series resistor. It is now easy to see what the influence is of the Q factor:

- $-1/2 \leqslant Q \leqslant 1/2$: In this case, the result is an ever increasing ($Q < 0$) or decreasing ($Q > 0$) function. Since all exponents are real, there will be no oscillations.
- $Q > 1/2$: Due to the complex exponent, this will result in an oscillation. Since the real part of the exponent is negative, the oscillation will decay.
- $Q < -1/2$: Again, this is an oscillator; the amplitude, however, increases and goes to infinity.

- $Q = \pm\infty$: Since this results in a complex exponential function, there will be an oscillation. The amplitude, however, will be constant and equal to $\sqrt{A^2 + B^2}$. The angular frequency in this case is equal to ω_n; in the other cases the angular frequency is somewhat lower.

Obviously, a negative Q cannot exist for a network containing only passive components. When $Q = 1/2$, the system is critically damped.

2.5.1.2 The Generalized Q factor

When a gain stage, Fig. 2.9b, is present in the electrical network, it can be useful to define the generalized Q factor. The differential equations in this case are not the same for the parallel and the series network:

$$\frac{d^2 v_P(t)}{dt^2} + \omega_n \left(\frac{1}{Q} - \sqrt{\frac{L}{C}} G \right) \frac{dv_P(t)}{dt} + \omega_n^2 v_P(t) = 0 \tag{2.72}$$

$$\frac{d^2 v_S(t)}{dt^2} + \omega_n \left(\frac{1}{Q} - \sqrt{\frac{L}{C}} G \right) \frac{dv_S(t)}{dt} + \omega_n^2 (1 - GR_s) v_S(t) = 0 \tag{2.73}$$

Although both equations have an analytical solution, things can be simplified by defining the generalized Q a follows:

$$Q_G = \left(\frac{1}{Q} - \sqrt{\frac{L}{C}} \cdot G \right)^{-1} \tag{2.74}$$

or more in general:

Definition 2.4 For a general second-order feedback system equation of the form (consisting of an amplifier and a feedback network):

$$\frac{\omega_n \cdot K \cdot s + L}{s^2 + \frac{\omega_n}{Q} \cdot s + \omega_n^2} \cdot I = U \tag{2.75}$$

where Q is the Q factor of the feedback network, ω_n is the natural angular frequency of the network and K and L are constants and I and U are the Laplace transform of the applied current and the resulting output voltage.

- $G = U/I$ is defined as the transconductance of the feedback amplifier.

- The generalized Q factor Q_G of the network is defined as:

$$Q_G = \left(\frac{1}{Q} - K \cdot G\right)^{-1} \tag{2.76}$$

When making use of this definition, the differential equations of the series and of the parallel network, both including a feedback amplifier, are written as[2]:

$$\frac{d^2 v_P(t)}{dt^2} + \omega_n \frac{1}{Q_G} \frac{dv_P(t)}{dt} + \omega_n^2 v_P(t) = 0 \tag{2.77}$$

$$\frac{d^2 v_S(t)}{dt^2} + \omega_n \frac{1}{Q_G} \frac{dv_S(t)}{dt} + \omega_n^2 \left(1 - \frac{1}{Q^2} + \frac{1}{QQ_G}\right) v_S(t) = 0 \tag{2.78}$$

The generic solutions to these equations are then rather straightforward:

$$\begin{aligned} v_P(t) = A \cdot e^{\frac{-\omega_n \cdot t}{2Q_G}} \cdot e^{\frac{\sqrt{1-4Q_G^2}}{2Q_G}\omega_n t} \\ + B \cdot e^{\frac{-\omega_n \cdot t}{2Q_G}} \cdot e^{-\frac{\sqrt{1-4Q_G^2}}{2Q_G}\omega_n t} \end{aligned} \tag{2.79}$$

$$\begin{aligned} v_S(t) = A \cdot e^{\frac{-\omega_n \cdot t}{2Q_G}} \cdot e^{\frac{\sqrt{1-4Q_G^2\left(1-\frac{1}{Q^2}+\frac{1}{QQ_G}\right)}}{2Q_G}\omega_n t} \\ + B \cdot e^{\frac{-\omega_n \cdot t}{2Q_G}} \cdot e^{-\frac{\sqrt{1-4Q_G^2\left(1-\frac{1}{Q^2}+\frac{1}{QQ_G}\right)}}{2Q_G}\omega_n t} \end{aligned} \tag{2.80}$$

where A and B are constants depending on the start conditions. The generalized Q factor Q_G plays the same role in a network with active components as the Q factor does in a passive network. Different from the Q factor, the generalized Q factor can be negative. For the parallel network, it is clear that the transconductance amplifier behaves as a parallel negative resistance which cancels the parallel resistor. When the resistor is in series with the inductor, the resistor cannot be canceled completely. The angular frequency at constant amplitude ($Q_G = \infty$) is in this case equal to $\omega_n \cdot \sqrt{1 - 1/Q^2}$ which is *lower* than in the case of a decaying/increasing oscillation amplitude. For the parallel network, the angular frequency at constant amplitude is ω_n which is somewhat *higher* than in the case of a decaying/increasing amplitude. The fact that the oscillation frequency depends on the amplitude stability shows the importance of a stable amplitude regulation.

[2] Since Q_G depends on G, GR_s can be substituted by $1/Q^2 - 1/(QQ_G)$.

2.5.2 *Stability of an Oscillator Signal*

The stability of an oscillator can have several meanings. In Sect. 2.4, a time-domain representation of an oscillator signal was defined (2.34). This equation both contains a non-constant amplitude function and a phase function. Systematic as well as random variations apply to both the amplitude as the phase. As previously shown, these variations are also visible in the output spectrum of the oscillator. However, it is impossible to separate amplitude from phase effects in the output spectrum. Since amplitude variations can easily be removed using a clipping amplifier, the focus is mostly on the phase variations. Note however, as shown previously, that an influence exists between the amplitude and the phase variations.

Apart from the difference between amplitude and phase errors, fluctuations in an oscillator signal are often divided into a *long-term* and a *short-term* contribution. This mostly corresponds to respectively *systematic* and *random* fluctuations in the oscillator signal. Random variations are mostly called noise, which will elaborately be discussed in Chap. 3. Systematic variations, caused by for instance temperature and supply voltage changes, have a slower impact on the oscillator frequency and amplitude. In the context of this work, the term 'frequency stability' is used to refer to these so-called PVT effects, elaborately discussed in Chap. 4. As will be seen in Chap. 3, low-frequency colored noise sources can also result in long-term systematic variations and are therefore an exception to the proposed division.

2.6 Conclusion

In this chapter, the basic principles of an oscillator together with the representations and properties of an oscillator signal have been discussed. Starting from the phase space description of a dynamic system, the minimum circuit requirements for and necessary components of an oscillator have been identified. From this, the difference between harmonic and relaxation oscillators has been explained. The discussion on oscillator properties has clarified that pointing out general design rules to obtain a stable oscillator is a complex process. The principles of oscillator noise and frequency stability will therefore be discussed in respectively Chaps. 3 and 4. In these chapters, the previously defined parameters to characterize and represent an oscillator signal will frequently be used.

Chapter 3
Jitter and Phase Noise in Oscillators

Thermal noise is caused by black body radiation, a phenomenon in quantum physics, which was accurately described by Max Planck in 1901. The frequency and power of the emitted radiation depends on the temperature of the matter. This radiation, and also its noise, is therefore present everywhere in the universe. This so-called Cosmic Microwave Background (CMB) Radiation, was accidentally discovered by the American physicists Arno A. Penzias and Robert W. Wilson. In 1965 at Bell Laboratories they measured the unexpected and annoying background noise source in microwave transmissions of telephone conversations. Nowadays, this radiation is used to gain some insight in the birth, age and evolution of the universe. For recognizing the importance of their discovery, both scientists received the Noble Prize for Physics in 1978 [223].

3.1 Introduction

As pointed out previously, the short-term stability of an oscillator mostly corresponds to the noise in the oscillator output signal. When talking about noise in general, this can be amplitude noise and phase noise. In most applications, the amplitude noise can be neglected since the oscillator is built to provide a clock signal, where the amplitude is clipped. The phase noise, on the other hand, is closely connected to the jitter and will therefore have an influence on the timing of the events in clocked circuits. In audio applications, however, both amplitude and phase noise can be heard and are therefore both an important specification. Furthermore, phase noise in a clock signal can easily be translated to amplitude noise in for instance a digital to analog converter. In this chapter, the general principles are discussed behind the generation of oscillator phase noise. When discussing different oscillators in the remainder of this work, this theory will be used to understand the phase noise generation in each oscillator implementation.

This chapter is organized as follows. The next section will briefly introduce the noise sources in an electronic circuit. A difference is made between white and colored

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noise sources. Section 3.3 will describe a typical noise spectrum. A first attempt is done to understand the mechanism behind this spectrum using the noise model of Leeson. Afterwards, in Sect. 3.4, the linear time-variant noise theory of Hajimiri will be discussed. This theory quantitatively describes the generation of the different slopes in an oscillator spectrum. A brief discussion on nonlinear noise models will be held in Sect. 3.5. The relationship between phase noise and jitter is discussed in Sect. 3.6 for white as well as colored noise sources. The relationship between the jitter and the Q factor will also be explained and the phase noise Figure of Merit (FoM) will be introduced. Finally, in Sect. 3.9, conclusions are drawn.

3.2 Noise Sources

In electronics, different noise sources can be identified. In this section a brief overview is given of the noise sources, including expressions for the corresponding noise spectra.

⋆ Thermal Noise
In 1927 John Bertrand Johnson, a Swedish-American Physicist, described the phenomenon of *'spontaneous motion of the electricity in a conducting body'* [118]. He built an experimental setup to characterize this effect and discovered that this motion depends on the temperature, which resulted in the name 'Thermal Noise'. It was, however, Harry Nyquist, who applied the fundamental principles of thermodynamics to Johnson's theory and proved the correctness of the mathematical expressions [191]. They showed that the noise power in a conductor is given by:

$$P = k \cdot T \cdot b \tag{3.1}$$

where k is the Boltzmann constant, T is the temperature and b is the measured bandwidth. Note that the noise *power* in a conductor does *not* depend on the resistor value. This is because so-called Johnson-Nyquist noise is caused by blackbody radiation. The charges in the conductor move to try to nullify the induced electrical fluctuations caused by the blackbody radiation in the inductor. Therefore, the noise power only depends on the temperature.
In the years after, also another type of noise was identified, pink noise or flicker noise, of which the noise density is inversely proportional to the frequency. This results in an equal noise power in every frequency decade, sounding 'flat' to a human ear. Aldert Van der Ziel discovered the first model which could explain the $1/f$ slope in the noise spectrum [323]. Up till today, however, the real mechanism or multiple mechanisms behind pink noise generation are still not completely understood.

3.2.1 Noise in a Resistor

The noise in a resistor mainly consists of thermal noise. This means that the noise voltage and equivalent noise current power spectral density are given by:

$$\overline{dv_R^2} = 4 \cdot k \cdot T \cdot R \cdot df \tag{3.2}$$

$$\overline{di_R^2} = 4 \cdot k \cdot T / R \cdot df \tag{3.3}$$

Due to its flat spectrum up till very high frequencies (10^{13} Hz), this noise is called *white noise* [219]. But a resistor also exhibits $1/f$ noise, which is in practical applications often neglected. The *pink noise* power spectral density strongly depends on the quality of the conductor (grain size, material), but also the voltage V_R over the resistor: the pink noise is therefore modeled by the following formula:

$$\overline{dv_{Rf}^2} = V_R^2 \cdot \frac{K_{fR} \cdot R \cdot df}{A_R \cdot f} \tag{3.4}$$

where K_{Rf} is a fitting parameter depending on the material properties of the resistor and A_R is the area or size of the resistor [219]. A commonly used technique to kill the pink noise of a resistor is to reduce the DC voltage over the resistor by putting a capacitor in series.

3.2.2 Noise in a P-N Junction

A P-N junction mainly produces shot noise. This type of noise is caused by the quantized charge carriers crossing the junction. The shot noise is independent of the temperature of the junction but does depend on the (forward/backward) current I_D [324]:

$$\overline{di_D^2} = 2 \cdot q \cdot I_D \cdot df \tag{3.5}$$

where q is the charge of a single charge carrier (electron or hole). Apart from this white noise source, there is also a pink noise source. Similar to a resistor, the noise power spectral density depends on the current through the diode and the size A_D of the junction:

$$\overline{di_{Df}^2} = I_D \cdot \frac{K_{fD} \cdot df}{A_D \cdot f} \tag{3.6}$$

where K_{fD} is a technology dependent constant.

3.2.3 MOS Transistor Noise

The noise of a MOS transistor consists of different noise sources. All these (thermal) noise sources can be taken together in one input source:

$$\overline{dv_{eq}^2} = 4 \cdot k \cdot T \cdot R_{eff} \cdot df \tag{3.7}$$

$$\text{where: } R_{eff} = \frac{2/3}{g_m} + R_G + R_S + R_B \cdot (n-1)^2 \tag{3.8}$$

$$\text{and: } (n-1) = g_{mb}/g_m \tag{3.9}$$

The first term of the equivalent resistor R_{eff} is due to the channel resistance, R_G and R_S are respectively the gate and source resistance of the transistor and R_B is the bulk resistance. The factor $(n-1)$ is caused by the fact that the transconductance g_{mb} at the bulk is in most cases much smaller than g_m [219]. Due to different mechanisms, the MOS transistor also generates pink noise. This is generated at the P-N junctions in the substrate as well as at the oxide-semiconductor interface at the gate. Again, all junctions can be referred to one gate input source:

$$\overline{dv_{eqf}^2} = \frac{K_{fT} \cdot df}{W \cdot L \cdot C_{ox}^2 \cdot f} \tag{3.10}$$

where K_{fT} is depending on the MOS topology (NMOS, PMOS, JFET, ...) and $W \cdot L$ indicates the size of the transistor. In [219] it is shown that the pink noise of a JFET is much lower compared to that of a MOSFET (due to the absence of the oxide-semiconductor interface), which makes them very suitable for audio applications. Another way to reduce the $1/f$ transistor noise, is by switching the MOSFET between inversion and accumulation. In [75, 283] it is assumed that this 5–8 dB reduction is caused by the reduction of oxide trap noise (charge traps at the semiconductor-oxide interface). In [93] it is demonstrated that this technique can be applied to reduce the phase noise in, for instance, a ring oscillator.

3.3 The Phase Noise Spectrum

When looking at the spectrum of the different noise sources, there is still a difference with the typical shape of the output noise of an oscillator. This spectrum is shown in Fig. 3.1. The noise spectrum can be divided into different sections [104, 190]. In this figure, which corresponds well to a real phase noise spectrum, the power-law model (2.48) can easily be recognized [164, 217].

- **White noise**: This noise is broadband phase noise and has in fact little to do with the resonance mechanism. In general, the cause of this noise is understood as the noise added by amplifiers.

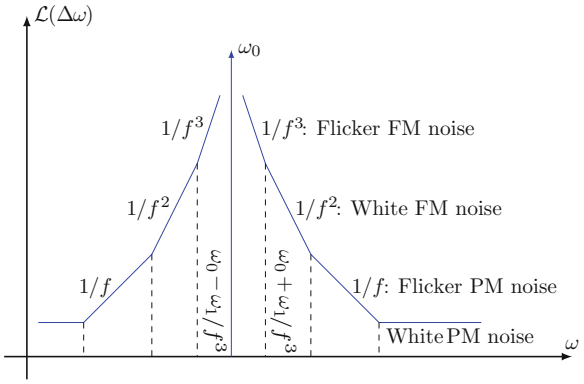

Fig. 3.1 Phase noise spectrum at the output of a generic oscillator. According to the power-law noise model, the spectrum can be divided in different zones, with a different noise origin or underlying mechanism

- **Flicker PM noise**: This noise can be related to a physical resonance mechanism in the oscillator. Usually, however, it is added by noisy and/or nonlinear electronics, amplifiers or mixers. This noise is common even in high-quality oscillators since the output signals of most oscillators need to be amplified or buffered before they can be used.
- **White FM noise**: This noise is typically understood as *phase noise* and is generated in oscillator circuits. As will be seen in the following sections, it is an up-conversion of the white noise of the components in the oscillator circuit.
- **Flicker FM noise**: Also $1/f$ noise can be up-converted by the oscillator circuit, which results in this type of phase noise. The corner frequency ω_{1/f^3} depends on the waveform as well as on the $1/f$ noise corner frequency of the noise sources.
- **Random Walk FM**: This noise has an even higher order ($1/f^4$). It is difficult to measure since it is very close to the carrier. This noise can typically be related to the oscillator's physical environment. Measurement of the environmental parameters (temperature, mechanical shock, vibration, ...) can often help to identify the noise sources.

Over the years, different noise models have been developed to understand the mechanism and origin behind this spectrum. This stays, however, an interesting topic for future research.

3.3.1 The Noise Model of Leeson

The noise theory of Leeson starts from the assumption that an oscillator is a Linear Time-Invariant (LTI) system. The output waveform of an oscillator is given by (2.35). Due to the nonlinear and unpredictable increase of the phase $\Phi(t)$ in this expression,

apart from the Dirac impulses at the oscillation harmonics, the spectrum also has side lobs around each harmonic [154, 211]. The shape of these side lobs is characterized by the PSD $S_x(\omega)$ or equivalently $\mathscr{L}(\Delta\omega)$ (2.50). To predict this noise spectrum, the impedance of the RLC network in Fig. 2.9a is calculated to be [equivalent to (2.66)]:

$$Z(\omega_n + \Delta\omega) = R_p \cdot \frac{1}{1 + j \cdot 2 \cdot Q \cdot \frac{\Delta\omega}{\omega_n}} \tag{3.11}$$

The transfer function of the complete network (Fig. 2.9b) for a parallel input current source is then:

$$H(\omega_n + \Delta\omega) = \frac{R_p}{1 + j \cdot 2 \cdot Q \cdot \frac{\Delta\omega}{\omega_n} - G \cdot R_p} \tag{3.12}$$

For a stable oscillation, the product $G \cdot R_p$ must be equal to one, which makes the closed-loop transfer function equal to:

$$H(\omega_n + \Delta\omega) = -j \cdot R_p \cdot \frac{\omega_n}{2 \cdot Q \cdot \Delta\omega} \tag{3.13}$$

The equivalent noise of the parallel resistor is equal to (3.3). Although also a significant noise contribution from the active devices exists, the total noise density is often written as:

$$\overline{di^2} = 4 \cdot F \cdot k \cdot T/R \cdot df \tag{3.14}$$

where F is a multiplicative factor, often called the *device excess noise factor*. The phase noise in the $1/f^2$ region of the spectrum is then calculated to be (assuming that the oscillation frequency ω_0 is equal to the natural frequency of the tank ω_n):

$$\mathscr{L}(\Delta\omega) = 10 \cdot \log \frac{\frac{1}{2} \cdot |H(\Delta\omega)|^2 \cdot \overline{di^2}/\Delta f}{\frac{1}{2} \cdot V_{\max}^2} \tag{3.15}$$

$$= 10 \cdot \log \left[\frac{2 \cdot F \cdot k \cdot T}{P_s} \cdot \left(\frac{\omega_n}{2 \cdot Q \cdot \Delta\omega} \right)^2 \right] \tag{3.16}$$

where the factor 1/2 comes forth from neglecting the amplitude noise and P_s is the average power dissipated in the resistive part of the tank. In this way at least the $1/f^2$ region of the phase noise spectrum can be understood. This is shown in Fig. 3.2. As can be seen, the $1/f$ noise is not present in the shaped spectrum. The theory does not explain any mechanism how this colored noise is up-converted to the oscillation frequency. However, in the Leeson-Cutler model a noise portion in the $1/f^3$ region is added, but is completely empirical to fit the measurements [41, 211]. The Leeson-Cutler formula of the resulting phase noise spectrum is equal to:

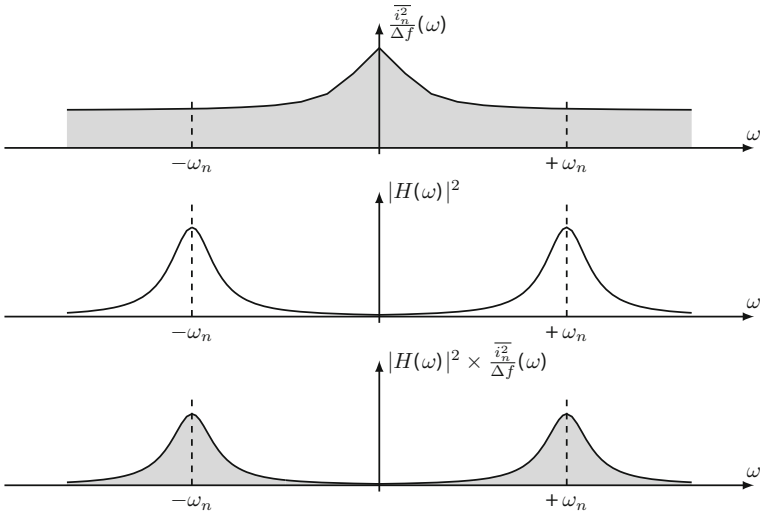

Fig. 3.2 The noise theory of Leeson-Cutler is based on the idea that the injected noise is multiplied by the transfer characteristic of the resonant network. Although this is an explanation for the $1/f^2$ slope in the phase noise spectrum, it does not take the up-conversion of the injected $1/f$ noise into account

$$\mathscr{L}(\Delta\omega) = 10 \cdot \log\left[\frac{2 \cdot F \cdot k \cdot T}{P_s} \cdot \left[1 + \left(\frac{\omega_n}{2 \cdot Q \cdot \Delta\omega}\right)^2\right] \cdot \left(1 + \frac{\Delta\omega_{1/f^3}}{|\Delta\omega|}\right)\right] \tag{3.17}$$

where ω_{1/f^3} is the corner frequency between the third- and second-order region. Often this frequency is said to be equal to the $1/f$ frequency of the noise sources. This, however, is a common misunderstanding which can be countered by measurement results [101]. Furthermore, due to the large transient signals of the oscillator, the noise sources are often not constant but cyclostationary. This makes it in most cases impossible to accurately calculate F. For similar reasons, one can wonder if the noise sensitivity is constant during the oscillation cycle, hence it is justified to question the used LTI approach.

Although some of the aspects of Leeson's noise theory are doubtful, it nevertheless has been proven to be useful for different oscillator topologies. In [211] the theory is applied to ring oscillators. It is extended for multiplicative noise, which is the result of noise mixing with the carrier frequency due to strong nonlinearities. It is also shown that the theoretical expected values are close to the obtained measurement results.

3.4 The Phase Noise Theory of Hajimiri

The noise theory of Hajimiri has been developed to take the periodically time-varying noise sensitivity into account. This is the result of the cyclostationary character of an oscillator which makes a Linear Time-Variant (LTV) approach more suitable. The LTV theory can be used to predict the noise performance of an oscillator circuit without use of any empirical parameters, including the up conversion of $1/f$ noise, and without the need for calibration by measurement results [101, 151].

3.4.1 Generation of the Phase Noise Spectrum

The mechanism explaining the shape of the phase noise spectrum, contains different steps. These steps are demonstrated and explained after which formulas are derived to approach the resulting noise spectrum.

3.4.1.1 The LTV Oscillator Model

An oscillator can be modeled as a system with n inputs, corresponding to the different noise sources, and 2 outputs, the instantaneous amplitude $A(t)$ and the excess phase $\phi(t)$, see (2.38). Since the different noise sources are considered to be independent, the superposition principle can be applied. Therefore, each noise source is treated independently as two autonomous single-input, single-output systems, one for the instantaneous amplitude and one for the excess phase. The outputs of these systems must be summed over all noise sources to obtain the complete noise spectrum. This is shown in Fig. 3.3. Both of these systems are (periodically) time variant, indicating the changing sensitivity of the oscillator to the injected noise current. When considering the tank shown in Fig. 2.9a, an injected noise pulse causes a voltage jump in the capacitor:

$$\Delta V = \frac{\Delta q}{C} \tag{3.18}$$

where Δq is the total injected charge by the applied noise current impulse. A phase trajectory of a decaying oscillation is shown in Fig. 3.4. This figure shows the injection of an equal charge at two different moments in the oscillation cycle. It can be seen that the moment of impact has a huge influence on the induced phase as well as on the amplitude effects. Furthermore, it is observed that the impact is higher for a low oscillator amplitude; the impact is inversely proportional to the maximum charge $q_{\max}$ on the output node. Simulations show [101] that the impact on both amplitude and phase linearly depends on the amount of charge injected in the circuit. The unit impulse response for the excess phase can then be expressed as:

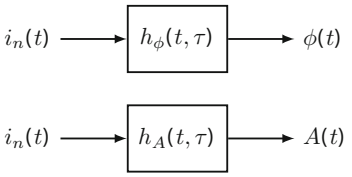

Fig. 3.3 The response of an oscillator to an injected noise current can be modeled using two single-input, single-output systems, one for the excess phase and one for the instantaneous amplitude

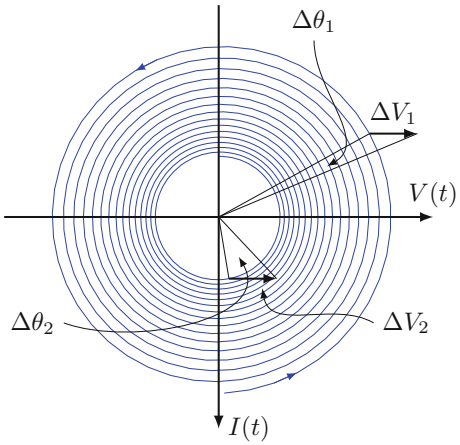

Fig. 3.4 State diagram of a free running LC tank. The losses in the tank result in a decreasing oscillation. It is clear that the sensitivity to an injected noise pulse does not only depend on the moment of impact, but also on the amplitude

$$h_\phi(t,\tau) = \frac{\Gamma(\omega_0 \cdot \tau)}{q_{\max}} \cdot u(t-\tau) \tag{3.19}$$

where τ is the moment when the noise current pulse is applied to the system and $u(t)$ is the unit step function or Heaviside function. $\Gamma(\omega_0 \cdot \tau)$ is called the impulse sensitivity function (ISF), denoting the sensitivity at each moment in the oscillation cycle. It is a dimensionless, frequency- and amplitude-independent function with period $2 \cdot \pi$. It only depends on the waveform or the shape of the limit cycle. The excess phase at the output is then calculated by the superposition of all applied noise impulses:

$$\phi(t) = \int_{-\infty}^{\infty} h_\phi(t,\tau) \cdot i_n(\tau) d\tau = \frac{1}{q_{\max}} \int_{-\infty}^{t} \Gamma(\omega_0 \cdot \tau) \cdot i_n(\tau) d\tau \tag{3.20}$$

where $i_n(t)$ represents the total noise current injected on a certain node (possibly coming from different noise sources). Since the noise is a completely random signal,

it is impossible to calculate this integral explicitly. The ISF is a periodical signal with the same period as the oscillator signal which can therefore be expanded in a Fourier series:

$$\Gamma(\omega_0 \cdot \tau) = \frac{c_0}{2} + \sum_{k=1}^{\infty} c_k \cdot \cos(k \cdot \omega_0 \cdot \tau + \theta_k) \tag{3.21}$$

where c_k are the Fourier coefficients of the ISF (as defined in Appendix A.1). Due to the randomness of the noise, the phase of the noise signal can impossibly be predicted nor retrieved. The phase θ_k of the harmonics in the ISF can therefore be neglected. The formula for the excess phase can then be written as:

$$\phi(t) = \frac{1}{q_{\max}} \cdot \left[\frac{c_0}{2} \int_{-\infty}^{t} i_n(\tau) d\tau + \sum_{k=1}^{\infty} c_k \cdot \int_{-\infty}^{t} i_n(\tau) \cos(k\omega_0 \tau) d\tau \right] \tag{3.22}$$

The importance and use of this formula can be shown by applying Simpson's formula on the argument of the second integral when a noise signal $\cos(\omega_i \tau)$ is injected into the circuit:

$$\cos(\omega_i) \cdot \cos(k \cdot \omega_0 \cdot \tau) = \frac{\cos[(k \cdot \omega_0 - \omega_i) \cdot \tau] + \cos[(k \cdot \omega_0 + \omega_i) \cdot \tau]}{2} \tag{3.23}$$

If the frequency of the injected noise signal is close to that of $k \cdot \omega_0$, one of the two terms results in a low-frequency signal. Due to the *averaging* nature of the integral, the high-frequency terms in the integral are negligible. The injected noise will therefore only have an impact if its frequency is close to zero or close to a harmonic of the oscillator waveform. This is shown in Fig. 3.5. If a noise signal with an amplitude I_n, an offset $\Delta\omega$ from the k-th harmonic is applied, the resulting excess phase is approximated by:

$$\phi(t) \approx \frac{I_n \cdot c_k \cdot \sin(\Delta\omega \cdot t)}{2 \cdot q_{\max} \cdot \Delta\omega} \tag{3.24}$$

This results in two equal sidebands at $\pm\Delta\omega$ in the power spectral density $S_\phi(\omega)$ of the excess phase $\phi(t)$. The higher the offset $\Delta\omega$ from one of the harmonics, the more the noise signal is attenuated by the integral operation. The transformation described up till now, namely the generation of the excess phase as a result of noise injection, has indeed shown to be a linear operation.

3.4.1.2 Phase Modulation of the Excess Phase

The next step is to insert the resulting excess phase (3.24) in (2.35). Using Euler's formula, the output signal of the oscillator (2.34) can be written as:

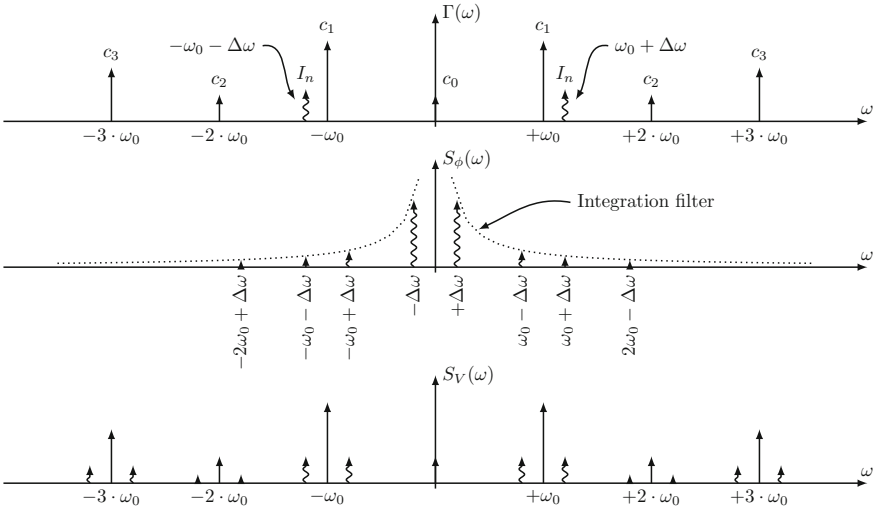

Fig. 3.5 An injected signal with amplitude I_n is converted to the spectrum of the excess phase $\phi(t)$. The signal is weighted by the Fourier coefficients of the ISF $\Gamma(x)$. Furthermore, a low-pass filtering is applied by the integral, in this way the signals close to the carrier or to one of the harmonics are dominant on the signals further away. The second step is the phase modulation of this excess phase. During this operation, the injected signal is up-converted to the carrier frequency (and to its harmonics)

$$v(t) = \Re\{A(t) \cdot e^{j\cdot\theta(t)} \cdot e^{j\cdot\omega_0\cdot t}\} \tag{3.25}$$

where $A(t) \cdot e^{j\cdot\theta(t)}$ is called the complex envelope of the signal [34]. For small phase deviations or for low-frequency phase changes (note that for noise signals this is always the case), the phase modulation is considered to be narrow-band angle modulation. The complex envelope is then approximated by its first-order Taylor expansion:

$$A(t) \cdot e^{j\cdot\theta(t)} \approx A(t) \cdot (1 + j \cdot \theta(t)) \tag{3.26}$$

The oscillator output voltage, i.e. the phase-modulated signal, for a sinusoidal noise input signal results in [using(3.24)]:

$$v(t) = A(t) \cdot \cos(\omega_0 \cdot t) - A(t) \cdot \theta(t) \cdot \sin(\omega_0 \cdot t) \tag{3.27}$$

$$= A(t) \cdot \cos(\omega_0 \cdot t) - A(t) \cdot \frac{I_n \cdot c_k \cdot \sin(\Delta\omega \cdot t)}{2 \cdot q_{\max} \cdot \Delta\omega} \cdot \sin(\omega_0 \cdot t) \tag{3.28}$$

Using again Simpson's formula, this formula results in two sidebands at $\omega_0 \pm \Delta\omega$. These sidebands are the result of using the LTV approach instead of the previously presented LTI approximation. In the latter case, an injected noise signal at $k \cdot \omega_0 + \Delta\omega$

can impossibly fold back around the natural frequency of the oscillator. Using (2.35) instead of (2.34) results in phase-modulated sidebands around each oscillator harmonic. The formula also shows the ratio of the (single) sideband power and the power of the carrier frequency:

$$P_{sbc}(\Delta\omega) = 10 \cdot \log\left(\frac{I_n \cdot c_k}{4 \cdot q_{\max} \cdot \Delta\omega}\right)^2 \tag{3.29}$$

Typically the unit dBc (dB compared to the carrier) is used for this ratio. Note, however, that due to the first-order Taylor expansion, the higher-order sideband peaks are neglected. *Carson's rule* states that 98 % of the total power of an angle-modulated signal is contained in the bandwidth [34]:

$$B_T = 2 \cdot (\beta + 1) \cdot B = 2 \cdot \left(\frac{I_n \cdot c_k}{2 \cdot q_{\max} \cdot \Delta\omega} + 1\right) \cdot \Delta\omega \tag{3.30}$$

where β is the phase modulation index and B is the bandwidth of the modulating signal. For injected signals which are small compared to the oscillator signal, this formula shows that most of the power is indeed in the two first-order sidebands at $\omega_0 \pm \Delta\omega$.

3.4.1.3 Application to an Injected Noise Spectrum

The next step is to apply this procedure to a complete noise spectrum. An overview is shown in Fig. 3.6. As shown previously, it is mainly the noise in the neighborhood of the oscillator harmonics which contributes to the low-frequency sidebands of $S_\phi(\omega)$. This PSD is therefore given by the sum of all noise contributions in the vicinity of the oscillator harmonics, weighted by the corresponding c_k. Next, these sidebands are transformed to close-in phase noise in the oscillator output spectrum $S_v(\omega)$. Assume that the injected noise spectrum consists of a $1/f$ noise region and a white noise region, then this results in a $1/f^3$ and a $1/f^2$ region around the oscillator frequency. The corner frequency between these two regions is *not* the same for the injected noise and for the up-converted phase noise since the noise in both regions is weighted by different scale factors c_k. In general, one can state that noise sources with a $1/f^n$ frequency dependence appear in the phase noise spectrum with a $1/f^{n+2}$ behavior.

Equation (3.29) can be used to calculate the total phase noise power in the sidebands. The injected noise in this case has a noise density $\overline{i_n^2}/\Delta f$, which is at each frequency equal to $I_n^2/2$ (the mean squared value of the injected signal). Furthermore, since both the injected noise at $k \cdot \omega_0 \pm \Delta\omega$ is transformed to phase noise at $\omega_0 \pm \Delta\omega$, a factor of 2 needs to be added. The total phase noise at frequency $\omega_0 + \Delta\omega$ is then [100]:

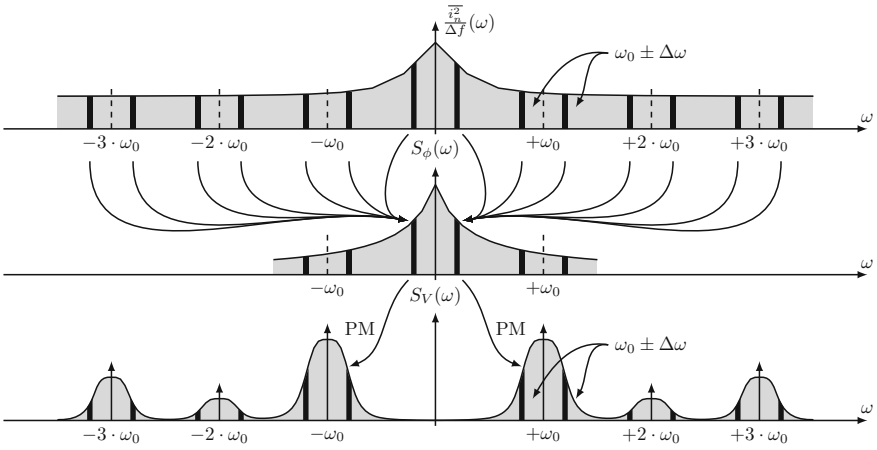

Fig. 3.6 Similar to Fig. 3.5, this figure shows the translation of a noise spectrum towards the oscillator phase noise spectrum. During the convolution of the ISF and the injected noise, the noise contribution around each harmonic of the ISF is translated into noise around zero in the spectrum of the excess phase $\phi(t)$. Keep in mind, however, that the noise contributions appear around each of the ISF harmonics but are filtered by the integral operator. During the phase modulation step, the spectrum is up-converted towards the oscillator center frequency and the harmonics. Although the LTV theory of Hajimiri predicts an infinite noise power close to the carrier, a Lorentzian spectrum is drawn

$$\mathscr{L}(\Delta\omega) = 10 \cdot \log\left(\frac{\frac{\overline{i_n^2}}{\Delta f} \cdot \sum_{k=0}^{\infty} c_k^2}{4 \cdot q_{\max}^2 \cdot \Delta\omega^2}\right) \tag{3.31}$$

This expression denotes the single-sideband noise of a (single-sided or positive) oscillator spectrum, symmetrical around the carrier. The sum can be simplified using Parseval's theorem (Theorem A.1):

$$\sum_{k=0}^{\infty} c_k^2 = \frac{1}{\pi} \cdot \int_0^{2\pi} |\Gamma(x)|^2 dx = 2 \cdot \Gamma_{rms}^2 \tag{3.32}$$

which results in the following expression for the $1/f^2$ noise of the oscillator at offset $\Delta\omega$:

$$\mathscr{L}(\Delta\omega) = 10 \cdot \log\left(\frac{\frac{\overline{i_n^2}}{\Delta f} \cdot \Gamma_{rms}^2}{2 \cdot q_{\max}^2 \cdot \Delta\omega^2}\right) \tag{3.33}$$

In a final step, the noise in the $1/f^3$ region needs to be quantified. A commonly used expression for the injected $1/f$ noise is:

$$\frac{\overline{i_{n,1/f}^2}}{\Delta f} = \frac{\overline{i_n^2}}{\Delta f} \cdot \frac{\omega_{1/f}}{\Delta\omega} \tag{3.34}$$

which is dominant in the noise spectrum for $\Delta\omega < \omega_{1/f}$. $\omega_{1/f}$ is the corner frequency of the device $1/f$ noise. In the $1/f^3$ portion of the phase noise spectrum the noise is then given by [100]:

$$\mathscr{L}(\Delta\omega) = 10 \cdot \log\left(\frac{c_0^2}{q_{\max}^2} \cdot \frac{\omega_{1/f} \cdot \overline{i_n^2}/\Delta f}{8 \cdot \Delta\omega^3}\right) \tag{3.35}$$

The $1/f^3$ corner of the phase noise is the frequency where the $1/f^2$ portion of the phase noise (3.33) is equal to the $1/f^3$ portion (3.35). This results in a corner frequency of:

$$\omega_{1/f^3} = \omega_{1/f} \cdot \frac{c_0^2}{4 \cdot \Gamma_{rms}^2} \tag{3.36}$$

The $1/f^3$ corner frequency is therefore always smaller than the $1/f$ corner frequency of the injected noise. The more symmetrical the oscillator waveform, the lower c_0 will be compared to the rms value of the waveform, and the lower the $1/f^3$ corner frequency will be compared to the $1/f$ corner frequency. A low $1/f$ device noise performance thus not necessarily implies a bad close-in phase noise performance.

3.4.2 Extensions to the Theory of Hajimiri

The basic principles behind the noise theory of Hajimiri have been discussed in the previous section. In this section a few extensions are briefly explained, relying on the same basic LTV theory.

3.4.2.1 Cyclostationary Noise Sources

Due to the fact that the cyclostationarity of the noise sensitivity is taken into account using the ISF, this noise theory delivers an efficient way to include cyclostationary noise sources. A cyclostationary noise source can be written as [101]:

$$i_n(t) = i_{n0}(t) \cdot \alpha(\omega_0 \cdot t) \tag{3.37}$$

where $i_n(t)$ is a cyclostationary noise source, $\alpha(\omega \cdot t)$ is a deterministic, periodic function with period 2π, normalized to have a maximum equal to 1 and $i_{n0}(t)$ is a stationary noise source (which possibly can be colored). In this way, $\overline{i_{n0}^2}$ is equal to

the maximum mean square noise power applied to the system. The influence of this noise source is then calculated using the superposition integral (3.20):

$$\phi(t) = \int_{-\infty}^{t} i_{n0}(\tau) \cdot \frac{\alpha(\omega_0 \cdot \tau) \cdot \Gamma(\omega_0 \cdot \tau)}{q_{\max}} d\tau \tag{3.38}$$

Since $\alpha(\omega_0 \cdot t)$ and $\Gamma(\omega_0 \cdot t)$ have the same period $2 \cdot \pi$, both functions can be taken together in one effective ISF:

$$\Gamma_{eff}(x) = \alpha(x) \cdot \Gamma(x) \tag{3.39}$$

When calculating the influence of cyclostationary noise sources, it is necessary to use this effective ISF to calculate the Fourier coefficients c_k. However, when cyclostationary as well as constant noise sources are present in the circuit, both calculations can be performed separately and added afterwards. This, as long as all noise sources are independent (which in most cases can be expected since the noise sources have a completely different origin).

3.4.2.2 Amplitude Noise

From the previous sections, it is clear that the close-in sidebands are completely dominated by the phase noise. The amplitude noise, on the other hand, has an impact on the far-out sidebands [151, 152]. Different from the excess phase $\phi(t)$, the effect on the instantaneous amplitude $A(t)$ decays over time. This is because of the amplitude restoring mechanisms in the oscillator circuit. In harmonic oscillators with a high Q factor, these restoring mechanisms will act rather slowly compared to in relaxation oscillators or ring oscillators. In the case of an under-damped amplitude regulation (see Sect. 2.2.4), this amplitude decay is also under-damped. Similar to the calculation of the phase noise, the sensitivity of an oscillator's amplitude to an injected charge (normalized to the maximum charge in the circuit) can be calculated. The impact on the amplitude is written as:

$$\Delta A = \frac{\Lambda(\omega_0 \cdot t) \cdot \Delta q}{q_{\max}} \tag{3.40}$$

where Δq is the injected charge and $\Lambda(x)$ is the amplitude impulse sensitivity function (A-ISF). This function has similar properties in terms of periodicity and magnitude as the ISF $\Gamma(x)$. The amplitude impulse response can be calculated as follows:

$$h_A(t, \tau) = \frac{\Lambda(\omega_0 t)}{q_{\max}} \cdot v(t - \tau) \tag{3.41}$$

where $v(t-\tau)$ determines the decay of the excess amplitude. For most oscillators the amplitude restoring mechanism is a first- or second-order system, which results for $v(t-\tau)$ in a decaying exponential or a damped sinusoid. Similar to (3.20), the excess instantaneous amplitude for an arbitrary noise input $i_n(t)$ is calculated using the superposition integral [151]:

$$A(t) = \int_{-\infty}^{\infty} \frac{i_n(\tau)}{q_{\max}} \Lambda(\omega_0 t) \cdot v(t-\tau) d\tau \tag{3.42}$$

For a first-order amplitude regulation this translates to [151]:

$$A(t) = \int_{-\infty}^{\infty} \frac{i_n(\tau)}{q_{\max}} \Lambda(\omega_0 t) \cdot e^{-\omega_0 (t-\tau)/Q} u(t-\tau) d\tau \tag{3.43}$$

where the exponential function implements the excess amplitude decay, Q is the Q factor of the oscillator and $u(t-\tau)$ is the unit step function. Again, the A-ISF $\Lambda(x)$ is a periodic function which can be transformed to a Fourier series. Using the same procedure as for the calculation of the excess phase, the power spectrum of the amplitude noise results in [108, 151]:

$$\mathscr{A}(\Delta\omega) = \frac{\Lambda_{rms}^2}{q_{\max}^2} \cdot \frac{\overline{i_n^2}/\Delta f}{2 \cdot \left(\frac{\omega_0^2}{Q^2} + \Delta\omega^2 \right)} \tag{3.44}$$

This amplitude noise spectrum is added to the phase noise spectrum. As mentioned earlier, however, the noise to the carrier is mainly determined by the phase noise and not by the amplitude noise. The amplitude noise is mostly observed around an offset frequency of $\Delta\omega = \omega_0/Q$, where it causes a pedestal in the oscillator spectrum. In some cases, however, the amplitude noise disappears completely under the (phase) noise floor.

3.4.3 Calculation of the ISF

To obtain a correct prediction of the phase noise in an oscillator circuit, the ISF must be calculated. Different methods to do so are described in [101, 108, 151].

3.4.3.1 Numerical Simulation of the ISF

The first method is to do a small charge injection at different moments in the oscillator period in a SPICE-like transient simulation. By simulating the next few cycles of the oscillator, it is possible to measure the impact of the charge injection on the zero crossings of the oscillator. When a phase shift Δt is measured, the excess phase can be calculated by noting that $\Delta\phi(t) = 2\pi\,\Delta t/T$ where T is the oscillation period. Once the impulse response is obtained as a function of the moment of impact, the ISF can be calculated by multiplication with $q_{\max}$.

3.4.3.2 Analytical Calculation Method

A second method to calculate the ISF is derived in [101] and relies on the trajectories in the state space of the oscillator. By analyzing the projection of an injected current pulse on the oscillator phase space trajectory, the excess phase as a result of the injected charge can be calculated. From this, a closed form of the ISF can be obtained. Assume that the different state variables f_i correspond to the voltages on the different nodes in the circuit normalized to amplitude and frequency [defined in (2.35)], then:

$$\Gamma_i(x) = \frac{f_i'}{\sum_{j=1}^{n} f_j'^2} \tag{3.45}$$

In case that not all state variables correspond to a node voltage, they correspond to another state in the oscillator circuit. As long as the voltage on node i corresponds to the state variable f_i, the ISF for an *applied current impulse* at node i can be calculated using this formula. For a second-order system (for instance an LC tank), the voltage on the output node and its derivative can therefore be used as the state variables. The formula for the ISF then reduces to:

$$\Gamma(x) = \frac{f'}{f'^2 + f''^2} \tag{3.46}$$

A final method to calculate the ISF is a simplified version of the previous formula and only uses the first derivative of the output signal. In many cases, the denominator of (3.45) is relatively constant. This is for instance the case in a ring oscillator [101]. The ISF can then be approximated by:

$$\Gamma_i(x) \approx \frac{f_i'(x)}{f_{\max}'^2} \tag{3.47}$$

where $f'_{\max}$ is the maximum 2-norm of the vector with derivatives of the voltages on the different nodes. This approximation, however, needs to be used with great care.

It is therefore advised to use the first or second method instead. Also note that the different methods can be used to verify each other's results.

3.4.3.3 Calculation of the A-ISF

Also for the A-ISF, an analytical calculation method can be used. In [108], expressions for both the (P-)ISF and the A-ISF are derived. Since the magnitude of these functions is proportional respectively to the tangential and the orthogonal component of the impact vector[1], it appears that there is a close connection between both functions. Similar to (3.45), the A-ISF can be calculated as:

$$\Lambda_i(x) = \sqrt{1 - \frac{f_i'^2}{\sum_{j=1}^{n} f_j'^2}} \tag{3.48}$$

or, as a function of the (P-)ISF:

$$\Lambda_i(x) = \sqrt{1 - f_i' \cdot \Gamma_i(x)} \tag{3.49}$$

In the following chapters, it will become clear that the analytical method is, as usual, the most useful to gather insight in the noise performance of a system.

3.4.4 Evaluation of Hajimiri's Theory

Although previous noise theories, starting from an LTI approach, offered useful qualitative insights, the phase noise theory of Hajimiri relies on a completely different mechanism. The results often correspond accurately to measurement results [101, 102, 104, 151]. Furthermore, because of the use of the ISF, the theory offers a high insight in the phase noise generation and up-conversion mechanism and can be used at design time to optimize the expected phase noise performance.

The Hajimiri theory, on the other hand, also has some shortcomings. First of all, the oscillator is treated as a linear system, which in reality is not always the case. The nonlinearities in the circuit, however, determine the oscillator output waveform and are therefore taken into account when using the ISF. Furthermore, it is observed in [101, 151] that the linearity holds up till relatively high injected amplitudes for the generation for the excess phase. Secondly, it uses a linear approximation of the complex envelope in (3.26). Since phase modulation is a strongly nonlinear process, this approximation only holds for small values of the excess phase. The third weakness is the infinite noise density around the carrier, which is not possible

[1] Note that this assumption, which is also used in [121] and seems perfectly intuitive in an LTV approach, was previously shown to be invalid [69, 70].

in a real system and complicates the calculation of the resulting timing jitter. As will be seen in the next section, a nonlinear approach is needed to overcome this infinite-noise-density problem and to obtain the correct (finite) spectrum.

3.5 Nonlinear Noise Theories

None of the discussed noise theories up till now results in a complete description of the noise behavior. In [121] an approach similar to Hajimiri is used, to split the noise into two orthogonal components $\phi(t)$ and $A(t)$. Using nonlinear equations instead, this results in a Lorentzian spectrum around the oscillator harmonics as a result of random (white) noise. This nonlinear theory, despites its general and rigorous treatment of phase noise, lacks quantitative and experimental results and has some shortcomings considering the solution of the differential equation of the phase error [67].

In [70] an attempt is done to obtain a *unifying theory* resulting in quantitatively correct predictions. To reach this goal, again a nonlinear approach has been taken. The oscillator is modeled by a nonlinear differential equation on which a perturbation is applied. Using Floquet theory, an equation for the phase error is obtained and solved. In a next step, by applying a noise spectrum to the oscillator, the phase noise spectrum can be obtained. These spectra are close to what is measured in practical implementations.

3.5.1 The Lorentzian Spectrum

In the absence of $1/f$ noise and neglecting the noise floor, a Lorentzian spectrum of phase noise is obtained around every harmonic of the oscillator [68, 70, 203]:

$$\mathscr{L}(\Delta f) = \frac{1}{\pi} \cdot \frac{\pi \cdot f_0^2 \cdot c}{(\pi \cdot f_0^2 \cdot c)^2 + \Delta f^2} \tag{3.50}$$

where c is a constant determining the spread of the spectrum. In this equation, as will be seen later, the term $\pi \cdot f_0^2 \cdot c$ is often substituted by γ. It is clearly visible that this spectrum does not reach infinity when approaching the carrier. Furthermore, the integral of this spectrum (3.50) divided by the power of the considered harmonic, is constant and equal to 1, independent of c, which denotes that the noise of the oscillator does not change the output power but spreads it over a broader spectrum. Note that this spectrum has a similar asymptotic behavior for large Δf as the spectrum predicted by Hajimiri's theory.

The difference between the linear and the nonlinear theories for frequencies close to the carrier frequency is mainly a result of the linear approximation of the phase

modulation step. Except from these nonlinearities, there is no reason to assume that a free running VCO is NOT an ideal integrator with an unbounded output value [104, 137]! In [203] the spectral line width of an oscillator is, similar to what's used in optics, defined as the half power width:

$$\Delta f_{-3dB} = 2 \cdot \pi \cdot f_0^2 \cdot c \tag{3.51}$$

The phase noise at offset frequencies larger than 1 Hz will always be lower than 0 dBc/Hz. At frequencies lower than 1 Hz, even in a low-noise oscillator, the phase noise power will be higher than 0 dBc/Hz. This is, however, exactly what is to be expected: a sharp peak in the spectrum representing the carrier frequency. The total power over a 1 Hz bandwidth will be equal to one. When the noise increases, however, the spectral line width will be greater than 1 Hz. The phase noise spectrum in this case is flat for frequencies lower than Δf_{-3dB}. This shows the high spectral line width of the oscillator and is compatible with the predicted Lorentzian spectrum.

Apart from this, this nonlinear theory also shows the stationarity of the noise at the oscillator output [70]. This seems strange at first sight since the oscillator is often treated as a cyclostationary process. Cyclostationarity, however, would by definition imply a time reference [69, 70]. The stationarity therefore reflects the fundamental fact that a noisy autonomous system cannot provide a perfect time reference. In a forced system, such as a PLL or an injection-locked oscillator, this is not the case (the stochastic process can be understood to be *reset* every cycle), and it can serve as a time reference. As mentioned previously, the nonlinear approach also shows that the amplitude and phase are oblique, not orthogonal.

3.5.2 The Gaussian Spectrum

As seen in [104], $1/f$ colored noise injection results in a $1/f^3$ slope in the output power spectrum close to the carrier and the harmonics. The spectrum is thus no longer Lorentzian as in the case of only white noise. The theory of Herzel [110] decomposes the spectrum in a Lorentzian and a Gaussian component. The resulting spectrum is the convolution of both spectra:

$$S_{Herzel}(\Delta\omega) = \frac{S_N}{4} \cdot \frac{\omega_{-3dB}^2}{\gamma} \cdot \pi \cdot \int_{-\infty}^{\infty} G[\sigma, \omega'] \cdot L[\gamma, \Delta\omega - \omega']d\omega' \tag{3.52}$$

$$\text{where: } G[\sigma, \omega] = \frac{1}{\sqrt{2 \cdot \pi} \cdot \sigma} \cdot e^{-\frac{\omega^2}{2 \cdot \sigma^2}} \tag{3.53}$$

$$L[\gamma, \omega] = \frac{1}{\pi} \cdot \frac{\gamma}{\gamma^2 + \omega^2} \tag{3.54}$$

where S_N is the constant value of the white input noise spectrum and ω_{-3dB} is the bandwidth at half maximum (equal to ω_n/Q, Definition 2.2). The parameters σ and γ depend on the injected noise density; in this model σ is equal to the standard deviation of ω_0 and γ is equal to the half-width at half maximum of the oscillator transfer function (3.12):

$$\gamma = (1 - G \cdot R_p) \cdot \frac{\omega_n}{2 \cdot Q} = \pi \cdot f_n^2 \cdot c \approx \pi \cdot f_0^2 \cdot c. \tag{3.55}$$

The Lorentzian and Gaussian spectrum avoid the singularity around the carrier which is resulting from Hajimiri's theory. In [110] it is stated that this expression holds as long as the applied noise is Gaussian, which is even for colored noise sources, although often considered to be correlated, a good approximation. Note, however, that this theory is based on the shaping of the input noise spectrum (similar to the noise theory of Leeson). As shown previously, this is not the most realistic noise-shaping mechanism. The resulting noise spectrum is called a Voight line profile, for which there is no analytical expression [110, 203]. At small offsets the spectrum looks Gaussian (when dominated by flicker noise), followed by a $1/f^3$ slope and finally a $1/f^2$ behavior and ultimately a flat spectrum.

In [136, 137] a nonlinear model is used to model the shape of the spectrum using an up-conversion mechanism (a random frequency modulation). Close to the carrier indeed a Gaussian spectrum is obtained, which shifts, for higher frequency offsets, smoothly towards a $1/f^\alpha$ slope. This work also discusses the amplitude-to-phase-caused phase noise (because of the non-orthogonality of the amplitude and phase components). Similarly, in [67], a Lorentzian spectrum is combined with another complex spectrum (similar to a Gaussian distribution) for the colored noise sources. The border between the two regions and numerical results are, unfortunately, not discussed. Note that the complex spectrum obtained for colored noise sources, can be approximated by a Lorentzian multiplied by the spectrum of the injected noise [67]. In [68] the same theory is described, be it accompanied with some more examples.

The nonlinear noise theories all predict a similar behavior for white and colored noise sources, despite their slightly different approach. Since these theories all attempt to find an exact solution to the oscillator equation, without doing initial assumptions or simplifications, they are believed to be closest to the real situation. In [70] a numerical simulation algorithm is derived from the model in [67] (considering, however, only white noise sources).

3.5.3 Evaluation

It has been shown that relying only on linearizations is not sufficient to obtain correct results in all areas of the phase noise power-law spectrum and in the neighborhood of the oscillator carrier. The actual derivation of the nonlinear noise theories, however, falls beyond the scope of this work. Furthermore, because of the high mathematical

complexity, the practical use of nonlinear noise theories is limited to computer simulations where it can provide accurate numerical results at a speed-up of up to 3 orders of magnitude compared to Monte-Carlo noise simulations [70]. In [185] a circuit model, based on this theory, is developed. In the remainder of this work, it will be shown experimentally that the LTI model of Leeson and the LTV theory of Hajimiri are sufficiently accurate for use at design time. In [269] it is shown that the results of the LTV theory compare well to the nonlinear theories in case of stationary noise sources, which is the case in free-running oscillators. In Chap. 7 it is shown that the spectrum of injection-locked oscillators is indeed somewhat different. As shown in [102–104], the LTV theory results in quantitatively correct results in the $1/f^2$ area of the noise spectrum. As will be seen in the next section, with respect to the cycle-to-cycle jitter, this is the most important region.

3.6 Phase Noise Versus Jitter

A tight connection exists between phase noise and jitter. Whereas the phase noise spectrum is a frequency-domain defined quantity, the jitter is the uncertainty in the time domain caused by this phase noise. This means that it is theoretically possible to obtain the jitter from the phase noise spectrum. However, this calculation is often complicated by unknown parameters such as the exact shape of the spectrum or singularities in the noise spectrum. The inverse operation (scalar to spectrum) is impossible unless also other information on the spectrum is known.

3.6.1 Definition of Jitter

Different definitions of jitter can be used. In general, jitter is defined as a statistical measure of a noisy oscillation process. Due to the noise in the circuit, a variation exists in the time between the subsequent zero crossings of the oscillator output signal. Hence, the period of each oscillation cycle will be slightly different. For a free running (noisy) oscillator, the oscillation period is expected to have a Gaussian distribution with a mean τ_{avg} and a standard deviation σ_c. This average is related to the frequency, $f = 1/\tau_{avg}$.

3.6.1.1 The Absolute Jitter

A first measure for the jitter is called the absolute or long-term jitter $\sigma_{abs}(t)$:

Definition 3.1 For an oscillator with a Gaussian-distributed period and an average period equal to τ_{avg}, the absolute or long-term jitter is defined as the sum of each period's variation from the average:

$$j_{abs}(t = N \cdot \tau_{avg}) = \sum_{i=1}^{N} \tau_i - \tau_{avg} \tag{3.56}$$

where τ_i is the length of the i-th oscillation period. The variance of this measure is sometimes also referred as the absolute jitter [67, 203]:

$$\sigma^2_{abs}(t = N \cdot \tau_{avg}) = E\left[\sum_{i=1}^{N} \tau_i - \tau_{avg}\right]^2 \tag{3.57}$$

The absolute jitter therefore depends on the observation time. The variance σ^2_{abs} of this measure diverges as time goes to infinity. On the other hand, however, when time goes to infinity, the absolute jitter goes to zero, since the average of τ_i will converge towards τ_{avg} for an infinitely high number of cycles. Because of its observation time dependence, the absolute jitter is not an interesting measure to quantify the noise in free-running oscillators. Every uncertainty in an early transition will affect all the following transitions and therefore the uncertainty will only accumulate [104]. The accumulated uncertainty over a time t can also be expressed as [70]:

$$\sigma^2_{abs}(t) = c \cdot t \tag{3.58}$$

where c is a scalar constant, which has the same value as in the noise distribution (3.50). Since a Lorentzian spectrum is assumed, this expression is only valid in the absence of colored noise! If different noise sources are present in the circuit, the resulting variances of the noise sources add up when calculating the resulting jitter, as long as the sources are random and uncorrelated.

3.6.1.2 The Cycle-to-Cycle Jitter

To obtain a time-independent value, the jitter can also be defined as the cycle-to-cycle jitter:

Definition 3.2 For an oscillator with a Gaussian-distributed period and an average period equal to τ_{avg}, the cycle-to-cycle jitter σ_c is defined as

$$\sigma_c^2 = \lim_{N\to\infty}\left(\frac{1}{N}\sum_{i=1}^{N}(\tau_i - \tau_{avg})^2\right) \tag{3.59}$$

where τ_i is the length of the i-th oscillation period. The cycle-to-cycle jitter is therefore an rms value and equal to the standard deviation of the oscillation period.

As opposed to Hajimiri and Demir, the cycle-to-cycle jitter is called cycle jitter by Herzel in [110]. Since the uncertainty on the length of an oscillation period is a random process over different periods, the relationship with the absolute jitter is rather straightforward. The cycle-to-cycle jitter can therefore be expressed as:

$$\sigma_c^2 = \frac{\sigma_{abs}^2(t)}{f_0 \cdot t} = \frac{c}{f_0} = \sigma_{abs}^2(t = 1/f_0) \tag{3.60}$$

This measure describes the magnitude of the period fluctuations but contains no information on the long-term fluctuations due to $1/f$ noise. A third definition of jitter, which is actually an alternative definition of the cycle-to-cycle jitter, is the variance of the length of successive periods, as defined in [110]:

Definition 3.3 For an oscillator with a Gaussian distributed period with an average period equal to τ_{avg}, the cycle-to-cycle jitter σ_{cc} is defined as

$$\sigma_{cc}^2 = \lim_{N\to\infty}\left(\frac{1}{N}\sum_{i=1}^{N}(\tau_{i+1} - \tau_i)^2\right) = 2 \cdot \sigma_c^2 \tag{3.61}$$

where τ_i is the length of the i-th oscillation period.

The interesting aspect about this measure for jitter is that, different from the previous definition, it partially compensates for possible drift in the phase and/or frequency. It will be seen below that these trends can occur in the case of colored noise sources. The relationship between both definitions ($\sigma_{cc}^2 = 2 \cdot \sigma_c^2$) is then of course no longer valid. In practice, however, for the case of a free running oscillator, it is mostly the cycle-to-cycle jitter σ_c which is used.

3.6.2 Only White Noise Sources

When only white noise sources are present, starting from a certain offset frequency on, the phase noise displays a −20 dBc/Hz frequency dependency. The phase noise in this frequency span can then be related to the rms jitter by [203]:

$$\mathscr{L}(\Delta f) = \frac{\sigma_c^2 \cdot f_0^3}{\Delta f^2} \tag{3.62}$$

This can easily be shown using (3.50). Above the pole frequency, the spectrum can be approximated by:

$$\mathscr{L}(\Delta f) = \frac{1}{\pi} \cdot \frac{\pi \cdot f_0^2 \cdot c}{\Delta f^2} \tag{3.63}$$

Substituting c using Eq. (3.60) results in the above relationship. Although the situation without $1/f$ noise hardly exists in practical implementations, this formula is often used. Indeed, in short-term measurements, the $1/f$ noise impact will not be visible.

3.6.3 Colored Noise Sources

The relation between the phase noise and the jitter becomes more complicated when also colored noise is injected in the oscillator. The uncertainty on the subsequent zero crossings is no longer uncorrelated since a high amount of low-frequency noise is present in the circuit. Hajimiri states that in this case rather the standard deviation than the variance of the noise must be integrated over time [104]. This can be understood by thinking of random noise sources at multiple frequencies modulating the frequency of the oscillator [110]. When a 'low-frequency' event at frequency f_1 is injected in the oscillator, it will last for a significant time $t_1 \propto 1/f_1$. In the neighborhood in time of this event, because of the low-frequent character of the noise, the mean period will be different to periods which are further away in time. Only when the signal statistics are calculated over an interval larger than t_1, the influence of this low-frequency noise will be seen. In a free running oscillator, this jitter will accumulate, similar to (3.58). Over a small time interval, (3.58) holds, since the effect of the $1/f$ noise cannot be observed yet. Due to the correlation of these noise injections over time, however, there will be a significant influence at larger time intervals. The variance of the absolute or long-term jitter can then be approximated by [203]:

$$\sigma_{abs}^2(t) = c \cdot t + \kappa \cdot t^2 \tag{3.64}$$

where κ is a noise constant depending on the $1/f$ noise processes in the oscillator. When the timing jitter σ_{abs} is plotted over time on a log-log scale, there will be a region with a slope of 1/2, followed by a region with a slope of 1.

3.6.4 General Calculation Method

Different equations have been published in literature to link the oscillator spectrum mathematically to the output jitter. Assuming that $S_\phi(f)$ is the spectral density of the phase noise (not the amplitude noise), Hajimiri predicts the absolute jitter to be [104]:

$$\sigma_{abs}^2(t) = \frac{4}{\omega_0^2} \int_{-\infty}^{\infty} S_\phi(f) \cdot \sin^2(\pi \cdot f \cdot t) df \tag{3.65}$$

When the noise spectrum has a $1/f^2$ slope (which is what Hajimiri predicts in case of only white noise sources), indeed this integral will converge. Another equation, proposed by Zanchi in [322], predicts the cycle-to-cycle jitter σ_c to be:

$$\sigma_c^2 = \frac{1}{f_0^4} \int_{-\infty}^{\infty} f^2 \cdot S_\phi(f) \cdot |\operatorname{sinc}(\pi \cdot f/f_0)|^2 df \tag{3.66}$$

where f_0 is the oscillation frequency.[2] Although this expression was published as a general link between phase noise and jitter, it can only be used in the absence of $1/f^3$ noise, or when used in a closed-loop PLL measurement setup. In open loop, due to the drift caused by the colored noise, the cycle-to-cycle jitter diverges anyhow. In Appendix C an elaborate discussion is held on these measurement issues. Furthermore, a general method to overcome these convergence problems in case of higher-order noise sources, is presented in the appendix. By the application of the Wiener-Khinchine theorem [34], this general method results in exactly the same expression. The last equation, proposed by Demir in [67], uses a complex exponential instead of a sine function [203]:

$$\sigma_{abs}^2(t) = c \cdot t + \int_{-\infty}^{\infty} S_{\phi,f}(f) \cdot \frac{1 - e^{j \cdot 2 \cdot \pi \cdot f \cdot t}}{4 \cdot \pi^2 \cdot f^2} df \tag{3.67}$$

where $S_{\phi,f}(f)$ is the spectrum of only the $1/f$ phase noise components and is assumed to be confined. The first term of the jitter is coming from the white noise contributions. Because of the two terms, this equation probably comes the closest

[2] In [203] it is wrongly stated that this formula results in the absolute jitter. The absolute jitter can be obtained from this using (3.64).

to the jitter characteristic of Eq. (3.64). Note, however, that none of these three equations has ever been validated or compared to each other [203]; they all connect an arbitrary noise spectrum to the absolute jitter. In practice, most often the jitter is measured over a short time, so that the $1/f$ noise can be neglected, and the phase noise is characterized by its $1/f^2$ spectrum. Anyhow, for a free-running oscillator, only this part of the spectrum has a significant influence on the cycle-to-cycle jitter, as was shown in the previous section.

3.7 The Q Factor and the Noise

It is often believed that an inversely proportional relation exists between the Q factor of an oscillator and the noise performance. This is clearly visible in some of the noise theories. In other models, however, this relationship is less obvious. In this section a short overview is given between the different noise theories and the influence of an increasing Q factor on their output noise spectrum.

3.7.1 The Theory of Leeson

In Leeson's approximation of the noise spectrum (3.17), it is assumed that the (white) input noise is shaped by the bandpass filter implemented by the oscillator tank. As shown in the discussion about the Q factor, one of the definitions of Q is related to the bandwidth of the resonant peak (Fig. 2.10). In this case the relationship between the noise spectrum and the Q factor is rather straightforward as shown in (3.16). Using (3.62), the relationship between the jitter and the Q factor is given by:

$$\sigma_c^2 = \frac{F \cdot k \cdot T}{2 \cdot f_0 \cdot P_s \cdot Q^2} \tag{3.68}$$

From this equation it is clear that the jitter is indeed determined by the Q factor.

3.7.2 The Theory of Hajimiri

The resulting noise spectrum using the theory of Hajimiri does not show the straightforward relationship with the Q factor. The output spectrum (as a result of white input noise) is given by (3.33). Different parameters in this equation, however, are related to the Q factor. Since the Q factor is proportional to the parallel resistance in the tank (2.64), the amplitude of the current noise source is lower for tanks with a higher Q. However, the noise sources in the oscillator consist mainly of transistor noise [102]; hence, this cannot be the only reason of the improved noise performance. A second

parameter which has a significant influence is the ISF or, more specifically, the spectral purity of the oscillator output. For a single-tone output signal, the ISF results in a sine wave. In this case the rms value of the ISF is equal to $\Gamma_{\max}/\sqrt{2}$. When the Q factor lowers, the waveform is less filtered, which often results in distortion due to the nonlinearities in the gain stage. As shown in Fig. 3.6, it is the noise around each harmonic of the ISF which contributes to the total noise spectrum. In the final spectrum, these contributions are included in the rms value of the ISF, which causes an increase compared to a non-distorted waveform. A final, but probably the most important link between Q and the noise performance follows from the first Definition (2.56). Due to the reduced losses in the tank, the feedback amplifier only needs a smaller g_m in order to meet the Barkhausen criterion. From (3.9) it follows that the injected noise in this case is lowered drastically.

3.8 Figures of Merit

As for many electrical circuits, a Figure of Merit (FoM) has been defined which takes several performance characteristics together in one figure. It is important that this figure takes the trade-offs between the different parameters into account. When comparing circuits, this is necessary to obtain a fair comparison. However, even the most balanced FoM needs to be used with care: optimization towards a certain FoM can be completely incompatible with certain applications or constraints in a system application.

3.8.1 The Phase Noise FoM

In the case of phase noise, an inversely proportional relationship exists with the power consumption. A well-developed FoM makes sure that these effects cancel each other. Nevertheless, each circuit has its optimum biasing point or environmental parameters at which the FoM is the highest. A commonly used FoM to measure the phase noise is given by [134]:

$$FoM_{PN} = 10 \cdot \log\left(\frac{1}{\mathscr{L}\{\Delta\omega\} \cdot P} \cdot \left(\frac{\omega_0}{\Delta\omega}\right)^2\right) \tag{3.69}$$

where the power consumption P is expressed in milliwatt.[3] As can be seen, this FoM has a constant value as long as the measurement is done in the $1/f^2$ region of the noise spectrum. This FoM is developed for oscillators with a constant output frequency. To take the noise degradation as a result of the tuning gain into account,

[3] Note that often the inverse value of this FoM is used, resulting in a $-$ sign.

e.g. in VCOs, an extra term has been added to this equation [49]:

$$FoM_{PN,tuned} = FoM_{PN} + 10 \cdot \log\left(\frac{tuning}{V}\right) \tag{3.70}$$

where the $tuning$ range is expressed in percents relative to the center frequency. Interesting to note is that for some implementations, an upper bound of this FoM (3.69) can be calculated. In [187] this exercise is performed for RC relaxation oscillators and ring oscillators. In [91] this is done for IV-C-relaxation oscillators (using an V-I ratio rather than a resistor). The resulting conclusions are shown in Table 3.1. Note, however, the big discrepancy between the theoretical limits and practical implementations for relaxation oscillators. The IV-C implementation in [90] attempts to bridge this gap, as explained in [91]. This implementation will briefly be discussed in Sect. 4.4.2. For an LC oscillator, a similar bound can be calculated, depending on the Q factor. Although the noise in an LC oscillator is often dominated by the amplifier, the theoretical maximum only takes the thermal noise and losses in the tank itself into account. Using Hajimiri's noise theory and (2.56), applied to the parallel RLC network of Fig. 2.9, the upper bound for the phase noise FoM in an LC tank is calculated to be (the noise calculation in an LC oscillator is discussed into more detail in Sect. 6.5):

$$FoM_{PN,LC} = 10 \cdot \log\left[\frac{2 \cdot Q^2}{k \cdot T}\right] \tag{3.71}$$

This expression, however, results in an unrealistically high phase noise FoM. Using (3.9) and (2.76), the channel noise of an amplifier with a constant g_m is added, which adds an extra factor of 3/5. This, however, is assumed to be an underestimate of the real impact [103, 151]. Note that the power consumed in the amplifier is also not taken into account.[4] The Q factor of an integrated LC tank is typically ranging between

Table 3.1 Maximum limits of the phase noise FoM

Topology	$FoM_{\max}$ (dB)	Practical designs (dB)
Ring oscillators	165	158–163
Relaxation RC-oscillators	169	145–155
Relaxation I-C-oscillators	165	<162
LC oscillator (tank)	222.7 ($Q = 8$)	150–195

[4] Certainly when using a constant-g_m amplifier (class A), the power efficiency expected to be poor.

4 and 8 [138], resulting in an upper bound of 222.7 dB. In [49, 134] an overview of existing LC implementations is given. In Sect. 4.4.1.1, different implementations will be discussed, mainly focusing on PVT-stability.

3.9 Conclusion

In this chapter, the different noise sources and mechanisms behind oscillator phase noise have been discussed. An explanation has been given for the conversion of the input noise spectrum to the oscillator's output spectrum. In the remainder of this work, these mechanisms will be used to better understand the behavior of the proposed oscillator designs. In a last step, also the connection has been made between the phase noise spectrum and the timing jitter in the oscillator output signal. As shown in Appendix C, this relationship results in several issues at measurement time when colored noise sources are included. Apart from the classically used phase noise measures, alternative measures to overcome these difficulties are defined in the appendix.

Chapter 4
Long-term Oscillator Stability

Clock drift is a phenomenon present in every physical oscillator. The causes of clock drift are very diverse, going from mismatch between clocks or between their environments to charges injected from external radiation. Modern atomic clocks, however, are often more accurate than the rotation of the earth itself [295]. *One very particular source of clock drift, which has an impact on* any *clock, is time dilation as described by Einstein's theory on special and general relativity. Although these effects only count for high speeds and gravitational fields, several high-accuracy applications exist in which the correction for clock drift is indispensable. If the atomic clock of a GPS satellite is not corrected for these effects, it results in a 38 μs or 10 km positioning error* every day [202]. *Although this effect is elaborately documented and believed to be understood, corrections from ground stations are used to decrease the remaining time errors* [239].

4.1 Introduction

When talking about long-term frequency stability, in this work this is considered to be the process, temperature and/or supply voltage (PVT) stability. However, ultra-low-frequency phase noise can also be considered to be long-term frequency instability and vice versa. The general discussion about noise can be found in Chap. 3. It is observed that the time constants of most external variations are much longer than the time constants of internal variations. Transistor aging effects, for instance, are a possible exception to this, but fall beyond the scope of this work [65, 172].

4.1.1 Causes of Frequency Drift

The PVT sensitivity depends on many parameters such as technology, circuit topology, component properties, etc. Although it is often an important specification in oscillator design, the fact that there are several ways to obtain frequency accuracy

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and even more to ruin it, makes it difficult to define general design rules. In [174] it is stated that 4 sources of frequency drift can be defined in an oscillator. Here, a fifth cause is added.

1. Colored noise can result in a frequency perturbation due to nonlinear effects [169].
2. Variations in the harmonic content in the oscillator signal which is injected in the tank.
3. A variation of the tank components (R, L and C), often caused by non-constant parasitics due to the amplifier circuit or switches.
4. Non-constant losses in one of the tank components, resulting in the oscillator frequency ω_0 differing from ω_n.
5. Instabilities in the oscillation amplitude.

The first source of frequency drift can be assumed to be negligible compared to the other sources. The second source is the result of harmonics in the oscillator signal (a non-sinusoidal oscillator output) which cause a harmonic work imbalance (HWI) in the tank. This has to be compensated by a small downwards frequency shift, as will be discussed in Sect. 4.2. The third cause for an unstable output frequency is probably the most important and is discussed in Sect. 4.2. A finite Q factor can result in a frequency shift compared to the natural frequency of the tank, as already shown in Sect. 2.5.1. The last cause of a frequency shift is an unstable amplitude. This simply follows from the differential equation from a harmonic oscillator. A discussion on this will be found in Chap. 5.

4.1.2 Organization of this Chapter

This chapter is organized as follows. In Sect. 4.2 the components of the oscillator will be discussed. It will be shown that these components have a crucial impact on the waveform, which in turn influences the output frequency. Also the temperature impact on these components will be investigated. The different available passives and their main properties will be discussed in Sect. 4.2.4. Next, in Sect. 4.3, different FoMs for long-term frequency stability will be introduced and compared. Different existing implementations from literature and their properties will be discussed in Sect. 4.4. Finally, in Sect. 4.5, conclusions will be drawn before going to the different oscillator implementations.

4.2 Building Blocks of an Oscillator

To obtain a stable oscillation, the losses present in any tuned network need to be compensated by an amplifier circuit. A typical oscillator topology is shown in Fig. 4.1, in which $H(s)$ is the tuned feedback network and $G(s)$ is the gain or *negative resistance*

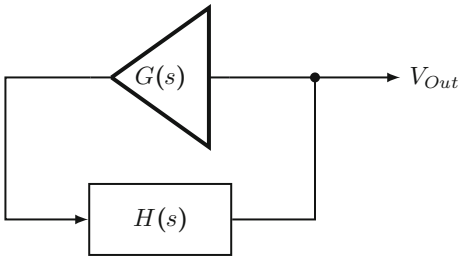

Fig. 4.1 Typical block diagram of a harmonic (linear) oscillator

which compensates for the losses. The Barkhausen criterion (Theorem 2.2) is used to determine the necessary gain and to calculate the oscillation frequency. Using this linear oscillator model, it is mostly assumed that the frequency is completely determined by the feedback network.

4.2.1 Linear Oscillator Systems

When both the feedback network and the amplifier are perfectly linear, determining the gain and oscillation frequency is rather straightforward. A second-order transfer function can be written in its standard form (2.66). When using a frequency-independent amplifier, the Barkhausen criterion results in:

$$\frac{\frac{s}{C}}{s^2 + \frac{1}{C \cdot R_P} \cdot s + \frac{1}{L \cdot C}} \cdot G = 1. \tag{4.1}$$

Substituting $s = j \cdot \omega$ results in two equations:

$$\begin{cases} \frac{1}{L \cdot C} - \omega^2 = \omega_n^2 - \omega^2 = 0 \\ j \cdot \omega \cdot \left(\frac{1}{R_p} - G \right) \cdot \frac{1}{C} = j \cdot \omega \cdot \left(\frac{\omega_n}{Q} - \frac{G}{C} \right) = 0 \end{cases} \tag{4.2}$$

From the first equation, the oscillation frequency f_0 can be calculated. The second equation shows that the transconductance amplifier behaves as a linear negative resistance. Assuming that the amplifier is frequency dependent:

$$G(s) = \frac{G}{1 - s/p} \tag{4.3}$$

where p is the pole frequency, then the Barkhausen criterion results in:

$$\frac{\frac{s}{C}}{s^2 + \frac{1}{C \cdot R_P} \cdot s + \frac{1}{L \cdot C}} \cdot \frac{G}{1 - s/p} = 1 \tag{4.4}$$

which corresponds to the following equations:

$$\begin{cases} \frac{1}{L\cdot C} - \omega^2 \cdot \left(1 + \frac{1}{C\cdot R_p \cdot p}\right) = 0 \\ \left(\frac{1}{R_p} - G\right) \cdot \frac{1}{C} + \frac{1}{p\cdot L\cdot C} - \frac{\omega^2}{p\cdot L\cdot C} = 0 \end{cases} \tag{4.5}$$

In terms of $\omega_n = 1/\sqrt{LC}$ and Q (2.64) this results in:

$$\begin{cases} \omega = \dfrac{\omega_n}{\sqrt{1 + \frac{\omega_n}{p\cdot Q}}} \\ \mathrm{G} = C \cdot \dfrac{\omega_n}{Q} \cdot \left[1 + \dfrac{Q \cdot \omega_n^2}{p^2 \cdot Q + p \cdot \omega_n}\right] \end{cases} \tag{4.6}$$

When the pole frequency p is high compared to ω_n, the pole can be neglected and the same results are obtained as in the case of an ideal amplifier. However, when the pole frequency decreases, the phase shift in the amplifier causes the oscillation frequency to drop. This drop also depends on Q: the higher the Q, the lower this frequency drop (2.69). The impact on the required DC gain to obtain a stable oscillation is significant: (1) it has to compensate for the gain drop due to the pole in the amplifier, and (2) it needs to compensate for the fact the oscillation frequency is no longer at the resonant peak in the feedback network's transfer function. For a pole frequency around ω_n, a factor of $\sqrt{2}$ is expected due to the pole in the amplifier. Nevertheless, an extra factor of $\sqrt{2}$ must be added due to the decreased gain in the feedback network. So the final shift is a factor 2.

4.2.2 Nonlinear Oscillator Systems

Up till now the amplifier was assumed to have a linear transfer characteristic. In practice, this situation does not exist. To calculate the influence of its nonlinearity, it is most interesting to use the concept of the negative resistor (4.2). The corresponding differential equation is given by:

$$\frac{d^2v(t)}{dt^2} + \frac{1}{C} \cdot \left(\frac{1}{R_P} - G(v)\right) \cdot \frac{dv(t)}{dt} + \frac{v(t)}{L \cdot C} = 0 \tag{4.7}$$

In this equation, $G(v)$ denotes the fact that the amplifier gain depends on the voltage over the tank. $G(v)$ can be written as:

$$G(v) = a_0 + a_1 \cdot v + a_2 \cdot v^2 + a_3 \cdot v^3 + \cdots \tag{4.8}$$

which completes the oscillation equation. Although this equation exactly describes the behavior of the oscillator, obtaining a closed-form expression for $v(t)$ is often impossible. Another strategy needs to be followed.

In most practical cases, and certainly in differential circuits, it can be assumed that the gain G is maximum for a zero input and decreases towards the edges of the input range. For a differential amplifier:

$$G(v) = G(-v) \tag{4.9}$$

which denotes the symmetry in the amplifier. The nonlinear amplifier characteristic causes the presence of harmonics in the system. When these harmonics are injected in the tank, this causes an imbalance between the work done in the capacitor and the inductor [174]. Or, in other words, due to the higher frequencies in the circuit, the reactive power component is no longer the same in the capacitor and the inductor. An excess amount of reactive power is generated in the tank. This effect is called Harmonic Work Imbalance or HWI. Since reactive power cannot be provided or absorbed by the amplifier, this imbalance must be compensated for by a frequency shift. The first to calculate the exact influence of these harmonics was Janusz Groszkowski, using the energy equations [98].

4.2.2.1 The Work Delivered by an Amplifier

In stable operation, the amplifier supplies the *real* part of the energy, needed to compensate the losses. At the same moment, reactive power or *imaginary* energy is exchanged between the tank components. Since the negative resistance can only deliver or absorb *real* energy, it must be a curve for which the current i is the univocal function of the voltage v, i.e. the amplifier has no hysteresis, state or memory. As a result, the area described by the instantaneous point of work in the (i, v) coordinate system must be zero over a complete period (the $i - v$ characteristic does not contain any loops):

$$\oint idv = 0 \tag{4.10}$$

Since the amplifier is directly connected to the oscillator tank, this equation gives the relation between the instantaneous current and voltage in the circuit. Since the output of the oscillator is a periodic signal, the current and the voltage are of the following form (see Sect. A.1.2):

$$v = \sum_{k=1}^{\infty} V_k \cdot \sin(k \cdot \omega_0 \cdot t + \alpha_k) \tag{4.11}$$

$$i = \sum_{k=1}^{\infty} I_k \cdot \sin(k \cdot \omega_0 \cdot t + \beta_k) \tag{4.12}$$

where V_k and I_k are the Fourier coefficients and α_k and β_k are the phase shifts corresponding to the k-th harmonic of the waveform. ω_0 is the fundamental

angular frequency of the nonlinear oscillator. Furthermore, there must be a relationship between V_k and I_k given by Z_k, which is the tank impedance for the k-th harmonic frequency:

$$I_k = \frac{V_k}{Z_k} \tag{4.13}$$

This relationship, together with (4.10), allows to calculate the oscillator's frequency variation as a function of the harmonic distortion in the amplifier. Using (4.11) it is known that:

$$dv = \sum_{k=1}^{\infty} k \cdot \omega_0 \cdot V_k \cdot \cos(k \cdot \omega_0 \cdot t + \alpha_k) dt \tag{4.14}$$

which makes (4.10):

$$\oint idv = \int \left[\sum_{k=1}^{\infty} I_k \cdot \sin(k \cdot \omega_0 \cdot t + \beta_k) \right] \left[\sum_{k=1}^{\infty} k \cdot \omega_0 \cdot V_k \cdot \cos(k \cdot \omega_0 \cdot t + \alpha_k) \right] dt \tag{4.15}$$

Calculating this integral over a complete period results in:

$$\begin{aligned} \oint idv = & \sum_{k=1}^{\infty} k \cdot \omega_0 \cdot V_k \cdot I_k \int_0^{2\pi/\omega_0} \sin(k \cdot \omega_0 \cdot t + \beta_k) \cos(k \cdot \omega_0 \cdot t + \alpha_k) dt \\ & + \sum_{\substack{m,n=1 \\ m \neq n}}^{\infty} m \cdot \omega_0 \cdot V_n \cdot I_m \int_0^{2\pi/\omega_0} \sin(m \cdot \omega_0 \cdot t + \beta_m) \cos(n \cdot \omega_0 \cdot t + \alpha_n) dt \end{aligned} \tag{4.16}$$

which can drastically be simplified using:

$$\begin{aligned} & \int_0^{2\pi/\omega_0} \sin(k \cdot \omega_0 \cdot t + \beta_k) \cos(k \cdot \omega_0 \cdot t + \alpha_k) dt \\ & = \cos(\alpha_k) \cdot \sin(\beta_k) \cdot \int_0^{2\pi/\omega_0} \cos^2(k \cdot \omega_0 \cdot t) dt \\ & - \sin(\alpha_k) \cdot \cos(\beta_k) \cdot \int_0^{2\pi/\omega_0} \sin^2(k \cdot \omega_0 \cdot t) dt \\ & + (\cos(\alpha_k) \cdot \cos(\beta_k) - \sin(\alpha_k) \cdot \sin(\beta_k)) \end{aligned} \tag{4.17}$$

$$\cdot \int_0^{2\pi/\omega_0} \sin(k \cdot \omega_0 \cdot t) \cos(k \cdot \omega_0 \cdot t) dt \tag{4.18}$$

$$= \frac{\pi}{\omega_0} \cdot (\cos(\alpha_k) \cdot \sin(\beta_k) - \sin(\alpha_k) \cdot \cos(\beta_k)) \tag{4.19}$$

$$= \frac{\pi}{\omega_0} \cdot \sin(\beta_k - \alpha_k) \tag{4.20}$$

$$\text{and} \int_0^{2\pi/\omega_0} \sin(m \cdot \omega_0 \cdot t + \beta_m) \cos(n \cdot \omega_0 \cdot t + \alpha_n) dt = 0. \tag{4.21}$$

This results in the following equation:

$$\oint idv = \sum_{k=1}^{\infty} \pi \cdot k \cdot V_k \cdot I_k \cdot \sin(\beta_k - \alpha_k) = 0. \tag{4.22}$$

As can be expected, the terms of this equation are equal to the imaginary part of the power delivered by the k-th harmonic:

$$P_R = \frac{1}{2} \cdot V_k \cdot I_k \cdot \sin(\beta_k - \alpha_k), \tag{4.23}$$

which means that (4.10) can be written as:

$$\oint idv = \sum_{k=1}^{\infty} V_k^2 \cdot \Im \left[\frac{k}{Z_k} \right] = 0 \tag{4.24}$$

where $\Im(x)$ denotes the imaginary part of x. The fundamental frequency can be eliminated, and the amplitude of other components can be written proportionally to the fundamental amplitude, according to:

$$\gamma_k = \frac{V_k}{V_1}. \tag{4.25}$$

Then (4.24) can be written as:

$$\Im \left[\frac{1}{Z_1} \right] + \sum_{k=2}^{\infty} \Im \left[\frac{k}{Z_k} \right] \cdot \gamma_k^2 = 0 \tag{4.26}$$

A similar equation can be derived for the currents [98]:

$$\Im\left[Z_1\right] + \sum_{k=2}^{\infty} \Im\left[k \cdot Z_k\right] \cdot \delta_k^2 = 0 \tag{4.27}$$

where:

$$\delta_k = \frac{I_k}{I_1}. \tag{4.28}$$

4.2.2.2 Application to a Known Network

This result can be applied to a known network, such as the parallel RLC network in Fig. 2.9a, repeated here in Fig. 4.2. The impedance of this network is given by (2.66). It follows that:

$$\frac{1}{H(s)} = s \cdot C + \frac{\omega_n}{Q} \cdot C + \frac{\omega_n^2}{s} \cdot C \tag{4.29}$$

$$\Im\left[\frac{k}{H(j \cdot k \cdot \omega_0)}\right] = \Im\left[\frac{1}{Z_k}\right] = k \cdot \omega_0 \cdot C - \frac{\omega_n^2}{\omega_0} \cdot C \tag{4.30}$$

$$= \frac{1}{\omega_0 \cdot L} \cdot \left(\frac{k^2 \cdot \omega_0^2}{\omega_n^2} - 1\right) \tag{4.31}$$

Since $\omega_0 \approx \omega_n$, this formula can be approximated for $k \neq 1$ by:

$$\mathrm{Im}\left[\frac{1}{Z_k}\right] \approx \frac{1}{\omega_0 \cdot L} \cdot (k^2 - 1) \tag{4.32}$$

which makes (4.26):

$$\left(\frac{\omega_0}{\omega_n}\right)^2 - 1 \approx -\sum_{k=2}^{\infty} (k^2 - 1) \cdot \gamma_k^2 \tag{4.33}$$

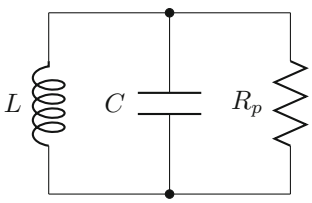

Fig. 4.2 A parallel RLC network, as shown previously in Fig. 2.9a

The left-hand side of this equation is approximated by its first-order Taylor expansion:

$$2 \cdot \frac{\Delta\omega_0}{\omega_n} \approx -\sum_{k=2}^{\infty}(k^2-1)\cdot\gamma_k^2 \tag{4.34}$$

$$\Leftrightarrow \frac{\Delta\omega_0}{\omega_n} \approx -\frac{1}{2}\cdot\sum_{k=2}^{\infty}(k^2-1)\cdot\gamma_k^2 \tag{4.35}$$

$$= -\frac{1}{2}\cdot(3\cdot\gamma_2^2 + 8\cdot\gamma_3^2 + 15\cdot\gamma_4^2 + \cdots) \tag{4.36}$$

where $\Delta\omega_0 = \omega_0 - \omega_n$. This is the same result as in [7, 98]. A similar calculation can be done using the Fourier series of the resulting current applied by the nonlinear amplifier (instead of the output voltage). Equation (4.27) then results in:

$$\frac{\Delta\omega_0}{\omega_n} = -\frac{1}{2\cdot Q^2}\cdot\sum_{k=2}^{\infty}\frac{k^2}{k^2-1}\cdot\delta_k^2 \tag{4.37}$$

as shown in Appendix B.1. The higher the amount of harmonics in the output waveform, the higher the frequency deviation from the expected fundamental frequency.

In some cases it is possible to make a theoretical estimation of the harmonic content in the output signal. For an amplitude-limiting amplifier with a symmetric (differential) transfer characteristic $i(v) = A_1\cdot v + A_3\cdot v^3$, an example is demonstrated in Appendix B.2. It is shown that the influence of the harmonics becomes significant for tanks with a low Q factor and a high amount of excess gain.

4.2.2.3 Maximum Frequency Offset due to HWI

The calculation of the resulting waveform is often not possible and mostly requires a huge effort. Therefore, using (4.37), an upper limit for the output frequency shift is determined [174]. This is when a comparator is used instead of a (slightly nonlinear) amplifier, resulting in a square-wave current at the amplifier's output. The square wave is defined as follows:

$$i(t) = \begin{cases} 1 & \text{for } \frac{2\cdot z}{2}\cdot T \le t < \frac{2\cdot z+1}{2}\cdot T \\ -1 & \text{for } \frac{2\cdot z+1}{2}\cdot T \le t < \frac{2\cdot z}{2}\cdot T \end{cases} \text{ and } z \in \mathbb{Z} \tag{4.38}$$

where T is the period of the square-wave function. This means that the current is an odd function of time which can be represented using a sine Fourier series:

$$I_k = \frac{2}{T}\int_0^T i(t)\cdot\sin\left(\frac{2\cdot\pi\cdot k\cdot t}{T}\right)dt = \begin{cases} 0 & \text{for even } k \\ \frac{4}{\pi\cdot k} & \text{for odd } k \end{cases} \tag{4.39}$$

The ratio of the k-th harmonic and the fundamental frequency is then:

$$\delta_k = \frac{1}{k} \tag{4.40}$$

which makes the maximum frequency shift caused by the nonlinearity in the amplifier (4.37) equal to:

$$\frac{\Delta\omega}{\omega_n} = -\frac{1}{2 \cdot Q^2} \cdot \sum_{k \in \{3,5,\dots\}}^{\infty} \frac{1}{k^2 - 1} \tag{4.41}$$

$$= -\frac{1}{8 \cdot Q^2} \tag{4.42}$$

The last step is proven in Appendix B.3. The maximum frequency shift strongly depends on the Q factor of the harmonic tank. For high-quality tanks, the influence of the nonlinearities in the amplifier is strongly reduced. For an amplifier with a constant gain the resulting frequency shift is not important as long as it is constant. Temperature and supply voltage changes have, however, a huge impact on the gain, and therefore also on the nonlinearity of the amplifier. Eventually, this also affects the oscillation frequency.

4.2.3 Transistor Behavior

In an integrated oscillator, amplifiers are built using transistors. These components compensate for the losses in the tank. As will be seen, tanks themselves can be made highly temperature- and supply voltage-independent. However, the transistors in the circuit also have an influence on the oscillator output frequency. Unfortunately, because of the temperature dependency of the transistor parameters, the short-term as well as long-term frequency stability is often degraded.

4.2.3.1 Impact of the Supply Voltage

A detailed and accurate transistor model is proposed in [40], based on the commonly used Enz-Krummenacher-Vittoz (EKV) model [21]. It can easily be seen from these models that transistors slow down at lower supply voltages. This is mainly caused by the output current, which depends quadratically on the gate-source voltage (V_{gs}) in the saturation region:

$$I_{ds} = \frac{\mu_n \cdot C_{ox}}{2} \cdot \frac{W}{L} \cdot (V_{gs} - V_{th})^2 \cdot \left(1 + \frac{V_{ds}}{V_E \cdot L}\right) \tag{4.43}$$

where μ_n is the electron carrier mobility (μ_p in a PMOS transistor), V_{th} is the threshold voltage, V_E is the early voltage and W and L are the transistor dimensions [219]. In the sub-threshold region these dependencies even become exponential:

$$I_{ds,wi} = I_{D0} \cdot \frac{W}{L} \cdot e^{\frac{V_{gs}-V_{th}}{n \cdot k \cdot T/q}} \tag{4.44}$$

where I_{D0} and n are technology parameters, k is the Boltzmann constant and q is the unit charge of an electron. This also has an impact on the transconductance g_m:

$$g_m = \frac{\partial I_{ds}}{\partial V_{gs}} = \frac{2 \cdot I_{ds}}{V_{gs} - V_{th}} \tag{4.45}$$

in the saturation region and:

$$g_{m,wi} = \frac{\partial I_{ds,wi}}{\partial V_{gs}} = \frac{I_{ds,wi}}{n \cdot k \cdot T/q} \tag{4.46}$$

in weak inversion. As can be seen, the decreasing voltage also has an impact on the output resistance:

$$r_0 = r_{ds} = \frac{V_E \cdot L}{I_{ds}} \tag{4.47}$$

In weak inversion, the output resistance is equal to ∞. The transition between both regimes is best described in [40, 80]. As can be seen, due to the typically lower current and higher impedances at lower biasing voltages, the bandwidth of the circuitry decreases. The delay of an inverter is roughly proportional to [96, 206]:

$$t_d \propto \frac{V_{dd}}{(V_{dd} - V_{th})^{\alpha}} \tag{4.48}$$

where $1 < \alpha < 2$, depending on the technology (saturation current). This shows that a stable DC-biasing of the MOS transistors in the circuit is necessary to keep the time delay values constant.

4.2.3.2 Impact of Temperature

When looking at the temperature dependence of MOS transistors, similar conclusions can be drawn. In [83, 259], the temperature dependence of the different MOS parameters is studied. The different parameters of the current Eq. (4.43) appear to be temperature-dependent. For the carrier mobility this is typically modeled as [143]:

$$\mu_n(T) = \mu_n(T_0) \cdot (T/T_0)^{\alpha_\mu} \tag{4.49}$$

where α_μ is a constant, typically assumed to be -2. Also the threshold voltage V_{th} is temperature-dependent [253]:

$$V_{th}(T) = V_{th}(T_0) + \alpha_{V_{th}} \cdot (T - T_0) \tag{4.50}$$

where $\alpha_{V_{th}} = \delta V_{th}/\delta T$ is assumed to be constant and depends on the technology. As a result, output parameters such as the current, the transconductance and the output resistance will depend on the temperature. In [83] it is shown that, when $\alpha_{\mu_n} = -2$, one specific biasing point exists where the V_{gs}-I_{ds} relationship is temperature-independent, the so-called Zero-Temperature-Coefficient (ZTC) point:

$$I_{ds} = I_{ds,f} = \frac{\mu_n(T_0) \cdot T_0^2 \cdot C_{ox}}{2} \cdot \frac{W}{L} \cdot \alpha_{V_{th}}^2 \tag{4.51}$$

$$V_{gs} = V_{gs,f} = V_{th}(T_0) - \alpha_{V_{th}} \cdot T_0 \tag{4.52}$$

For an ideal transistor, this means that the $V_{gs} - I_{ds}$ curves cross in exactly one point. In a real transistor, however, $\alpha_{\mu_n} \neq -2$ and the curves do not have a common interception point, they have a 'bottleneck' only. It will be shown that using a diode-connected transistor in this DC setting (voltage and current) can be used to obtain a temperature-stable oscillator circuit.

The changing transistor parameters also have an impact on the gain, which, as shown in Sect. 4.2.2, influences the linearity, the waveform and the frequency of the oscillator. As will be seen in the remainder of this work, all these effects need to be examined carefully to fully understand the frequency variations as a result of supply voltage and temperature changes.

4.2.4 Properties of the Feedback Network

When building a fully-integrated clock reference, the quality of the integrated passives is of huge importance. Generally speaking, 3 different components are available: resistors, inductors and capacitors. As previously seen, these components need to be combined to obtain a tuned network. All three components are briefly discussed in terms of their temperature and supply voltage dependency. Since every CMOS process is slightly different, it is, however, necessary to use the specific process data.

4.2.4.1 Resistors in Standard CMOS

In a standard CMOS process, different resistors are available. Resistors can be constructed using doping implants in the mono-crystalline silicon substrate [64] (so-called n+ and p+ resistors) but also by depositing doped polysilicon [146] (n-poly and p-poly resistors). Within these construction methods, often different subcategories such as high-resistive or low-resistive polysilicon are available. In [168] it is shown that the sensitivity of poly resistors to the doping concentration is higher than in the case of an implant resistor and is decreasing with increasing grain size. However, these resistors have many benefits such as the isolation from the substrate and the lower parasitic capacitances. The voltage dependency or linearity is

mainly determined by the junction between the silicon grains. These junctions cause a small nonlinearity in the I-V transfer characteristic. In most cases, however, this is negligible [146]. Furthermore, the temperature dependency of the bulk resistance of n-poly and p-poly is opposite, which can be used to obtain a temperature-independent resistor [31]. These combinations, however, depend on matching properties. For poly resistors, [18, 27] report a relative mismatch (3σ) lower than 1 % for resistor values higher than 20 kΩ and a width of at least 500 nm.

4.2.4.2 Inductors in Standard CMOS

On-chip inductors are constructed using the standard interconnect metal layers. No special layers or doping implants are needed. The temperature behavior of inductors is considered to be stable since the properties mainly depend on the physical dimensions of the inductor. The main problem, however, is the quality of the inductor, which is mainly limited by the small dimensions and the proximity of the silicon substrate [141]. As shown in Fig. 4.3, some capacitive coupling exists between the inductor and the substrate, but also between the inductor windings. Since nowadays most CMOS technologies allow the use of metal tracks under a 45° corner, octagonal inductors are commonly used rather than square and/or circular devices.

Another type of losses are the Eddy currents. When an alternating current flows through the inductor, the resulting magnetic field causes a current in the silicon substrate which flows in the opposite direction [285]. This results in an energy loss in the substrate and a decrease of the inductance because of the decreased resulting magnetic field. This is shown in Fig 4.4a.

Another effect, which is also caused by a variation of the applied current, is the skin effect [284]. Due to the current in the metal tracks, a magnetic field is generated which, on its turn, generates circular current flows in the conducting metal. This circular current, superposed on the forward current, forces the net current to flow at the outside of the metal wire, see Fig. 4.4b. The resistance of the conductor increases and can be calculated using the *skin depth*, which expresses the average thickness of the resulting outer shell of the conductor that is actually used. The value of the skin depth δ_{Xx}, where Xx is the material of the conductor, mainly depends on the frequency ω, the conductivity $\boldsymbol{\rho}$ and the magnetic permeability μ of the conductor and is therefore a material constant. In normal cases, for a conducting metal, the skin depth is approximated by:

$$\delta_{Xx} = \sqrt{\frac{2 \cdot \rho}{\omega \cdot \mu}} \tag{4.53}$$

In materials with a poor conductivity, also the electric permittivity ε, has an influence. For aluminum and gold, which are commonly used materials in chip interconnect fabrication, the skin depth at 1 GHz is:

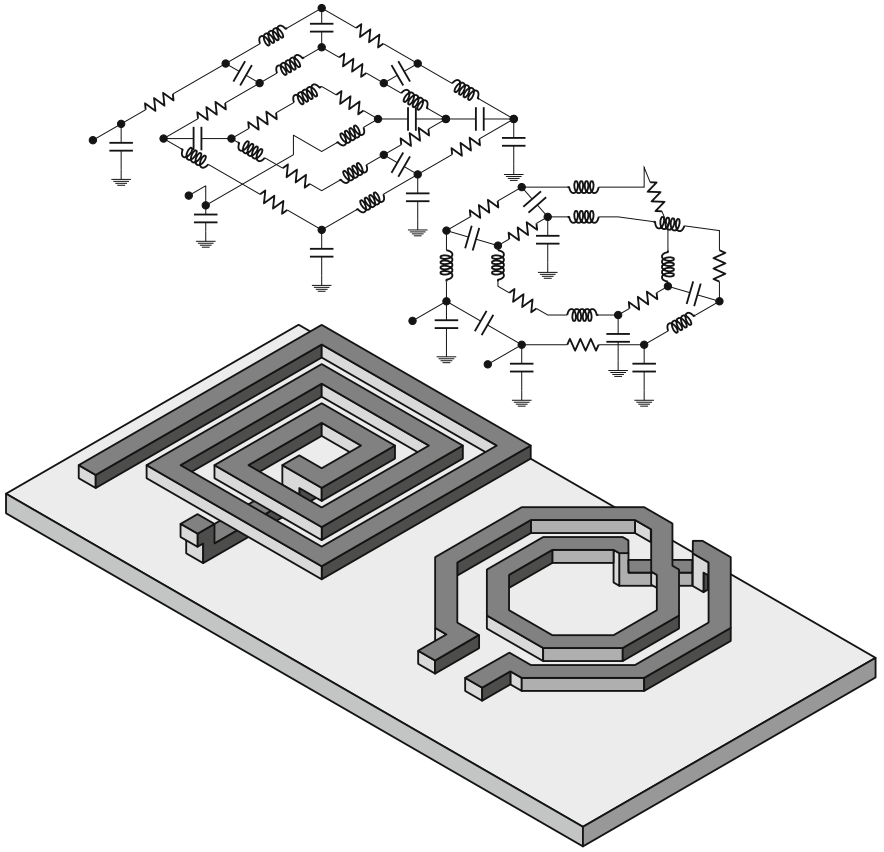

Fig. 4.3 Two typical structures of an integrated inductor. *Above* an electronic model is shown with some of the parasitics. Note that the number of components in the lumped inductor model needed to accurately simulate the behavior, depends on the wavelength of the applied signal. Due to its small dimensions (usually smaller than 1 mm), and the lossy silicon substrate underneath, a lot of capacitive parasitics arise. Furthermore, the series resistance and Eddy currents in the substrate cause significant energy losses

$$\delta_{Al} = 2.53\,\mu\text{m} \tag{4.54}$$

$$\delta_{Au} = 2.50\,\mu\text{m} \tag{4.55}$$

which has a significant impact, even for an integrated inductor. The current density distribution in the conductor is then given by:

$$J(d) = J_s \cdot \mathrm{e}^{-d/\delta_{Xx}} \tag{4.56}$$

where d is the depth from the surface and J_s is the current density at the surface of the conductor. A similar effect also impacts the current distribution in conductors which

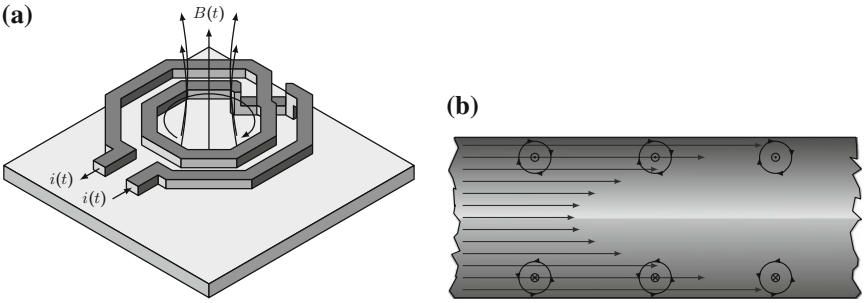

Fig. 4.4 Schematic drawing of the losses in an inductor, both caused by the flow of a changing current in the conductor. **a** Eddy currents are circular currents in the substrate, which cause a power loss and a decrease of the inductance. **b** Skin effect: due to circular currents in the conductor itself, the current is forced to the outer shell of the conductor

are close to each other. Due to this effect, which is called the proximity effect, the effective resistance increases. Generally speaking, a finite element simulator will be needed to calculate the impact of this effect for a given inductor or wire configuration.

A last source of resistive losses is caused by so-called crowding effects: it is observed that the resistance of inductors increases dramatically as a function of the DC current [140]. Although this effect affects the linearity of the integrated inductor, it is considered to be negligible in low-power oscillator applications.

Due to these losses, typically, a Q factor of only 4–8 around frequencies of 1–3 GHz can be obtained for silicon-integrated spiral inductors [138]. Some technologies provide for instance a thick copper layer as top metal layer to reduce the series resistance of the inductor. These process features can increase the Q factor slightly above 10 in standard CMOS technologies or to around 30–40 when non-standard process steps such as micro machining are used [30]. Over the years, different layout techniques have been invented to improve the inductor performance. In [184] patterning of the substrate is used to reduce the circular flow of Eddy currents, and an 11 % increase of the Q factor is reported. In [167] a cavity is etched under the inductor which strongly reduces the Eddy currents and substrate coupling resulting in a Q above 40. Some techniques to create a 3-D horizontally-oriented integrated inductor [4] or an integrated inductor with Cobalt/Nickel core [204] have been patented. Unfortunately no measurements results were reported on these inventions. To avoid the influence of external objects (which can influence the magnetic field and therefore also the inductance), using a Faraday shield around the inductor has been proposed by IDT [176]. Finally, also bondwires can be used to obtain an inductor. In most cases this technique does not require extra production steps but makes the bonding process more tedious. Due to the increased distance between the substrate and the inductor, the capacitive coupling as well as the Eddy currents are reduced drastically. Furthermore, the series resistance of a bondwire is much lower than of on-chip metal tracks. This technique was first reported in [37], but afterwards used in various

implementations [131, 245], also in the field of integrated DC–DC converters [153, 285]. Q factors up to 40 are reported for high inductor values [153], see Chap. 6.

Questions arise, however, about the mechanical stability and the reproducibility of bondwire inductors. Apart from mechanical vibrations, which can result in higher-order colored noise (Chap. 3), also deformations can occur as a result of mechanical shocks or temperature changes. When considering robustness combined with temperature dependency, fully integrated inductors are more suitable. Probably this is the main reason that monolithic LC oscillators were the first to become a commercially available crystal replacement (see Sect. 4.4.1).

4.2.4.3 Capacitors in Standard CMOS

For the temperature dependency and the linearity of integrated capacitors similar conclusions can be drawn. Typically, different capacitor topologies are available in CMOS technologies. First of all, there are the MOS capacitors which consist of the gate capacitance of a MOS transistor [179]. It is clear that the linearity as well as the temperature dependency in this case is determined by the semiconductor properties. Since the V_{th} of the transistors depends on temperature, also the construction of for instance the depletion layer does, which has an influence on the temperature-capacitance as well as the voltage-capacitance characteristic. The series resistance of these capacitors is rather high compared to the other capacitor architectures, caused by the channel resistance. Next to MOS capacitors, MoM and MiM capacitors are often available. Their drawback is, however, the reduced density compared to MOS caps. Metal-oxide-Metal (MoM) capacitors consist of the capacitance between different metal tracks and therefore require no extra layers nor processing steps in the CMOS process. Metal-insulator-Metal (MiM) capacitors, on the other hand, do need extra layers: mostly they are placed right above the top metal. These capacitors have a low temperature dependency since they only depend on their physical dimensions. Furthermore, they are highly-linear over a wide voltage span and can be constructed having a low series resistance. Also the parasitic coupling to the substrate can in most cases be neglected, depending on the used metal layers for MoM capacitors. The intra-die matching of the MiM capacitors is, due to their relatively large dimensions, expected to be around 0.05 % in a 130 nm technology [163].

4.2.5 How to Obtain a Stable Oscillator?

A possible strategy to obtain a stable oscillator is to limit the influence of the temperature-dependent transistor parameters and mainly rely on the properties of the passives. One way to achieve this is using only high-quality tanks. When doing so, as a result of the low losses, the role of the active circuitry is extremely limited. A different way to understand this, is the fact that the Q factor is related to the bandwidth of the resonant peak in the transfer function. The suppression of external influences

pulling the oscillation frequency away from this natural frequency is therefore higher and a high frequency stability is assured. Furthermore, a high Q factor diminishes the effect of the Harmonic Work Imbalance as a result of nonlinearities. This technique will be demonstrated in Chap. 6.

It is, however, not always possible to use a high-Q resonator. In Chap. 5 it will be shown that, by using the right circuit design, amplifiers can be made independent of the transistor parameters themselves. This technique is mainly applicable in low-frequency applications and when sufficient supply headroom is available. For low-voltage oscillator design, a different approach is needed.

A third technique to obtain long-term frequency stability is by keeping the transistor parameters themselves constant. Different methods to do so will be discussed throughout the remainder of this work. Supply voltage instabilities can be rejected by making use of voltage and current regulators (Chap. 5). A technique based on the ZTC point will briefly be discussed in Sect. 4.4.2.

The proposed techniques all rely on the fact that the frequency-determining components themselves need to be (kept) PVT-stable. It is, however, also possible to use compensation mechanisms.

4.2.5.1 First-Level Versus Second-Level Techniques

At design time, two questions need to be answered: '*How stable are these frequency-determining components?*' and '*What is the influence of the parasitic effects?*'. The answers to both questions are closely connected to the final long-term stability result. The design techniques to achieve this result can be subdivided in two categories:

- **First-level techniques** are the techniques used to improve the stability of the components themselves and the techniques to diminish the influence of the parasitic components. These techniques are therefore mainly responsible for the answer to both questions.
- **Second-level techniques**, also called compensation techniques, are techniques to overcome the remaining instability by using an extra circuit or mechanism to compensate for any residual component variations or parasitic influences.

Although it is possible to achieve a high accuracy by mainly relying on second-level techniques, for instance compensating a changing resistor value by adapting a biasing current, the use of first improving the stability of the parasitics and components itself before using any compensation techniques is often a more successful strategy. Second-order techniques often suffer much more from mismatch and process variations and can therefore easily degrade the oscillator performance.

4.3 Figures of Merit for Long-term Stability

Because of the lack of a closed relationship between the power consumption and the temperature or supply voltage dependency, it is difficult to put these parameters into the same FoM. The temperature and supply voltage dependency are therefore mostly expressed in terms of ppm/°C or ppm/V, respectively.

4.3.1 Temperature FoM

In [176], an attempt has been made to define a FoM relating the rms phase jitter, the power consumption and the frequency accuracy. The idea is that, especially in sub-μm CMOS technologies, temperature accuracy is achieved by using active (second-level) compensation mechanisms, which lead to an increased power consumption. The jitter σ used in the proposed formula is calculated as the integrated jitter over a 12 kHz to 20 MHz band, which is said to be approximately independent of the oscillator's frequency [176]. This results in the following definition:

$$FoM_{JT} = 10 \cdot \log\left(\frac{\Delta f_T}{f_0} \cdot 10^6 \cdot \sigma_j \cdot P/6\right) \tag{4.57}$$

where $\Delta f_T/f_0$ is the relative frequency variation as a result of temperature changes, the jitter σ_j is expressed in ps and the power P is expressed in mW. Note that the division by 6 is omitted while calculating the FoM in the remainder of [176]. Furthermore, it is not clear how the temperature stability is defined. This can be over a certain temperature span, but can also be the deviation over 1 °C. It is concluded, based on this FoM, that crystal oscillators are performing the best, followed by MEMS devices and CMOS implementations. Unfortunately, the implementations compared are not referenced properly, which makes a further comparison impossible.

A possible improvement, compared to (4.57), is the use of the phase noise spectrum instead of the jitter. The relative phase noise density is equal to:

$$\mathscr{L}_r = \mathscr{L}\{\Delta\omega\} \cdot \left(\frac{\Delta\omega}{\omega_0}\right)^2 \tag{4.58}$$

where $\Delta\omega$ is an offset frequency in the $1/f^2$ region. This formula therefore takes the $1/f^2$ slope of the phase noise into account. Similar to the phase noise FoM, this figure needs to be compared to the power consumption of the implementation. The combined temperature-phase noise FoM then results in:

$$FoM_{PNT} = 10 \cdot \log\left[\mathscr{L}_r \cdot P^2 \cdot \frac{\Delta f_T}{f_0} \cdot 10^6\right] \tag{4.59}$$

$$= FoM_{PN} + 10 \cdot \log\left[P \cdot \frac{\Delta f_T}{f_0} \cdot 10^6\right] \tag{4.60}$$

$$= FoM_{PN} + FoM_T \tag{4.61}$$

To our believe, any FoM lacking a closed relationship between the included output parameters can be considered to be useless. Therefore, when talking about temperature stability, the output parameters can better be presented separately to be interpreted or compared by an experienced reader.

4.3.2 Supply Voltage FoM

Since this work also focuses on supply voltage-independent implementations, an extra dimension needs to be added in the comparison. Also here, it is important to make a fair comparison between implementations working at different supply voltages. To do so, the relative supply voltage span is defined:

$$\Delta V_{rel} = \frac{2 \cdot (V_{\max} - V_{\min})}{V_{\max} + V_{\min}} \cdot 100\,\% \tag{4.62}$$

The relative frequency deviation, expressed in ppm, divided by the relative supply voltage span ΔV_{rel} can then be used as a measure, independent of the supply voltage of the used technology:

$$\Delta f_{V,r} = \frac{\Delta f_V / f_0 \cdot 10^6}{\Delta V_{rel}} \tag{4.63}$$

where $\Delta f_V / f_0$ is the relative frequency deviation under a changing supply voltage. The unit of this figure is ppm/%. This value can also be expressed in dB:

$$FoM_V = 10 \cdot \log\left(\frac{\Delta f_V / f_0 \cdot 10^6}{\Delta V_{rel}}\right) \tag{4.64}$$

If desired, this number can be combined with the previously presented figures:

$$FoM_{PNTV} = 10 \cdot \log\left[\mathscr{L}_r \cdot P^2 \cdot \Delta f_{V,r} \cdot \frac{\Delta f_T}{f_0} \cdot 10^6\right] \tag{4.65}$$

$$= 10 \cdot \log\left[\mathscr{L}\{\Delta\omega\} \cdot \left(\frac{\Delta\omega}{\omega_0}\right)^2 \cdot P^2 \cdot \frac{\Delta f_V / f_0 \cdot 10^6}{\Delta V_{rel}} \cdot \frac{\Delta f_T}{f_0} \cdot 10^6\right] \tag{4.66}$$

$$= FoM_{PN} + FoM_T + FoM_V \tag{4.67}$$

or, when the phase noise is not included in the comparison:

$$FoM_{TV} = 10 \cdot \log\left[P \cdot \frac{\Delta f_V / f_0 \cdot 10^6}{\Delta V_{rel}} \cdot \frac{\Delta f_T}{f_0} \cdot 10^6\right] \tag{4.68}$$

$$= FoM_T + FoM_V \tag{4.69}$$

Apart from the fact that very little oscillators found in literature mention all the needed dependencies, a combined FoM results in an extremely non-transparent comparison. Furthermore, not every application, not even in WSNs, needs oscillators optimized towards all three parameters. In the remainder of the text and especially in the conclusion chapter, the measured output parameters will be used, sometimes accompanied by a FoM or a plot. In this way, the FoMs themselves can be evaluated and the reader is able to clearly understand the different trade-offs in the oscillator design space.

4.4 Oscillators for Low-Power Applications

The measurement of time exists since the ancient ages. Furthermore, time references are used for all communication purposes and in every clocked circuit. As a consequence, up till today, oscillators are a hot research topic, about which a lot of literature is available. In this section, a short overview is presented of existing implementations. The focus is on fully-integrated oscillators in standard CMOS technology, since these are most relevant in the context of this work. The previously discussed principles and parameters are applied to these existing implementations in order to understand the strengths and drawbacks of the implementations.

Depending on the application in which a time reference is used, different requirements in terms of noise and frequency stability over temperature and supply voltage (PVT) variations exist. This is shown in Fig. 4.5. For instance, in digital microcontroller systems, an accuracy of around 1 % is in many cases sufficient [317]. Some datasheets even report accuracies lower than ±10 % [194]. When it comes to communication, however, a higher accuracy is required. For low-speed USB 1.0, an accuracy of ±15,000 ppm or 1.5 % was required. When the speed increases, also the required clock accuracy increases: ±2,500 ppm for Full-Speed USB 1.0, ±500 ppm for High-Speed USB 2.0 and ±300 ppm for Super-Speed USB 3.0 [33, 258]. Serial-ATA and 10/100/1,000 Ethernet require a frequency accuracy of ±350 ppm and ±100 ppm respectively [174, 193]. When the data rate increases further, even higher accuracies will be required in wired applications.

In wireless applications the frequency specifications are even more tight. This has mainly to do with the fact that the signal strength is much lower and that a lot of unwanted interferers are present. An accurate timing of for instance the carrier frequency is of great importance in the case of smallband signals. In (pulsed) Ultra-Wideband (UWB) applications, this high accuracy is needed for the symbol clock [271]. A wireless LAN (802.11a) and Bluetooth transceiver for instance need a clock accuracy of ±20 ppm, which results in a maximum frequency difference of ±40 ppm between two nodes [14, 229]. For Zigbee, which works at a lower data rate, this is

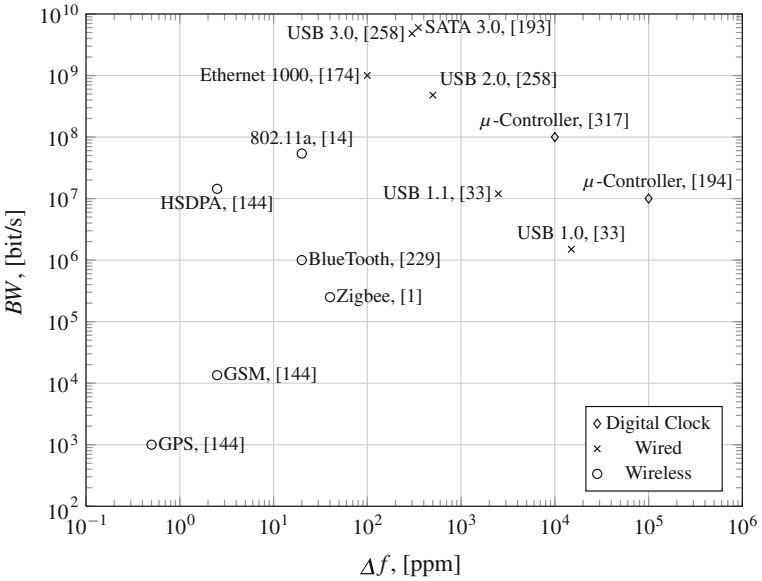

Fig. 4.5 Comparison between different communication technologies: the bandwidth BW is plotted versus the maximum frequency error

±40 ppm at each side [1]. When the distance between the transmitter and the receiver increases, the specifications further tighten to ±2.5 ppm for a mobile handset and ±0.5 ppm for GPS applications [144].

Up till now, the only way to achieve these high accuracies in an economical way, is by using a quartz crystal. These crystals combine an ultra-low-temperature dependency with a high Q factor, which makes them suitable for low-power and low-noise applications. Furthermore, they can be produced at a low cost and, although it is impossible to integrate them in a CMOS process, further miniaturization is going on [127, 144]. This is the main reason that the frequency control market, with a total yearly value of 4.5 billion dollars, is for 90 % dominated by quartz crystal oscillators. A graphical representation of the performance of crystal oscillators is given by the red line in Fig. 4.6 [176]. While a non-compensated or voltage-compensated crystal oscillator (XO or VCXO) can achieve an accuracy of 20–100 ppm, a temperature-compensated oscillator (TCXO) delivers accuracies below 1 ppm and an oven-compensated crystal oscillator (OCXO) can even achieve 1 ppb!

Since these oscillators rely on the piezo-electric effect in a crystal, which corresponds to a mechanical resonance, the miniaturization is limited [144]. Furthermore, this electro-mechanical interaction makes them sensitive to mechanical vibrations, which can cause frequency shifts or higher-order phase noise, as seen in Chap. 3.

Because of the increasing integration and miniaturization of CMOS circuitry, an increasing demand for integrated frequency references is observed. Furthermore, this facilitates the possibility for complete on-chip devices without the need for

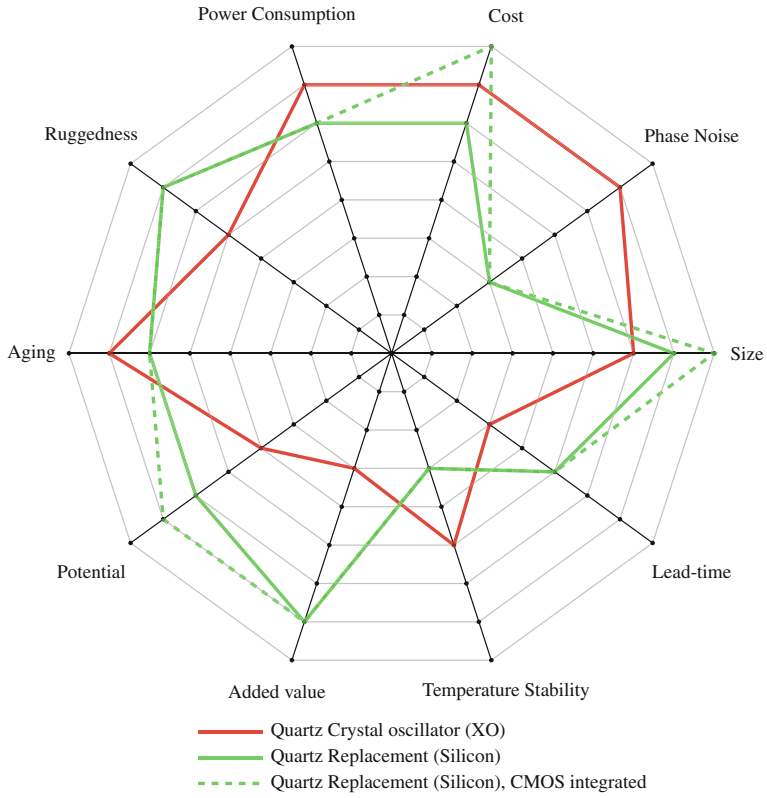

Fig. 4.6 Qualitative comparison of different properties of (uncompensated) crystal oscillators and silicon replacement circuits [176]. The *dashed green line* shows that a huge benefit of cost and size can be achieved when the oscillator can be integrated together with all other CMOS circuitry

any external components, which results in a considerable cost reduction (see the dashed line in Fig. 4.6). In the 1960s the first silicon alternatives of a crystal have been proposed using MEMS. These devices, for which the production steps are unfortunately not standard available in most commercial CMOS processes, also rely on electro-mechanical interaction. Hence, they do not overcome the problem of external vibrations and only result in a small cost reduction due to the need for non-CMOS technologies. The remainder of this section will only focus on frequency references which are fully compatible with standard CMOS technology. MEMS and crystal oscillators are not further discussed. As will be seen, apart from solutions based on a MEMS structure, state of the art LC oscillators are found to be competitive with crystal oscillators in terms of supply voltage and temperature stability.

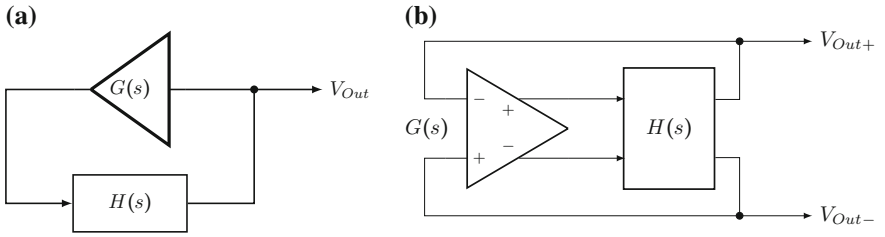

Fig. 4.7 Block schematic of a generic harmonic oscillator. **a** A single-ended amplifier and a feedback network. **b** Its differential equivalent. The amplifier compensates for the losses in the feedback network

4.4.1 Harmonic Integrated Oscillators

The category of harmonic oscillators can contain time references based on two different energy reservoirs as well as combinations of (at least 2) energy reservoirs and a resistor (see Sect. 2.3). Since a harmonic oscillator uses linear components, it can easily be described using transfer functions, the Q factor and the Barkhausen criterion. A block schematic of a typical harmonic oscillator is shown in Fig. 4.7: it consists of a tuned feedback network and an amplifier which compensates for the losses in the feedback network.

4.4.1.1 LC Oscillators

LC oscillators are based on the combination between two energy reservoirs. Because of the lack of resistors, these tanks mostly have a high Q factor compared to RC implementations. This makes LC oscillators, among other integrated solutions, the most suitable for low-phase-noise applications [38, 48, 102]. In [134] an overview of low-noise oscillators is given, based on the phase noise FoM (3.70). As shown in Sect. 4.2.5, a high-Q resonator also has several benefits in terms of long-term frequency stability due to the limited role of the amplifier. When making use of integrated components only, the size of the inductor as well as the capacitors is limited (Sect. 4.2.4). This typically results in RF-range frequencies (1–10 GHz) and puts a lower limit on the power consumption. When going towards deep submicron technologies, where chip area becomes more expensive, these frequencies will increase even further to stay economically feasible [107, 240, 241]. By making use of varicap diodes instead of fixed capacitors, a VCO is obtained, which can be used in for instance a PLL [48, 133]. As a frequency reference, however, special attention needs to go towards the sensitivity to PVT variations. As seen in Sect. 4.2.4, the influence of the temperature due to the capacitive parasitics in the amplifier is dominant on the temperature dependency of the tank itself [174]. In terms of absolute accuracy, mismatch and process variations still pose a major problem in CMOS technologies.

★ Mobius Microsystems
In 2004 Michael McCorquodale founded a company, Mobius Microsystems, focusing on the use of all-silicon frequency references for USB applications, mobile applications and other computer communication protocols. In a few years this company became world leader in this market: in 2007, the first fully integrated LC oscillator compliant with USB2.0 was published [178]. In the years after, different other time references based on similar technology were published [176, 177]. All of these references obtain, after trimming of the center frequency, an accuracy in the order of several hundreds of ppms. Although the output frequency of the devices is around 10–25 MHz, all references are based on a high-frequent (up to 5 GHz) LC frequency tank. This results in a power consumption of several tens of milliwatt. Thanks to this success, Mobius was acquired by IDT (Integrated Device Technology, Inc.) in 2010 [81]. In August 2012, the technology, which was further developed within IDT, was licensed to another semiconductor company for use in USB 2.0 and/or USB 3.0 applications [81]. The best reported temperature dependencies of these products are $<$50 ppm over a $-$20 to 70 °C temperature span [176]. To obtain these accuracies, they make use of an active as well as a passive temperature compensation scheme, previously demonstrated in [175, 177] respectively. Although the current consumption was reduced with a factor of 7 with the introduction of the passive compensation scheme, both schemes separately result in a temperature dependency of around 300 ppm over a 0–70 °C temperature span. Because of the numerous parameters influencing the oscillation frequency, a two-point calibration is necessary to obtain the reported temperature dependency.

Because of the high frequency, the need for a non-inverting amplifier and the low-noise requirements, an LC oscillator is typically built in a differential topology. The oscillator then uses a differential common-source amplifier [212], see Fig. 4.8. The circuit can be analyzed in two ways, as a fully differential amplifier and a differential network (Fig. 4.7b) or as a loop of 2 amplifiers in series with 2 times the equivalent feedback network. Obviously, both methods lead to exactly the same conclusions. Unfortunately, the tank cannot be made without resistive losses.

Assume that the series resistance of the capacitor and inductor are respectively R_C and R_L, then the angular frequency ω_0 of the oscillator is given by:

$$\omega_0 = \frac{1}{\sqrt{LC}} \cdot \sqrt{\frac{L - C \cdot R_L^2}{L - C \cdot R_C^2}} = \omega_n \cdot \sqrt{\frac{L - C \cdot R_L^2}{L - C \cdot R_C^2}} \tag{4.70}$$

where ω_n corresponds to the angular frequency of a lossless energy tank. In practice, however, the losses in an integrated inductor are much higher compared to the losses of a capacitor. Therefore, this equation in practice simplifies to:

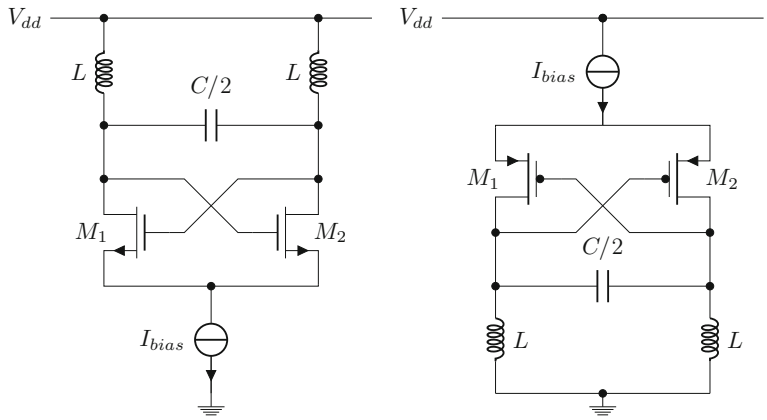

Fig. 4.8 Typical differential implementation of an LC oscillator. *On the left*, the amplifier is implemented with NMOS transistors; *on the right* PMOS transistors are used. A combination of both is also possible [212]

$$\omega_0 \approx \omega_n \cdot \sqrt{1 - \frac{C}{L} \cdot R_L^2} = \omega_n \cdot \sqrt{1 - \frac{1}{Q^2}} \tag{4.71}$$

In an oscillator which makes only use of a linear amplifier, this will be the oscillation frequency. It can be seen that the oscillation frequency drops to zero from the moment Q reaches 1. From this point, it is no longer possible to obtain a stable oscillator from the LC tank. When looking at the transfer function of the feedback network, it can be understood that the Barkhausen criterion can no longer be fulfilled by just using a frequency-independent amplifier. In practical implementations, where a nonlinear amplitude control is always present, the oscillation frequency is also influenced by the resulting distortion of the amplifier or the amplitude regulation, as discussed in Sect. 4.2.2. In the worst case, the impact on the frequency is given by (4.42). For high Q factors and softly distorted amplifiers, however, this effect is assumed to be negligible.

In terms of PVT stability, the state of the art can be found in the products of Mobius Microsystems (see grey inset). In their commercially available designs, active as well as passive compensation techniques in combination with a calibration step are used to obtain this frequency stability. However, recently also another technique has been invented, based on the so-called LC T-null concept [3, 109, 234]. When drawing the transfer function of an LC tank for different temperatures, the resonance frequency (phase shift equal to zero) slightly drifts as a result of temperature drift on the passives. This drift, with an estimated value of 4,000 ppm over a 70 °C temperature span, is mainly caused by changing losses in the inductor [3]. It was observed that one frequency exists at which the phase shift of the feedback network is constant over temperature. This frequency is called the T-null frequency. In [3] the oscillator is forced towards this frequency by building a quadrature oscillator and

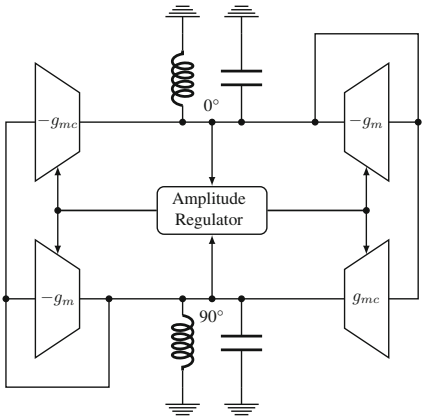

Fig. 4.9 A quadrature oscillator is forced towards its zero temperature frequency by cross-injection of quadrature signals [109]. The amplitude control is used to keep the amplifiers in the linear region. An external trimming circuit is used to trim g_{mc} towards the T-null frequency

adding part of the quadrature signal to the feedback amplifier output. In this way an extra phase shift is generated, which needs to be compensated by a frequency shift in the feedback network. A block diagram of this structure is shown in Fig. 4.9. Two regulation mechanisms are used to obtain the correct injected phase shift. The first is an amplitude regulator which is mainly responsible to limit the harmonic content in the oscillator: all amplifiers need to stay in the linear region. The second mechanism is similar to the Wobble technique proposed in [63]: by modulating the temperature by on-chip resistive heaters and measuring the phase of the corresponding frequency shift, the biasing point can automatically be tuned towards the T-null frequency. This tuning is done once by an external reference circuit after which the resulting feedback gain is stored in an on-chip memory. The resulting frequency accuracy of the 180 nm implementation is ±50 ppm over a 0–70 °C temperature span. The power consumption at an output frequency of 25 MHz and a 3.3 V supply voltage is equal to 23.4 mW.

In [234] a single tank oscillator is built based on the same concept. In this case the tank output signal is fed through a low-pass and a high-pass filter. By feeding back a weighted combination of the outputs of both filters, the desired phase shift is introduced. This results in a ±100 ppm frequency change over a −40 to 85 °C temperature range. The power consumption at an output frequency of 25 MHz at 3.3 V is equal to 23.1 mW.

In literature, however, the focus is more often on the phase noise performance, mostly using the phase noise FoM (3.70). In [134] an elaborate overview of low-noise implementations is found. The best phase noise FoM of an integrated LC oscillator at the time was 187 dB [281]. The 0.35 μm, 12 mW oscillator implementation makes use of a metal inductor in combination with the parasitic gate capacitance of the amplifying transistors, both a cross-coupled NMOS and PMOS pair. The Q factor of

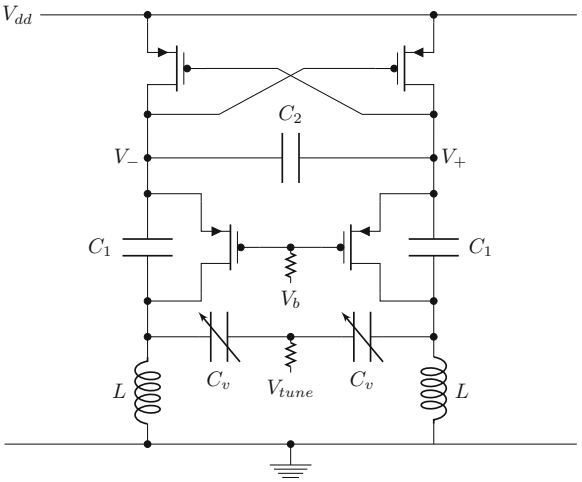

Fig. 4.10 Low-noise differential Colpitts topology presented in [252]. Because of their better noise performance, only PMOS transistors are used

the tank is around 5 and the bulk contact of the PMOS transistors is used to tune the oscillation frequency (9.8 GHz) with a sensitivity of 135 MHz/V over a 2 V tuning range. In [252] two important improvements are made to this differential topology. First of all, a Colpitts topology is used. As stated in [101], these structures owe their improved noise performance to the fact that the energy is injected at the moment when the noise sensitivity is low. The second improvement is the use of only PMOS transistors, which have intrinsically a better noise performance in the $1/f$ as well as the white noise region. The proposed 5 GHz oscillator, shown in Fig. 4.10, is processed in a 0.18 μm technology and consumes 3 mW. This results in a 189.6 dB phase noise FoM.

In [117] the LC tank and cross-coupling of the transistors is done in a different way, as shown in Fig. 4.11. The inductors are laid out as a transformer to improve the magnetic coupling and to increase the Q factor to around 8. This results in a differential 0.18 μm, 2.5 mW oscillator with a phase noise FoM of 190.3 dB. The center frequency is 5.6 GHz with a ±300 MHz tuning range. In [165] the switching technique to reduce the $1/f$ transistor noise described in [283] (see Sect. 3.2.3) is applied to a differential LC oscillator using a cross-coupled NMOS pair and a PMOS biasing. It is also noted that the reduced noise is injected at the moment when the oscillator is the least sensitive to charge injection [101] (see Chap. 3). The resulting 5 GHz oscillator consumes around 5 mW and has a 190.2 dB FoM. By reducing the duty cycle of the biasing transistors, the phase noise can be reduced even further [166]. The presented oscillator has an NMOS cross-coupled pair and NMOS biasing transistors. The reduced duty cycle results in a 191.1 FoM. When using both a PMOS and an NMOS cross-coupled pair, the noise can be reduced by minimizing the overlap between the on-time of both transistors. In [77] this is

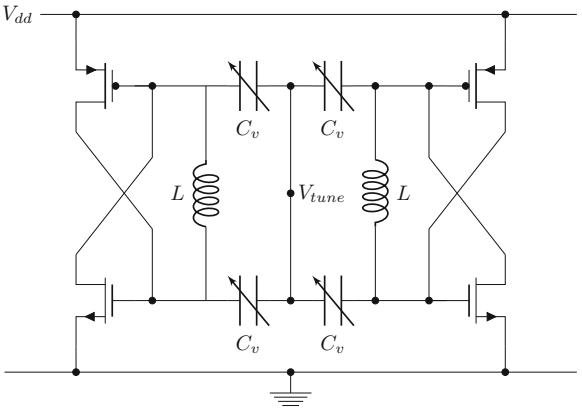

Fig. 4.11 Differential LC topology with an altered cross-coupling of the active devices [117]

achieved by slightly reducing the supply voltage of the 1.8 GHz, 170 μW oscillator, simulated in a 0.18 μm technology. The simulated phase noise FoM is 199 dB but has not been confirmed by measurements.

When the power consumption of the oscillator is an important specification, LC oscillators appear not to be the best choice. However, different techniques are reported to reduce the power consumption of an LC oscillator. In [150] the two differential branches of a differential LC oscillator are put above of each other. In this way, the biasing current flows through both transistors. Evidently, the signal must be capacitively coupled to the gates of the amplifying transistors. The oscillator, which is meant to be injection-locked to an external signal, is tunable from 2.11 to 2.42 GHz and has a power consumption of 0.95 mW. In [148] an oscillator is presented with a sub-threshold amplifier. The 2.63 GHz oscillator works down to a 0.45 V supply voltage and has a 430 μW power consumption. The phase noise FoM at this operating point is 184.8 dB. In the same article, also two other FoMs are used to characterize the phase noise compared to $k \cdot T$. Another ultra-low-power 2.4 GHz VCO for an IEEE 802.11b receiver is presented in [119]. This 0.25 μm implementation makes use of both a cross-coupled NMOS and PMOS pair to optimally use the biasing current. The design only consumes 80 μW, at the cost of a phase noise FoM of only 161 dB. To our knowledge, this is the lowest power consumption reported for an LC oscillator using an integrated inductor.

4.4.1.2 RC and RL Harmonic Oscillators

RC and RL oscillators are both based on an energy reservoir in combination with a resistor to obtain a tuned network. In combination with a feedback amplifier, this results in a harmonic oscillator with a sine wave output. The frequency of these oscillators mainly depends on the feedback network. However, because of the reduced

Q factor of the network compared to that of LC tanks, the role of the amplifier and also its non-idealities have more impact (see Sect. 4.2.5). Compared to an LC network, temperature as well as mismatch have a higher impact on the components in the feedback network [146, 179]. This typically results in a 10 % frequency variation. By means of trimming and/or compensation techniques, this variation can be reduced to around 1 %. Despite their lower accuracy, compared to LC oscillators, RC (and RL) implementations are suitable for low-frequency (10^5–10^8 Hz) and low-power applications (1 μW–1 mW). In [116] an oscillator structure is proposed based on a single current conveyor (often used as an ideal transistor). This topology is shown in Fig. 4.12. It is shown that, to obtain an oscillation, C_x must satisfy:

$$C_x = C_2 \cdot (1 + R_2/R_1) + C_1. \tag{4.72}$$

Then the angular frequency of the oscillator is equal to:

$$\omega_0 = \sqrt{\frac{R_x - R_1}{R_1 \cdot R_2 \cdot R_x \cdot C_1 \cdot C_2}} \tag{4.73}$$

which shows the nonlinear but highly-sensitive tuning possibilities of the oscillator. Furthermore, it is shown that the sensitivity to mismatch in the current conveyor is

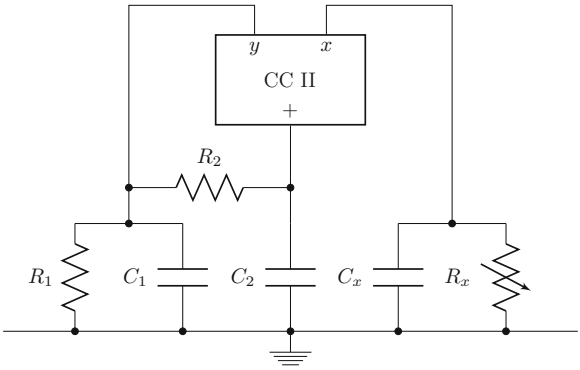

Fig. 4.12 Tunable RC oscillator based on a single current conveyor [116]

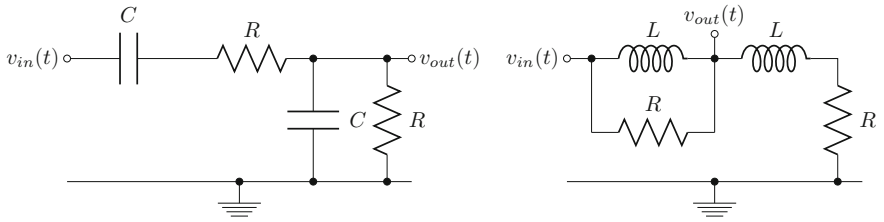

Fig. 4.13 Schematic drawing of a commonly used RC feedback network, called Wien bridge. *On the right* also its dual RL equivalent is shown

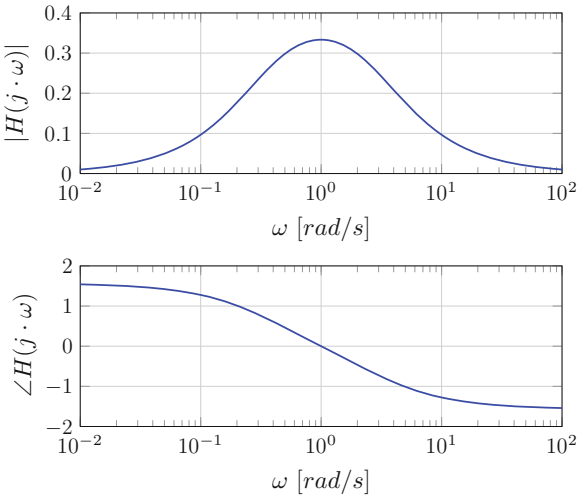

Fig. 4.14 Transfer function of the Wien bridge feedback network

extremely low. In [238] a current-tunable RL oscillator is presented, with a continuous tuning range of 3 orders of magnitude! Such wide tuning ranges can impossibly be achieved using an LC topology. As will be demonstrated, RC or RL networks are typically used in a different configuration than an LC feedback network.

An example is the commonly used Wien bridge RC feedback network, named after its inventor Max Wien [303]. Originally, this network was used in a similar way as a Wheatstone bridge (see Fig. 4.15), to measure complex impedances. In Fig. 4.13, the RC oscillator feedback network and its dual RL network are shown. As can be seen, it is the voltage–voltage transfer function which is used to obtain an oscillator. A plot of this transfer function, for a normalized network, is shown in Fig. 4.14. The RC (RL) network acts as a bandpass filter. A feedback amplifier with a gain of 3 is needed to obtain a stable oscillation.

As will be shown in Chap. 5, one of the main problems with RC feedback networks is the output resistance of the used amplifier. Since an ideal amplifier does not exist, this impedance becomes part of the feedback network and therefore has a significant influence on the frequency. The LR oscillator in [238] is suffering from similar problems. However, due to its huge tuning range, it is likely to use this reference in a feedback topology (such as a PLL). In this configuration, PVT variations can easily be compensated. Another application of a Wien bridge oscillator is to generate chaos. An adapted Wien bridge oscillator to do so is presented in [186]. As seen in Sect. 2.2.1, at least one extra capacitor is needed to obtain a chaotic dynamic system.

4.4.2 Relaxation Integrated Oscillators

Relaxation oscillators can be understood as 'switching' oscillators, as described in Sect. 2.3.3. This typically results in an output waveform with a discontinuous first derivative. Most relaxation oscillators are based on an RC network or a capacitor in combination with a voltage and a current. Similar to harmonic RC oscillators, the frequency range is typically 10^5–10^8 Hz and a low power consumption can be achieved. Drawbacks are the sensitivity to PVT variations. While for a harmonic oscillator the supply dependency can be canceled using a voltage regulator, this is more challenging in a relaxation oscillator, as will be shown in Chap. 5. As long as the frequency is mainly determined by the passives, the sensitivity to process and temperature variations is assumed to be similar to that of harmonic RC oscillators. When the active circuitry (often a comparator in this case) has a dominant impact on the frequency, a comparison can only be made by investigating the specific circuit topologies and implementations.

A typical example of a relaxation oscillator is the multivibrator. Of this circuit, three types are available: bistable, monostable and astable [305]. All three circuits are used commonly in for instance reset circuitry (monostable) [142], as a flip-flop (bistable) or as an oscillator (astable). A schematic of an astable multivibrator is shown in Fig. 4.16. The working principle can best be understood when both transistors are assumed to be 'hard switching' and the base-emitter junction clips at 0.6 V. The supply voltage is equal to 1.2 V. The cross-coupled differential pair functions both as a comparator ($V_{ref} = 0.6\,\text{V}$) and a latch. The different node voltages for $R_1 = R_2 = R_3 = R_4 = R = 1\ \Omega$ and $C_1 = C_2 = C = 1$ F are shown on the right. In this configuration, the oscillation frequency is equal to:

★ Max Wien °1866–†1938
Max Wien was a German physicist and director of the Institute of Physics at the University of Jena [303]. He was a cousin of the Nobel prize winner Wilhelm Wien. He invented the *Löschfunkensender* for the generation of slightly weakened electromagnetic oscillations, which was used on the *rms Titanic* (Fig. 1.7). His most famous invention is the Wien bridge, invented in 1891. Although he is also linked to the Wien bridge oscillator, he never implemented it because no amplifying components were available at that time. It was William Hewlett, co-founder of Hewlett-Packard, who used this network for the first time in a feedback configuration at Stanford University in 1939 [316]. The amplifier gain was controlled by a light bulb of which the impedance increases at high currents (amplitudes).

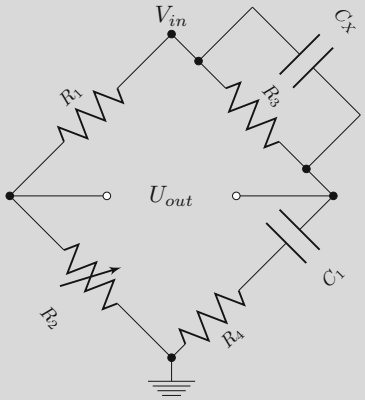

Fig. 4.15 Schematic of the Wien bridge, which was used, similar to the Wheatstone bridge, to measure the value of capacitors in terms of frequency and resistance

By adjusting the angular frequency of the input signal and the value of resistor R_2, the bridge can be balanced (voltage over the bridge equal to zero) and the value of capacitor C_x can be calculated.

$$f = \frac{1}{T} = \frac{1}{2 \cdot R \cdot C \cdot \ln\left[\frac{V_{dd}}{V_{dd}-0.6}\right]} \tag{4.74}$$

As can be seen, the main drawback of this circuit is its high sensitivity to the supply voltage. Note that the circuit, apart from the 2 capacitors, also has a discrete state variable.

Although this topology is commonly used, it lacks accuracy. Furthermore, it suffers greatly from PVT variations. This can be solved by decoupling the latch and the comparator function as shown in [192]. A schematic of such a topology is shown

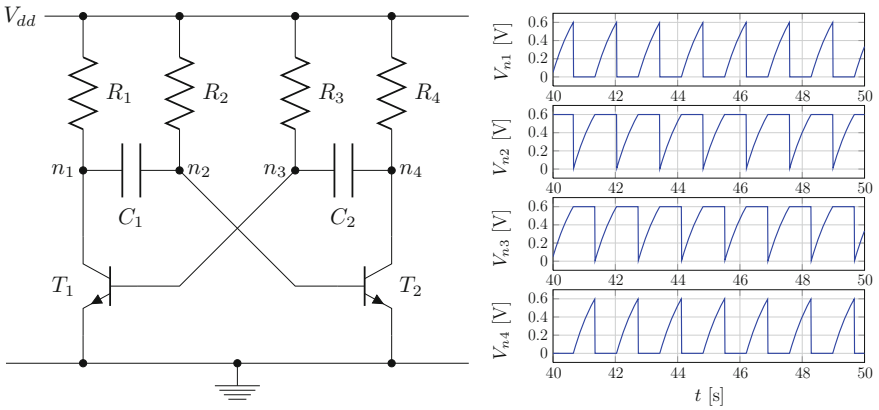

Fig. 4.16 Schematic drawing of an astable multivibrator. *On the right* the output waveforms are shown

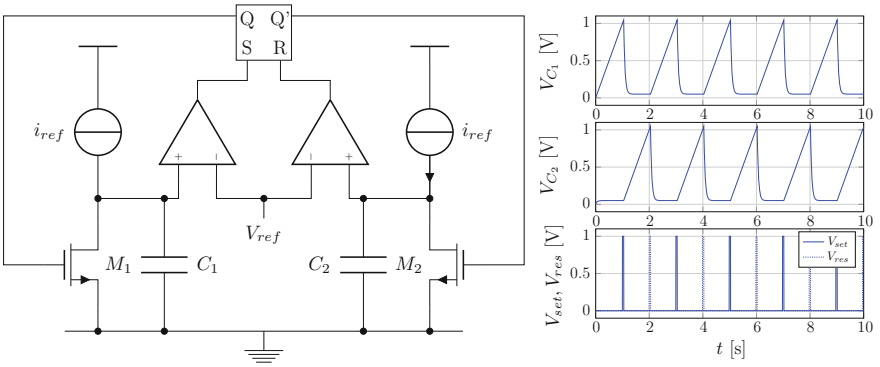

Fig. 4.17 Schematic drawing of a relaxation oscillator based on a multivibrator [192]. *On the right* the output waveforms are shown. The reference voltage is equal to 1 V and the latch has a delay of 50 ms

in Fig. 4.17. Also the output waveforms are shown on the right. For this simulation $C_1 = C_2 = 1$ F, $I_{ref} = 1$ A and $V_{ref} = 1$ V. The amplifier and latch together have a delay $T_d = 50$ ms and the switch resistance is equal to $R_{sw} = 0.05\ \Omega$. As a result, the capacitors are not fully reset. To solve this, an extra switch can be used to disconnect the current source. The oscillation frequency is then equal to:

$$f = \frac{1}{\frac{(C_1+C_2)\cdot(V_{ref}-I_{ref}\cdot R_{sw})}{I_{ref}} + 2 \cdot T_d} \tag{4.75}$$

$$\approx \frac{I_{ref}}{(C_1 + C_2) \cdot V_{ref}} \tag{4.76}$$

As long as the switch resistance is low compared to I_{ref} and T_d is low compared to the charging time, the oscillator frequency is mainly determined by V_{ref}, I_{ref} and $C_1 + C_2$. In [92] a circuit is proposed to bypass the latch. In this way, the impact of the latch on the frequency is reduced. However, the amplifier and some logic gates are still in the critical path. The implementation in [192] uses a bandgap reference to generate both V_{ref} and I_{ref}. In this way a frequency deviation below ± 5 % is obtained over a -40 to 125 °C temperature range and ± 1 % over a 2.5–5.5 V supply voltage range. One-point calibration is used to reduce the ± 25 % process spread on the 12.8 MHz output signal to the reported values. In [275] a similar topology is presented, this time with two possible output frequencies: 11.6 or 21.4 MHz. This results in an accuracy of ± 2.5 % over a -40 to 125 °C temperature range and ± 1.5 % over a 3–5.5 V supply voltage range. Again, one-point calibration is used. The improvement of the temperature offset is by applying a second-level compensation technique in the bandgap reference based on the measured output values of the prototype circuit of [192]. The reported mismatch on the duty cycle (which is a measure for the capacitor mismatch) is below 0.8 %. The technology used is 0.5 μm and the power consumption is 400 μW.

The problem of a non-zero (and temperature-dependent) delay T_d is addressed in different other implementations. In [254] T_d is canceled by generating a reference level $V_{ref} - \Delta V$. In this way, the comparator is activated a little earlier, resulting in an oscillation frequency exactly equal to (4.76). The generation of ΔV happens every cycle and alternates between the two comparators. When the left capacitor is charging, ΔV of the right comparator is generated and vice versa. This results in a 180 nm 6.66 kHz oscillator with a temperature variation of 56 ppm/°C over a -40 to 120 °C temperature range. The frequency varies only 0.98 % over a 0.8–1.8 V supply voltage sweep. A process sensitivity of 0.8 % (σ) was reported. Similarly, in [251] a voltage-averaging feedback loop is implemented to make the oscillation frequency insensitive to the comparator delay. The voltage of the capacitors is fed to the input of a low-pass filter and compared to a reference voltage. This signal is fed back as a reference voltage to the comparators. In this way, similar to the solution in [254], the reference voltage is adapted when the comparator delay increases/decreases as a function of temperature. Another benefit is the reduction of low-frequency noise, which is also compensated for by the (low-frequency) feedback loop. The resulting 180 nm oscillator has an output frequency of 14 MHz, which has a temperature coefficient of only 11.5 ppm/°C over a -40 to 125 °C temperature range. The power consumption is 45 μW.

Another implementation based on the same structure is presented in [29]. The main improvement compared to the previous designs, is the implementation of a chopping circuit. This circuit does not only reduce the offset in the comparators but also drastically reduces the $1/f$ noise. As a result, a low-power (38.4 μW) 3.2 MHz oscillator for biomedical applications is obtained. The resulting accuracy after trimming is ± 0.25 % over a 20–60 °C temperature range. Due to the chopper, the rms jitter is reduced from 524 to 455 ps.

In [92] two important noise sources in this multivibrator-based oscillator are identified: the charging current and the reference voltage. The noise on the charging

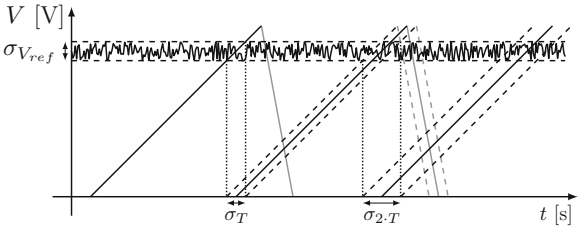

Fig. 4.18 The noise on the reference signal is directly translated to timing jitter on the next charging curve

current is integrated on the capacitors and therefore causes a voltage and time offset. The impact of the noise on the reference voltage is shown in Fig. 4.18. When the voltage on the capacitor crosses the reference voltage, the latch is triggered, which results in an 'early' or 'late' switching for a noisy reference voltage (or comparator). As can be seen, the impact on the timing jitter increases for a lower charging slope on the capacitor. The impact of this voltage noise, however, is related to the 'hard switching' of the comparators and can drastically be reduced by switching more slowly instead: the noise is averaged during the switching operation. In [92, 94] a differential pair is used instead of a comparator. Due to the longer switching period T_{switch}, the jitter caused by the noise on the reference voltage is drastically reduced. This results in a 0.8 μm 1.5 MHz oscillator with an rms jitter of 65 ps and a 150.7 dB phase noise FoM. The power consumption at 5 V is 1.8 mW. Due to the linear charging curves on the capacitor, similar to the previous implementations, a high control linearity can be obtained. However, when V_{ref} is lowered, this interacts with the non-zero switching period, resulting in an increased nonlinearity. This shows the trade-off between a high frequency range, a good control linearity and a low jitter. Unfortunately, the absolute accuracy of this oscillator is not mentioned.

The implementation in [90, 91] uses a different principle compared to the previously presented implementations. In [91] it is explained that the minimum achievable phase noise can only be achieved by decoupling the jitter and the comparator. A schematic of the proposed oscillator is shown in Fig. 4.19. The working principle of the circuit is non-trivial: at the beginning C_2 is charged to the level at which $I_{ds,M_1} = I_1$. At this moment the current I_1 is completely flowing through C_1. The voltage over C_1 is increasing, until the moment $V_{c2} - V_{c1}$ (the input of the comparator on the right) drops below the reference level $V_{ref,1}$. As a result ϕ is activated: C_2 is toggled ($V_{c2} = -V_{c2}$) and I_2 is activated. Due to the sudden voltage drop at both terminals of C_1, M_1 is completely switched off, and all the current $I_1 + I_2$ is flowing to C_2. Furthermore, I_2 also transfers an amount of charge from C_1 to C_2. This goes on until $V_{c2} - V_{c1}$ rises above $V_{ref,1}$. At that moment I_2 is switched off. During the following moments, I_1 is charging C_2. When V_{c2} is rising, M_1 slowly opens until $I_{ds,M_1} = I_1$ (at this point $V_{c2} = V_{ref,2}$). C_1 is charged further until ϕ is activated again.

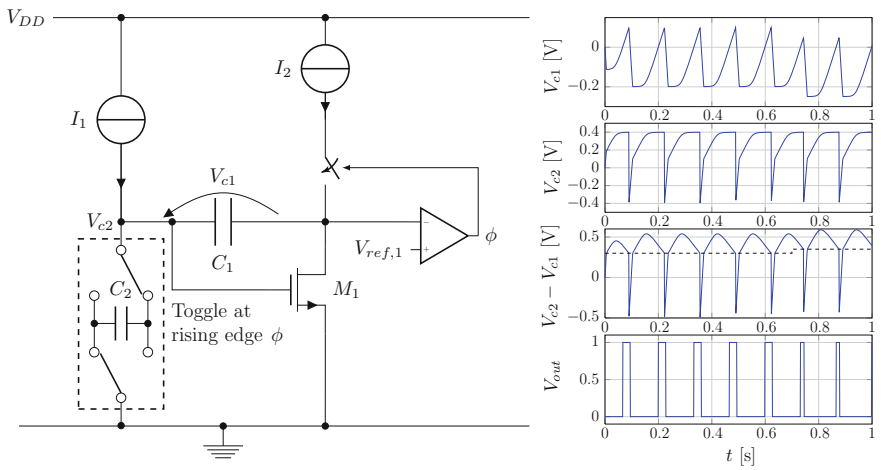

Fig. 4.19 Schematic of a low-jitter relaxation oscillator. The frequency is determined by C_2, I_1 and the value of V_{c2} at which the current through M_1 is equal to I_1, called $V_{ref,2}$. *On the right* the output waveforms of a simulated Matlab model are shown. The output signal V_{out} is obtained by putting V_{c1} through a comparator. As can be seen, $V_{ref,1}$ (*dashed line*) has no impact on the timing of the rising edges in the output signal

The interesting thing about this circuit is that the rising edge of the output signal V_{out} (i.e. the moment when V_{c1} becomes positive) is completely independent of the current I_2 and the reference voltage $V_{ref,1}$. To give an example: suppose that due to noise or a variation in $V_{ref,1}$ an increased amount of charge is pushed back by I_2 through C_1. This charge will result in a too fast increase of the capacitor voltage V_{c2}. However, V_{c2} always settles at the voltage at which $I_{ds,M_1} = I_1$ ($V_{ref,2}$) and the 'early charging' of C_2 is compensated by an exactly equal discharge of V_{c1}, which also has to be compensated for by I_1. From the moment C_2 is completely charged, the timing of the rising edge V_{c1} will therefore be exactly the same as expected. One period is therefore completely independent of I_2 or $V_{ref,1}$ and equal to the time it takes for I_1 to charge C_2 to exactly $2 \cdot V_{ref,2}$. By using a (slow-switching) transistor instead of a hard-switching comparator, this charge is determined very accurately and noise-independently (the noise is averaged over the switching period). In [90] this result in a 12 MHz oscillator with a phase noise FoM of 162 dB (compared to a theoretical limit of 165 dB, see Table 3.1).

Another interesting property of this oscillator is its temperature dependency. After analyzing the oscillator circuit, it can be seen that the oscillation frequency is equal to:

$$f_{osc} = \frac{1}{T_{osc}} = \frac{1}{T_d + \frac{V_{ref,2} \cdot C}{I_1}} \tag{4.77}$$

$$\approx \frac{I_1}{V_{ref,2} \cdot C} \tag{4.78}$$

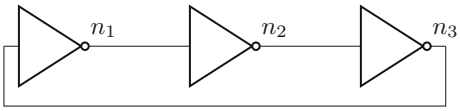

Fig. 4.20 Block diagram of a 3-stage ring oscillator

where T_d is the delay, or charge injection, caused by toggling the capacitor. $V_{ref,2}$ is determined by the properties of the transistor and is therefore sensitive to temperature variations. However, as described in Sect. 4.2.3.2, one biasing point exists at which the combination of V_{gs} and I_{ds} is temperature-independent (the ZTC point). When sizing the transistor in such a way that the ZTC point exactly coincides with $V_{c1} = V_{ref,2}$ and $I_{ds} = I_1$, a temperature-independent oscillation frequency is obtained. Due to mismatch and process variations, however, it is impossible to obtain this biasing without trimming or calibration. In [63] a 'Wobble' technique is presented to reach this biasing point automatically by use of a dynamic feedback system.

4.4.3 Ring Oscillators

Ring oscillators, of which the frequency is also determined by a combination of a resistor and a capacitor, can be considered as a special case of RC oscillators. Due to their high speed, low noise and the possibility for tuning, they are widely used in PLLs and clock recovery circuits [104, 127, 180, 181]. Most often, ring oscillators are realized as a closed ring of an odd number of cascaded CMOS inverter stages. This basic implementation makes them, however, vulnerable to supply noise. In [104] it is shown, however, that the impact on the phase spectrum of injected noise close to some harmonics of the oscillator frequency is reduced by taking the correlation between the oscillator stages into account. The impact on the amplitude spectrum, however, does not benefit from this correlation. In [180] it is stated that supply or tail-current noise is often the most dominant noise source in a ring oscillator. When looking at the working principle, they can both be analyzed in the analog and the digital domain. At startup, every inverter can be considered as an amplifier with a pole at its output. This means that a small sine wave, for which the total phase shift is equal to zero, propagates through the loop with an increasing amplitude. The frequency, at this moment, can easily be calculated using the small-signal transfer function of the inverter chain. Due to the typically high gain of a CMOS inverter, the amplitude grows rapidly. From the moment the signal starts to clip, the oscillator behaves more as a relaxation oscillator. Every stage has a delay t_d which is approximated by the voltage swing of the inverter times the output capacitance divided by the current through the inverter. The oscillating period is then $2 \cdot n \cdot t_d$ where n is the number of inverter stages. The oscillation frequency drops slightly when going from harmonic to relaxation operation (Fig. 4.20).

One of the drawbacks of a single-ended ring oscillator is the supply-noise sensitivity, the control nonlinearity and the limited output swing, which also depends on the

control signal. To improve the noise sensitivity, and to obtain a larger differential output signal, these oscillators can also be implemented using fully-differential inverters. A standard differential pair, however, only improves the supply-noise sensitivity. A better solution is to use a differential pair with a symmetrical load, as proposed in [171]. This results in a drastically improved control linearity, making it more suitable for use in feedback topologies. When using the correct biasing circuit, also the output swing of the differential cell is held constant as a function of the control and supply voltage, and the supply-noise sensitivity is reduced drastically [25].

The schematic of a single delay cell is shown in Fig. 4.21 [244]. In this design an open-loop compensation scheme is implemented. A bandgap reference is used to obtain a reference voltage. This voltage is used to stabilize the supply voltage, which is used by the other blocks. Another circuit is used to measure the V_{th} variation over temperature and process variations. In this way, the control voltage V_{ctrl} is generated, which is used afterwards to generate V_b using a replica of the oscillator stage. The resulting 3-stage 7 MHz ring oscillator has a ± 2.6 % frequency deviation over a -40 to 125 °C temperature span, over a 2.4–3 V supply voltage and over all process variations without trimming (94 samples of 2 different batches). This is a clear example of a second-level compensation technique.

The PVT effects can also be compensated for using a closed-loop approach instead. An example of this is presented in [149]. Again, a bandgap reference is used to generate a regulated supply voltage. The feedback uses a frequency to voltage converter to measure the oscillator output frequency. This signal is compared to a reference voltage (generated by the bandgap reference) and fed back to the oscillator. In this way, a frequency deviation of ± 0.05 % is achieved against a supply variation of 1.2–3 V. The temperature deviation is 67 ppm/°C over a -20 to 120 °C temperature span. The 10 MHz oscillator is processed in a 180 nm technol-

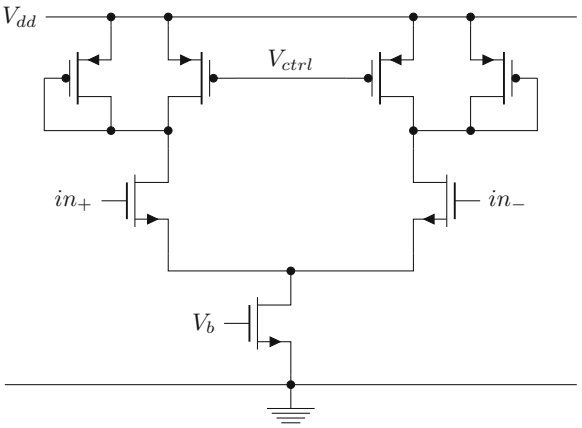

Fig. 4.21 Schematic of a fully-differential delay stage with a symmetrical load as used in [244]. The delay can be controlled through V_{ctrl}

ogy and consumes 80 μW at a 1.2 V supply voltage (including the bandgap reference). Another closed-loop design, using a frequency to current converter instead, is presented in [257]. This results in similar sensitivities as [149], however, using an externally applied control voltage.

4.4.4 Other Implementations

Over the years, different alternative clock reference topologies were invented. Some of them are discussed in this section. They are using different physical properties of silicon or other materials. Nevertheless, as will be shown, they all depend on the quantities discussed in Sect. 2.3. The oscillator structure itself is often not fundamentally different from previously discussed implementations. The implementations below are an attempt to obtain an *absolute accurate electrical parameter* from the silicon itself, which is afterwards used to implement a time reference.

4.4.4.1 Mobility-Based Frequency References

The mobility of the charge carriers in silicon depends strongly on the doping concentration and is an essential part of the MOSFET current equation (4.43) [40, 212, 219]. In [224] a circuit is presented that generates a current proportional to μ_n, as shown in Fig. 4.22. The output current of the circuit can easily be derived by noting that A_2 in combination with the PMOS transistors result in a low-voltage current mirror with a low input impedance. Transistor M_2 is diode connected through A_1 and R_0. Using the square-law MOS model (4.43), the output current can easily be shown to be [224, 225]:

$$I_{out} = \frac{\mu_n \cdot C_{ox}}{2} \cdot \frac{W_2}{L_2} \cdot \frac{V_R^2}{\left(\sqrt{\frac{n}{m}} - 1\right)^2} \tag{4.79}$$

where $n = (W_3/L_3)/(W_4/L_4)$ and $m = (W_1/L_1)/(W_2/L_2)$ and μ_n is the electron mobility. The main problem of using the electron mobility as an absolute reference is its temperature dependency, as shown in (4.49). In the 65 nm CMOS technology used in [225], measurements show that α_μ is around -1.4 to -1.6. Although this has to be compensated for by using a PTAT-dependent (externally applied) V_R, the main benefit of using the electron mobility is its matching properties.

The oscillator itself is a multivibrator similar to the one in Fig. 4.17, but using only one chopped comparator. The frequency deviation of the 100 kHz oscillator over a -40 to 85 °C temperature range compared to a $T^{-1.6}$ trend line, is below ±1.1 % after one-point trimming. When using a $V_R \propto T$ (PTAT), the frequency deviation over the same range is around ±2 %. The power consumption is 34 μW and the supply voltage dependency is below ±1.1 % from 1.12 to 1.39 V. It is, however, using 2.5 V thick-oxide devices to reduce gate leakage.

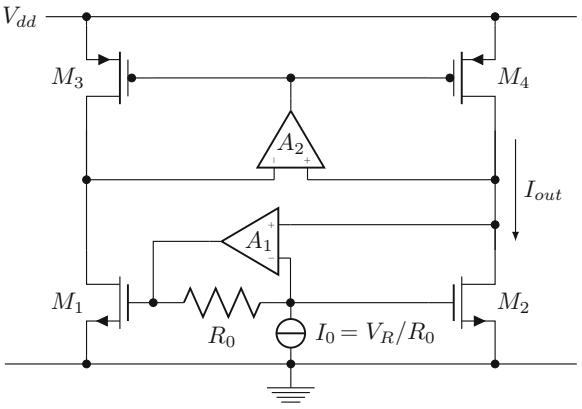

Fig. 4.22 Schematic of a mobility-based current source. The current I_0 is based on an externally applied reference voltage V_R

In [227], the same authors present a similar oscillator with integrated bandgap temperature sensor. This sensor, which was previously published in [226], has an inaccuracy of only ± 0.2 °C $(3 \cdot \sigma)$ over a -70 to 125 °C temperature range and consumes 10 µW. The output signal of the sensor is subjected to a nonlinear mapping, after which it is used to compensate for the temperature dependency in the electron mobility. The digital logic for the mapping as well as for the temperature compensation of the output frequency is done externally in an FPGA. The oscillator and the temperature sensor are integrated on the same 65 nm CMOS die and consume 51.12 µW from a 1.2 V supply. After one-point trimming, this design results in a ± 2.7 % frequency deviation over a -55 to 125 °C temperature range. This is reduced to ± 0.5 % when using two-point trimming instead. The sensitivity to a changing supply voltage is not reported in this work.

Another interesting implementation of a mobility-based oscillator is found in [71]. The proposed oscillator runs at 3.3 kHz and has an extremely low power consumption of 11 nW at a 1 V power supply. Similar to the previous design, a current is generated which is proportional to the mobility. The circuit is shown in Fig. 4.23. M_{n1} is operated in the triode region and therefore acts as a high degeneration resistance for M_{n2} and M_{n3}. The equilibrium of the circuit is reached when the loop gain, due to the local feedback by M_{n1}, reduces to one. When M_{n3} and M_{n4} are operated in weak inversion, V_B is given by:

$$V_B = \frac{k \cdot T}{q} \cdot \ln(N \cdot J) \tag{4.80}$$

It can be shown that the output current is equal to:

$$I_B = K_I \cdot \mu_n \cdot C_{ox} \cdot \frac{W_{n1}}{L_{n1}} \cdot 2 \cdot n \cdot \left(\frac{k \cdot T}{q}\right)^2 \tag{4.81}$$

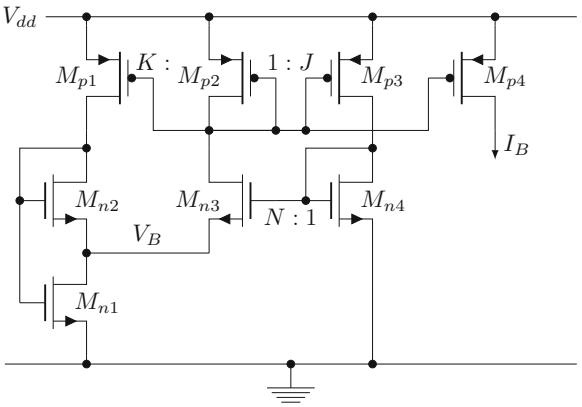

Fig. 4.23 Schematic of a mobility-based current source. By controlling the inversion level of M_{n1}, the output current I_B can be made PTAT

where n is the slope factor (see (4.44) and [219]) and K_I can numerically be calculated using the dimensions of M_{n1} and M_{n2}, K and V_B. By controlling the inversion level of M_{n1}, the output current I_B can be made PTAT.

This current is used to feed a low-power relaxation oscillator. The relaxation oscillator uses only one capacitor which is charged using I_B. When a reference voltage V_{ref} is reached, the capacitor is flushed and the cycle restarts from the beginning. Using a very similar circuit as the left two transistor branches of Fig. 4.23, V_{ref} is (similar to V_B) generated and found to be PTAT too. This results in a rather temperature-independent oscillation frequency. The oscillator itself is fed by a voltage regulator to obtain a reduced supply current (0.8 V) and to reduce the power consumption. A frequency deviation of 500 ppm/°C is obtained over a −20 to 80 °C temperature range. The frequency change over a 1–2.5 V supply voltage sweep is 3.5 %/V and the absolute accuracy is 20 % ($3 \cdot \sigma$).

Note that the working principle of mobility-based oscillators themselves is not different from other oscillators. In the two presented circuits, the frequency is based on a voltage, a current and a capacitor. Although the absolute matching of the mobility-based current source is quite good, the temperature dependency is a huge drawback. Although compensation of this is possible, this puts a lower limit to the reachable accuracy over temperature, unless (external) digital matching circuits are used.

4.4.4.2 Thermal-Diffusivity-Based References

Different from the previous category, oscillators based on a thermal filter are fundamentally different from other oscillators. Instead of using the energy reservoirs available in standard CMOS, the thermal capacity of the silicon substrate is used. In [125] an electro-thermal filter (ETF) has been demonstrated using an on-chip heating

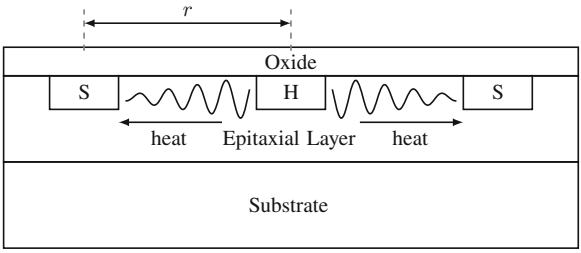

Fig. 4.24 Schematic drawing of an ETF. The heater (H) is driven with a square wave: the heat transfers through the silicon to the temperature sensors (S) which are laid out in circular pattern around the heater

element in combination with a temperature sensor at a distance r. This is schematically drawn in Fig. 4.24. The heater in the center is driven with a square wave. The heat transfers through the silicon towards the sensors (thermopiles) which are laid out circularly around the heater. The delay or phase shift between the input and the output signal depends on the geometry of the ETF and the thermal diffusivity D_{eff} of the silicon:

$$\phi_{ETF} \propto r \cdot \sqrt{\frac{f_{in}}{D_{eff}}} \tag{4.82}$$

where f_{in} is the applied input frequency. It is also shown that the thermal diffusivity is accurately defined in pure silicon, but is also temperature-dependent [170, 246]:

$$D_{eff} \propto \frac{1}{T^{1.8}} \tag{4.83}$$

Due to the high thermal conductivity of the silicon, the output signal is, for a few milliwatt at the input, typically in the order of several millivolt.

Due to the highly-accurate thermal delay of this structure, it can be used to lock an oscillator in a frequency-locked loop (FLL). A block diagram of this structure is shown in Fig. 4.25. In [126] a phase-domain sigma-delta modulator is used instead of the phase detector and a digital sigma delta modulator is used to generate ϕ_{ref}, the reference phase angle based on the output of an on-chip bandgap temperature sensor. In this way, the noise can be reduced (applying noise shaping) and the temperature dependency of the output frequency is reduced drastically, both in the digital domain. The ETF has been designed to obtain a 90° phase shift for a 100 kHz input at room temperature. Due to process variations in the 0.7 µm CMOS process used, the maximum mismatch is around 0.1°.

The oscillator used is a simple multivibrator similar to the one shown in Fig. 4.17. The charging current can be controlled to control the output frequency. The complete system has been processed in a 0.7 µm CMOS process and consumes 7.8 mW, of which 2.5 mW is dissipated in the ETF. The frequency inaccuracy after a single-point trimming at room temperature is ±0.1 % over a −55 to 125 °C temperature span

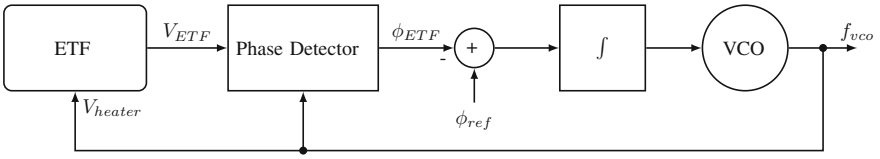

Fig. 4.25 Schematic drawing of an FLL using an ETF. The VCO locks on the thermal delay of the ETF, resulting in $\phi_{ETF} = \phi_{ref}$

($\pm$11.2 ppm/°C). The sensitivity to the 5 V supply voltage was unfortunately not reported.

4.4.5 Comparison of the Different Topologies

In the previous section, different oscillator topologies have been discussed. All of them have certain benefits and certain drawbacks, mainly depending on their topology, as will be pointed out in this section. In Table 4.1, the specifications of 6 previously discussed state of the art oscillator circuits are shown. These numbers clearly show the strengths and weaknesses. To demonstrate the fact that *there ain't no such thing as a free lunch (TANSTAAFL)*, the specifications are also qualitatively compared in a radar plot, Fig. 4.26. The length of the graph needed to describe a certain topology can be considered as a quality measure. When the state of the art advances, the circular plots on the graph move to the outside. Note, however, since most references do not mention all numbers, this graph is only included to show the design trade-offs. In Appendix D a complete overview of the discussed implementations is found, ordered in 4 different tables.

First, the 3 LC implementations will be discussed. As mentioned earlier, LC oscillators are typically used in RF applications, such as the local oscillator in a receiver or transmitter, because of their phase noise performance. This is clearly demonstrated in [155]. An important drawback, however, is the high frequency, which typically results in a high power consumption. Jou et al. [119] tries to avoid this by using a current-reuse circuit. This results in an acceptable power consumption, be it at the cost of a decreased noise performance. When looking at the long-term frequency stability, McCorquodale et al. [178] demonstrates a feasible solution. Due to the high core frequency and the used compensation circuitry, the power consumption increases drastically, which also deteriorates the phase noise FoM. After trimming, however, this results in a highly-accurate fully-integrated frequency reference, compliant with USB 2.0. As a result of the inductor, the core area is significantly higher compared to a relaxation oscillator. When looking at the field of WSN, LC oscillators are typically too power hungry. Although [119] is an attempt to solve this problem, it does not report any values on PVT stability.

The ring oscillator in [149] has a low-frequency output and an acceptable power consumption. Compensation circuits are used to reduce the PVT dependency, which

Table 4.1 Comparison of some implementations from literature

	[178]	[119]	[155]	[149]	[197]	[126]
Topology	LC harm.	LC harm.	LC ring	Ring	IV-C rel.	ETF-FLL
Technology	350 nm	250 nm	130 nm	180 nm	65 nm	0.7 µm
Frequency	12–96 MHz	2.4 GHz	5.1 GHz	10 MHz	9–30 kHz	1.6 MHz
Power consumption	31.4 mW	80 µW	4.01 mW	80 µW	120 nW	7.8 mW
FoM_{PN} (dB)	135.2	161	194.2	–	–	119.2
Rel. volt. range* (%)	20	–	–	85.7	75	–
Voltage sens. (ppm/%)	1.85	–	–	11.7	240	–
Temp. range (°C)	−10 to 85	–	–	−20 to 120	0 to 90	−55 to 125
Temp. coeff. (ppm/°C)	8.1	–	–	66.7	22.2	11.2
Absolute accuracy (ppm)	±100	–	–	–	–	±1,000
Core area (mm^2)	0.22	0.59	0.73	0.22	0.03	6.75
Trimming	Yes	No	No	No	No	Yes

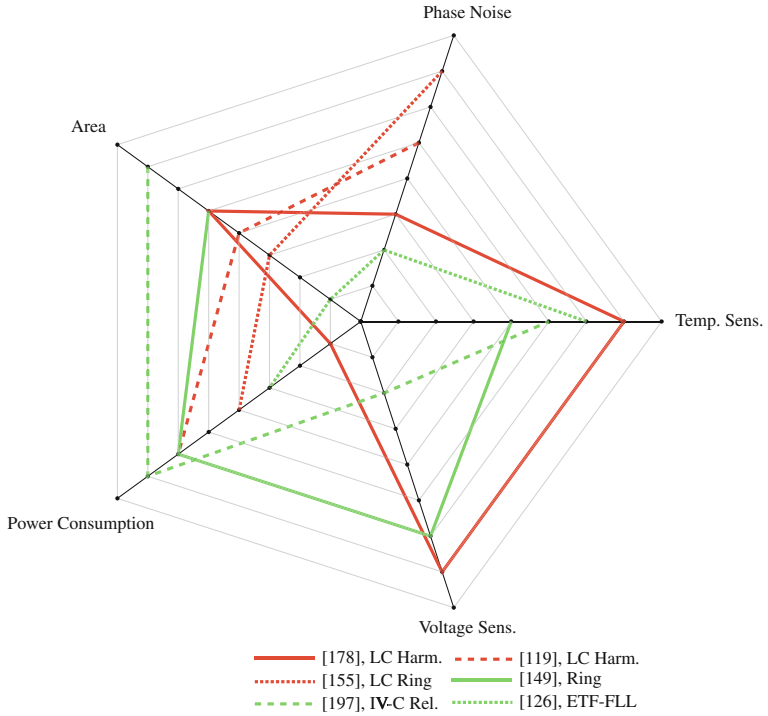

Fig. 4.26 Qualitative comparison of different integrated oscillator topologies from literature

results in a good temperature performance and a wide temperature range. The voltage dependency is good, however, only a small part of the 85.7 % voltage range can be used to stay below the 100 ppm frequency change within one burst. The lowest

power consumption is reported in [197], an IV-C relaxation oscillator. Again, the temperature dependency is really low, at the cost of an increased supply voltage dependency. This low-frequency oscillator is not suitable as a master clock on the tag, nevertheless, due to its extremely low power consumption it can be used as a watchdog timer in sleep-mode. Both the ring and relaxation oscillator have a small area, which is, certainly in [149] mostly occupied by the regulation circuitry.

The last implementation [126] mainly focuses on temperature stability. The power consumption as well as the phase noise performance suffer greatly from the use of the ETF, which is a power-hungry building block. However, the temperature dependency of this ETF-FLL architecture is highly process independent. After a 1-point trimming, this results in a long-term stability comparable to [178], consuming only one-fourth of the energy. In [178] a more advanced digital trimming scheme is used. Another, less important, drawback is the chip area.

From this discussion, it appears that none of the reported designs fully meets the required specifications for use on the wireless tag. The use of a standard LC topology is out of the question as a result of its high (core) frequency, resulting in a high power consumption. However, the non-common structure proposed in [119] demonstrates that low-power LC design is possible. The PVT dependency, which is inherently good for the LC tank itself, needs to be investigated further. Both the implementations in [149, 197] show that good results can also be obtained relying on integrated resistors and capacitors, often accompanied by a compensation circuit. Finally, the table also shows that (1-point) trimming is unavoidable in applications requiring an absolute accurate timing. Therefore, mostly RC implementations are investigated in this work. In Chap. 6, a more exotic LC implementation is studied.

4.5 Conclusion

In this chapter, the different sources of long-term frequency drift have been investigated. Starting from an ideal-oscillator model, the impact of a frequency dependent and distorted amplifier has elaborately been discussed. Afterwards, also the linearity and temperature behavior of the available CMOS components, actives and passives, has been studied, mostly using experimental data and models from literature. Different measures and FoMs for frequency accuracy have been defined. The remaining part of the chapter has been devoted to an exploration of the state of the art of fully-integrated (standard CMOS) timing references. This finally resulted in a comparison between the available oscillator topologies and a conclusion on their applicability in WSNs.

Part II
Oscillator Designs for Temperature and Voltage Independence

As pointed out in Part I, the spread on active components due to mismatch, temperature, and other external parameters is large and difficult to control. These effects are even more dominant in deep-submicron CMOS processes. Passive devices, or at least their linearity and temperature dependency, are much more predictable and controllable, providing a better starting point for an oscillator with PVT-independence. In this part, six design cases to obtain a voltage- and/or temperature-independent time value are studied and implemented.

In Chap. 5, two RC oscillator designs are discussed. The first design starts from the principle that the frequency should only be determined by passive components (R, C, or L) and that the influence of active components on the oscillation frequency should be minimized. It will be shown that at low supply voltages this methodology becomes difficult or even impossible. Therefore, a second RC oscillator design is designed, using control circuitry to keep the transistor parameters as constant as possible.

In Chap. 6, a completely different approach is taken. Instead of using a low-Q RC tank, an LC tank is used. Due to the high Q factor of the bondwire inductor, the energy losses in the tank are extremely small. As a result, the impact of the amplifier can drastically be reduced. In order to keep the power consumption as low as possible, an alternative 'pulsed' driving technique was developed. This results in a highly temperature- and voltage-independent low-power oscillator.

The designs in Chap. 7 do not rely on the absolute accuracy of a free-running oscillator anymore. A low-quality oscillator is built and injection-locked to an external RF reference clock. Two designs are discussed: the first locks to the carrier frequency and the second locks to an AM-modulated clock signal. In both cases this results in an exact low-power clock reference. The second design can also be used as an ultra-low-power AM-PSK receiver.

The last chapter of this part, Chap. 8, uses an oscillator as a sensor interface. To obtain a temperature- and voltage-independent sensor value, a ratio of two time values is used rather than an absolute time value. Simulations show that the proposed interface topology scales properly towards deep-submicron CMOS technologies. This design was implemented in 40 nm CMOS.

Chapter 5
Design of Two Wien Bridge Oscillators

In 1939, William Redington Hewlett, finished his master's degree thesis entitled 'A New Type Resistance-Capacity Oscillator' at the Stanford University. The oscillator made use of the RC network originated by Max Wien in 1891 [316]. *One of the main problems to obtain a proper sine wave at the output was the amplitude control: if the gain is too low, no oscillations occur, if the gain is too high, a square wave appears at the output. Hewlett proposed the following solution: 'For the variable resistance, a small tungsten lamp may be used. It is a well-known property of such lamps that as the current through them increases, the filament warms up, thereby increasing the lamp resistance.' By putting a light bulb in the feedback network, the gain automatically drops when the amplitude increases. This very first Wien bridge oscillator was commercialized together with David Packard as the HP 200, the very first product HP ever built.*

5.1 Introduction

It has previously been shown that oscillators can be based on different passive components. Since a low-power, low-frequency time reference is desired in low-power WSNs, RC-based oscillators are preferred rather than the LC-based topologies [218, 224]. A solution is found using a well-known harmonic oscillator structure: the Wien bridge oscillator [22, 32, 219]. As will be shown, however, the classical Wien bridge design using an operational amplifier is not suitable when external parameters such as supply voltage and temperature are varying. Therefore, an improved topology was developed, making use of a common-source amplifier instead. The use of this improved topology is applied in two design cases; a temperature-independent as well as a voltage-independent Wien bridge oscillator. The target specifications of both oscillators were previously summarized in Table 1.1. Note, however, that both oscillators address either temperature or supply voltage stability.

This chapter is organized as follows. The next section contains a discussion on the classical Wien bridge topology and its drawbacks in nanometer CMOS technologies. Afterwards, in Sect. 5.2, the development of the first topology is discussed. This

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oscillator is mainly important for its temperature independence. In this oscillator, the output frequency only depend on the passive (RC) feedback network. The amplitude regulator incorporated in the oscillator is investigated in Sect. 5.2.2. The noise propagation in the Wien bridge is discussed in Sect. 5.2.4. In Sect. 5.3 a second oscillator implementation is discussed, focusing on the supply voltage dependency. Since the design goals of both oscillators are completely different, it is difficult to make a comparison between both. Therefore, at the end of each section, each oscillator is compared to other state of the art implementations, focusing on the circuit novelties and strengths. Finally, in Sect. 5.4, a global conclusion is drawn.

5.1.1 The Wien Bridge Oscillator

The Wien bridge oscillator is a commonly used RC (or RL) oscillator topology, previously introduced in Sect. 4.4.1.2. The Wien bridge oscillator is a harmonic oscillator consisting of 2 building blocks: an amplifier and a passive RC-feedback network. A generic schematic of an RC Wien bridge oscillator is shown in Fig. 5.1. The transfer function of the feedback network is written as:

$$H(s) = \frac{s \cdot R \cdot C}{1 + 3 \cdot s \cdot R \cdot C + s^2 \cdot R^2 \cdot C^2} \tag{5.1}$$

It can be seen that, for an ideal Wien bridge oscillator, an amplifier stage with a gain of 3 is needed to obtain a stable oscillation (see Theorem 2.2). This results in the following oscillation frequency:

$$f = \frac{1}{2 \cdot \pi \cdot R \cdot C} \tag{5.2}$$

where R and C are the values of the resistors and capacitors in the feedback network. In the basic implementation (Fig. 5.1) the amplifier consists of an opamp and two

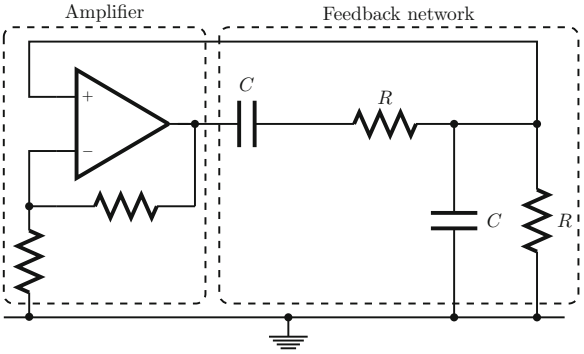

Fig. 5.1 Conventional Wien bridge topology using a passive feedback network and an opamp. Due to the feedback resistors, the amplifier has a gain of 3

feedback resistors to adjust the gain to 3. The Q factor of this harmonic oscillator is easily extracted from (5.1):

$$Q = 1/3 \tag{5.3}$$

The other calculation methods presented in Sect. 2.5.1, based on the phase and the gain of the feedback network, result in the same Q factor.

5.1.1.1 Frequency-Determining Factors

It is clear that, when using an ideal opamp in combination with two resistors to control the gain, the oscillation frequency only depends on the passive RC network (Sect. 4.2). If a temperature-independent oscillation is required, this network should consist of temperature-insensitive passive components. In most modern CMOS technologies, N- and P-poly resistors and MiM-capacitors are available. The temperature dependency of the capacitors is considered to be negligible (Sect. 4.2.4). Since the N- and P-poly resistors have a positive and a negative first-order temperature dependency respectively, a combined resistor with only remaining second-order temperature dependence is obtained. It appears that all of these components have a high linearity.

5.1.1.2 Implementation Non-idealities

Using a non-ideal opamp introduces a finite output impedance and possibly also a phase shift in the transfer function. The output impedance becomes part of the feedback circuit, thereby becoming a determining parameter for the oscillation frequency. Since the output resistance of the transistors changes considerably with temperature and supply voltage, and the pole frequencies in the amplifier (controlling the phase shift of the amplifier) are also affected, this poses a serious problem to obtain a PVT-independent oscillation. The opamp therefore becomes the critical part of the oscillator circuit. A PVT-stable oscillator using the conventional Wien bridge topology implies the use of a very high-performance opamp or alternative opamp configurations [22]. This, in turn, severely limits the low-power operating capabilities of such a circuit.

The impact of process variability makes matters even worse. The gain, output impedance and phase shift will have wide distributions, which has a large impact on the absolute accuracy of the oscillation frequency. To avoid this trade-off between power consumption, PVT stability and absolute accuracy, a new oscillator topology has been developed.

5.2 The Temperature-Independent Wien Bridge

The goal in this design is to obtain an oscillator of which the output frequency solely depends on the temperature-independent passives in the circuit. Indeed, by using an N- and P-poly combination, a first order temperature-independent

resistance is obtained, based on their respective temperature coefficients. Moreover, the temperature variation of both N- and P-poly resistors is only 2 % over a temperature span of 140 °C. In case of a 10 % resistor mismatch, this results in a temperature dependency of only 0.2 %, which corresponds to an extra 14 ppm/°C. As will be shown in Sect. 5.2.2, this is only one third of the deviation caused by the amplitude regulator. In the used 65 nm CMOS technology, the optimal ratio of the ideal N- to P-poly resistance was simulated to be approximately 2/3. The resulting temperature coefficient (36 ppm/°C) allows its use in a temperature-stable oscillator topology.

5.2.1 Basic Amplifier Structure

As explained in the previous section, the amplifier is the critical component in the Wien bridge oscillator. The requirements can be summarized as follows: (1) a constant output impedance, (2) no phase shift at $f = f_0$, and (3) a non-inverting voltage gain of 3. It is clear that these conditions have to be preserved under changing temperature and process variability.

The amplifier can easily be realized using a simple common-source transistor M_1 with drain resistor, as shown in Fig. 5.2. The drain resistor R becomes, together with the output resistance of the transistor r_0, part of the feedback network. Since the total output resistance $R_{tot} = R \| r_0$ determines the oscillation frequency and r_0 strongly varies with temperature, R_{tot} should only be determined by the temperature-stable resistor R. This is achieved by maximizing the output resistance of the amplifier r_0 by adding two cascode transistors (Fig. 5.4). In this way the total equivalent resistance R_{tot} is almost independent of r_0, the output resistance of the transistor branch.

The phase shift of the amplifier should be minimized at the oscillation frequency and is determined by the pole frequencies of the amplifier. Since poles exist at the sources of the cascode transistors, their sizes should be limited ($W/L = 3 \times 0.475\,\mu\text{m}/0.565\,\mu\text{m}$). A solution to the inverting behavior of the amplifier is found in cascading two (inverting) amplifiers with feedback network, as shown in Fig. 5.3. The result is a loop of two Wien bridge oscillators. A differential signal is found between the output nodes of the two amplifiers.

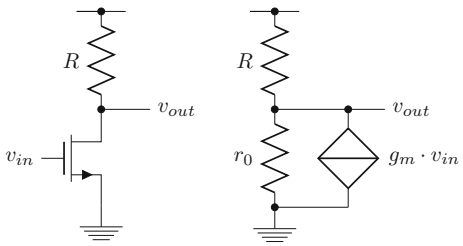

Fig. 5.2 Schematic and small-signal model of a common-source amplifier with drain resistor

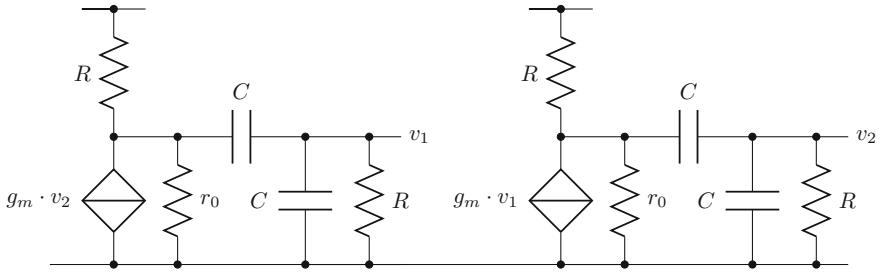

Fig. 5.3 Small-signal model of the improved Wien bridge oscillator Topology

5.2.1.1 Stability of the Voltage Gain: Source Degeneration

In a Wien bridge oscillator, a voltage gain of 3 is required. The voltage gain of the common-source amplifier is calculated to be:

$$A = g_m \cdot (R \| r_0) \tag{5.4}$$

where g_m is the transconductance of the transistor. As stated before, the output resistance of the transistor branch r_0 is maximized, resulting in an amplifier output resistance determined by resistor R, which is strongly temperature-independent. In contrast, the transconductance of the transistor g_m varies as much as 35 % over a temperature range of −40 to 100 °C, resulting in a large fluctuation of the gain. In order to stabilize this gain, source degeneration is used. Using this technique, the transconductance of the amplifier becomes:

$$g_{m,deg} = \frac{g_m}{1 + g_m \cdot R_{deg}} \approx \frac{1}{R_{deg}} \tag{5.5}$$

which is largely determined by the source resistor $R_{deg} = 11.94\ \text{k}\Omega$, a temperature-independent component (Fig. 5.4). This source degeneration also results in an increase of the output resistance by a factor $(1 + g_m \cdot R_{deg})$, which is favorable. Apparently there is a trade-off between the magnitude and the temperature stability of the transconductance. As the transconductance of a transistor can be written as:

$$g_m = \frac{2 \cdot I_{ds}}{V_{gs} - V_{th}}, \tag{5.6}$$

then an increased current through the common-source transistor is needed to enhance g_m and $g_{m,deg}$. Since, given a certain DC-biasing, the output resistance drops inversely proportional to the transistor current, the amplifier gain (equal to $g_{m,deg} \cdot R$) is not affected by the increased biasing current.

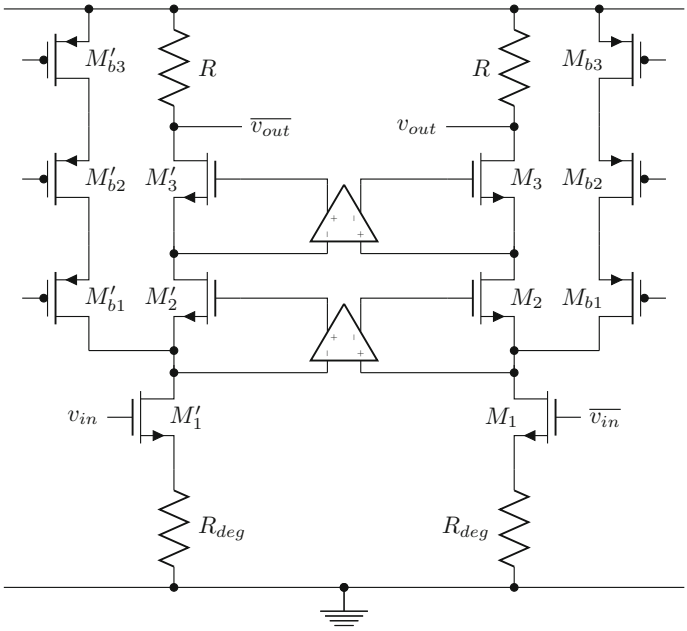

Fig. 5.4 Complete amplifier used in the Wien bridge oscillator

5.2.1.2 Increase of the Gain: Current Bleeding

A solution to the previous problem is found in the current bleeding technique. Using this technique, extra current can be delivered to the common-source transistor (increased g_m), without increasing the current through the cascodes (output resistance preserved) and output resistor R. To minimize the impedance reduction at the current bleeding node, two cascode transistors M_{b1}, M_{b2} are added to the inserted current sources M_{b3} (see Fig. 5.4). The resulting amplifier has a temperature-stable voltage gain of 3. Due to the high output impedance of the transistor branch (the transconductance amplifier), the output impedance of the amplifier is equal to R.

5.2.1.3 Controlling the Output Resistance: Gain Boosting

To increase the output resistance of the transconductance amplifier even more, gain boosting is applied to both cascode transistors. This results in an additional increase of the output resistance with a factor which is approximately equal to A, being the voltage gain of the gain-boosting amplifier. More important in this implementation, however, is the fact that gain boosting also has a positive effect on the phase shift of the amplifier: since the impedance at the source of the gain-boosted cascode transistor is reduced, its pole shifts towards a higher frequency. This reduces the phase shift of the amplifier at the oscillation frequency significantly and the amplifier can be used up to higher frequencies.

For reasons of compatibility with the differential architecture of the oscillator, the gain-boosting amplifiers have been implemented as fully-differential amplifiers. The gain-boosting amplifier used on the lower cascode is shown in Fig. 5.5. The input ($v_{in,+}$, $v_{in,-}$) and output ($v_{out,-}$, $v_{out,+}$) terminals are respectively connected to the sources and gates of the cascode transistors, as shown in Fig. 5.4, which presents the complete amplifier. The gain-boosting amplifier used on the upper cascode is similar, but uses a NMOS differential pair. Due to the limited supply voltage in 65 nm, capacitive coupling between the output of the gain-boosting amplifiers and the gate terminals of the cascode transistors is used. The resulting amplifier is shown in Fig. 5.4.

The Bode plot in Fig. 5.6 shows that the active frequency span of the gain-boosting amplifiers ($A_{gainboost}$) ranges from 200 kHz to 100 MHz (dashed lines). In addition, the reduction of the source impedance of the cascode transistors ($Z_{source,casc}$) near the oscillation frequency is also shown on the graph. Finally, the overall gain of

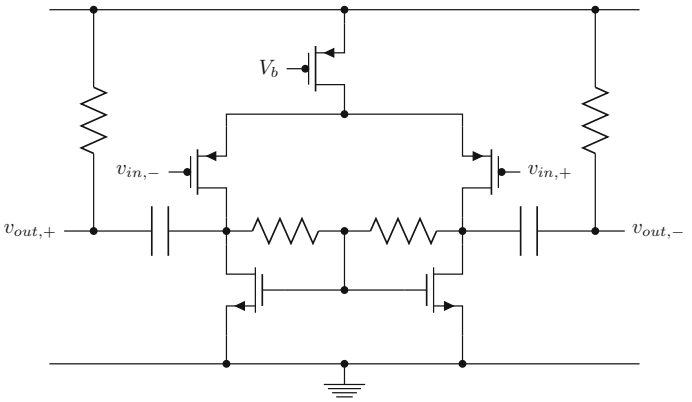

Fig. 5.5 Gain-boosting amplifier for the lower cascode transistors

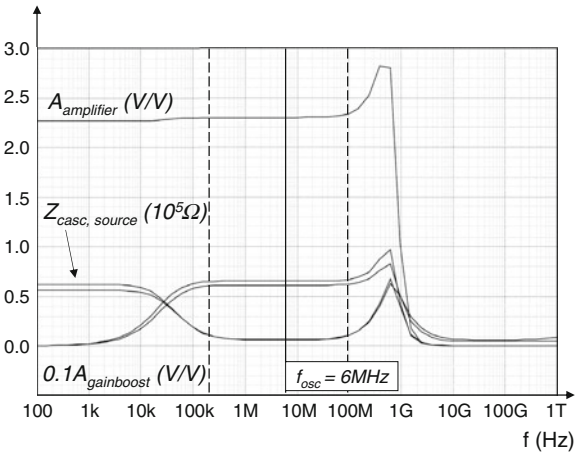

Fig. 5.6 Bode plot showing the gain of the gain-boosting amplifiers and the complete amplifier. The source impedance of the cascode transistors is also shown. The *dashed lines* indicate the active region of the gain boosters

the amplifier ($A_{amplifier}$) is visualized. The overall phase shift is below 0.4° up to a frequency of 24 MHz and below 2.1° at 48 MHz, resulting in a negligible phase shift at the oscillation frequency of 6 MHz. Note that even in a 48 MHz oscillator, the amplifier should hardly have an influence on the oscillation frequency.

Under all circumstances the simulated ratio between the transistor branch output resistance and the output resistor value R is higher than 1,000.

5.2.1.4 Guaranteeing the Absolute Accuracy

A lot of design decisions have been made to reduce the influence of the transistor branch on the oscillation frequency. Since this frequency is purely dependent on the passives in the feedback network, the accuracy of f_0 depends on the spread of these component values. In a CMOS technology, the spread of passive components is due to their bigger size typically significantly smaller compared to active components [198]. Furthermore, the absolute matching performance usually becomes better towards deep submicron due to the increasing resolution of lithography [23, 147]. In the worst case, the numbers presented in Sect. 4.2.4 (based on a 130 nm technology), are used. The expected mismatch in oscillation frequency (5.2) resulting from these figures within one wafer is about 1.1 %. The expected wafer-to-wafer frequency mismatch is 10–15 times higher [27]. Therefore, for each wafer some trimming could possibly be required.

5.2.2 The Amplitude Regulator

To make sure that the output impedance of the transistor branch remains high, the transistors have to operate in the saturation region. Furthermore, as shown in Sect. 4.2.2, any distortion on the output signal results in a frequency shift due to the harmonic work imbalance and needs to be avoided. This means that the output amplitude has to be limited prior to the deformation of the output signal. As shown in Sect. 2.2.3, this is only possible with a nonlinear circuit which influences the gain of the feedback amplifier.

Typically, an amplitude-regulation circuit consists of three parts: (1) measurement of the amplitude by peak detection, (2) integration of the peak signal on a capacitor, and (3) feedback to the gain of the amplifier. As described in [270], one of the main problems of an amplitude regulation using peak detection is its instability. A first pole in the feedback network can be found in the integrator. The second pole appears due to the delay between the gain adaptation and the amplitude change. This is, in a harmonic oscillator, a consequence of the finite Q factor of the resonator (Sect. 2.2.3). Furthermore, it has been shown that an instability in the amplitude regulation will cause a time-varying shift on the oscillator's frequency. Certainly in applications where a high frequency accuracy is required or where down-mixing is used, this is not acceptable.

5.2.2.1 Proposed Solution and Implementation

One solution to cope with this under-damped feedback system is to provide a shortcut around the second pole for high amplitudes. If the peak-detection circuit immediately influences the oscillation amplitude, this shortcut is realized. In the proposed amplitude regulator, the signal peaks are compared to a reference voltage V_{ref} which is generated using a replica of the amplifier (Fig. 5.7). If the peaks are too high, the signal will leak through the source of the peak-detecting transistors $M_{c,1}, M_{c,2}$. When the regulator network is in stable operation, only a very small peak current is running through these transistors, which makes the input impedance of the measuring circuit very high. The increased leakage current over temperature causes a small linear temperature coefficient of the input impedance. The larger the peak detection transistors, the more stable the amplitude regulator, but the higher the temperature-dependent leakage current will be. Good results have been obtained with a transistor size of $3 \times 0.65\ \mu\text{m}/3\ \mu\text{m}$.

The adaptation of the gain is done by adding a transistor between the two differential amplifier branches (between the sources of M_1 and M_1' in Fig. 5.4). This transistor controls the resulting source degeneration resistance, which in turn controls the gain. One important benefit of this technique is that it does not influence the DC operating point of the circuit, only the AC gain is altered in this way. The influence on the output resistance is negligible due to the shielding by the gain-boosted cascode transistors. Figure 5.8 shows the voltage gain as a function of the gate voltage of the 'bridge'

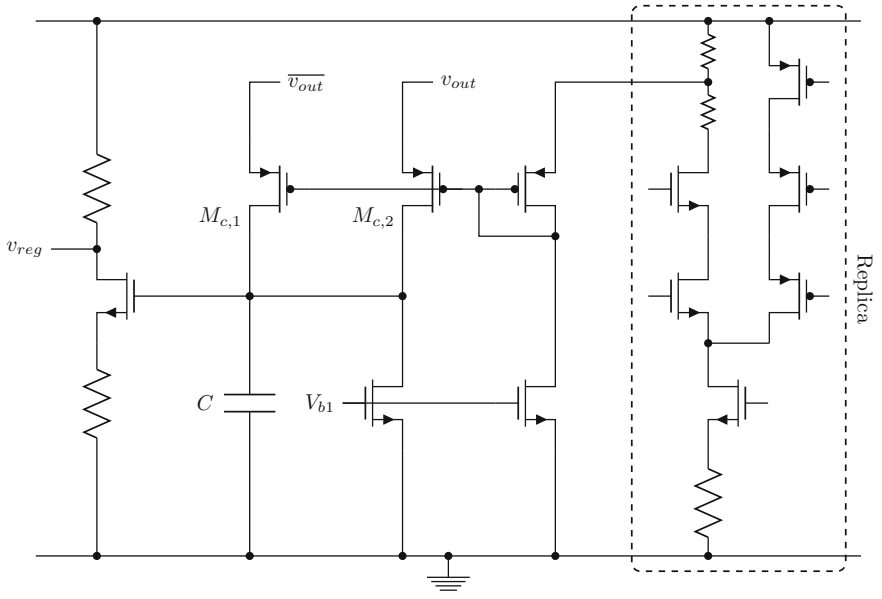

Fig. 5.7 Schematic of the amplitude-regulator circuit

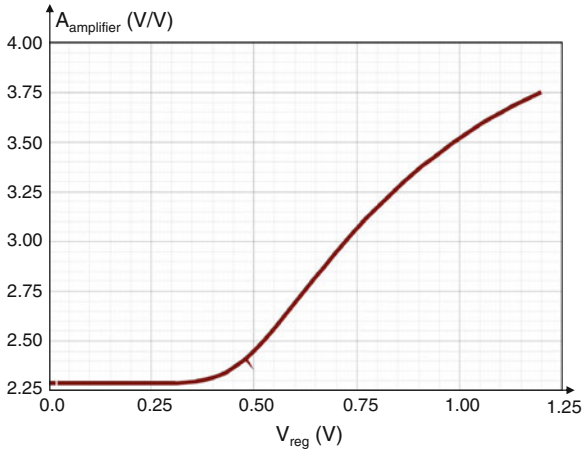

Fig. 5.8 Gain of the amplifier as a function of the voltage applied to the bridge transistor

transistor. By using a transistor of $W/L = 0.3\,\mu\text{m}/0.1\,\mu\text{m}$, a very wide tuning range ($A = 2.25 \ldots 3.5$) is obtained.

The complete amplitude-regulation circuit with peak-detection transistors $M_{c,1}$ and $M_{c,2}$, integration capacitor C, amplifier replica and feedback amplifier is shown in Fig. 5.7.

5.2.3 Complete Circuit

Using the different components discussed in the previous sections, the complete oscillator is now constructed. The schematic can be seen in Fig. 5.9, where the gain-boosting amplifiers and the amplitude-regulator circuit have been left out, to increase clarity. The current drawn by the input transistor is 10 µA, of which 60 % is flowing through the cascode transistors. The remaining 40 % is supplied through the current bleeding. The total power consumption, biasing included, is 66 µW at a supply voltage of 1.2 V. The feedback circuit, with a resistor value of 50 kΩ and a capacitor value of 530 fF, is designed to obtain an oscillation frequency of 6 MHz. At both outputs, two cascaded source followers have been added to provide a sufficient buffering of the signal. These are not drawn in Fig. 5.9.

5.2.4 Phase Noise Performance

Although the circuit was originally not designed for phase noise performance, it is interesting to identify the different noise sources. In this way it is possible to predict the noise behavior as a function of the power consumption and other design

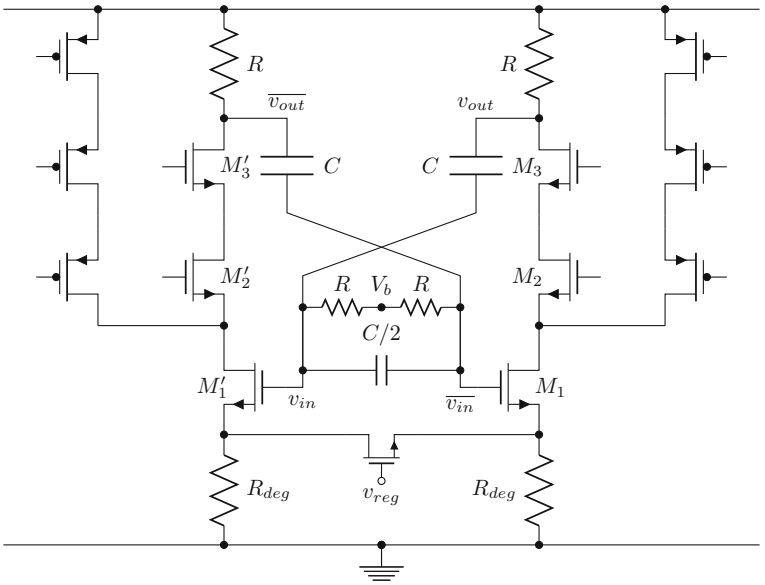

Fig. 5.9 Complete schematic of the Wien bridge oscillator. The gain-boosting amplifiers and the amplitude-regulator circuit are omitted for clarity reasons

parameters. Also the difference between the standard single-loop topology and the differential structure is investigated.

5.2.4.1 Noise in the Transconductance Amplifier

In a first step the resulting noise of the transconductance amplifier is modeled as a single current noise source $i_{n,A}$ at the output. This equivalent noise current is a combination of the most important noise sources in the amplifier (Fig. 5.10). Three different noise sources are drawn: a voltage source $v_{n,1/f}$ at the input, which represents the flicker noise at the gate-semiconductor interface and two current sources, $i_{n,tr}$ and $i_{n,R_{deg}}$, which represent the channel noise and the resistor noise respectively. As stated in [219], the noise of the cascode transistors and gain-boosters is negligible compared to the noise of the input transistor. Because the current sources for the current bleeding are not conducting any AC current, their dimensions and output resistance can be maximized in order to minimize the noise. This makes them negligible in the noise calculation. Consequently, the transfer functions of the different noise sources to the amplifier's output current can be calculated. The resulting noise contribution of the source resistor to the output noise is given by, using (3.3):

$$i^2_{n,R_{deg},out} = \frac{4 \cdot k \cdot T}{R_{deg}} \cdot \left(\frac{g_m \cdot R_{deg}}{1 + g_m \cdot R_{deg}} \right)^2 = \frac{4 \cdot k \cdot T \cdot g_m^2 \cdot R_{deg}}{(1 + g_m \cdot R_{deg})^2} \tag{5.7}$$

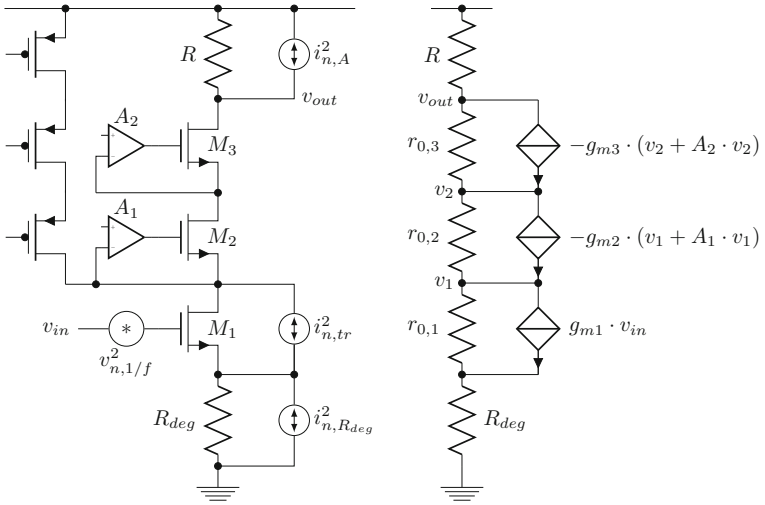

Fig. 5.10 Main noise sources in the transconductance amplifier

where k is the Boltzmann constant. The noise contribution from the transistor itself is caused by two complementary sources. The flicker noise is (3.10):

$$i^2_{n,tr,1/f,out} = \frac{K}{W \cdot L \cdot C^2_{ox} \cdot f} \cdot \frac{g^2_m}{(1 + g_m \cdot R_{deg})^2} \tag{5.8}$$

which is inversely proportional to f and where K is a transistor parameter dependent on the technology node. The other contribution of the input transistor is white channel noise and is given by (3.9)[1]:

$$i^2_{n,tr,out} = \frac{8 \cdot k \cdot T}{3 \cdot g_m} \cdot \left(\frac{g_m}{1 + g_m \cdot R_{deg}} \right)^2 = \frac{8 \cdot k \cdot T \cdot g_m}{3 \cdot (1 + g_m \cdot R_{deg})^2} \tag{5.9}$$

Note that the input transistors are rather large ($W/L = 5 \times 0.5\,\mu\text{m}/3.4\,\mu\text{m}$) to enhance their flicker noise behavior and eliminate the short-channel effects, which also have an influence on the transistor noise. The rms current of the resulting noise source $i_{n,A}$ at the output of the transconductance amplifier is calculated as the sum of these 3 contributions.

5.2.4.2 Noise Propagation in the Feedback Network

The noise of these different noise sources (amplifier and resistors in the feedback network) is then propagated and filtered by the feedback network. To calculate the

[1] The source, gate and drain resistance are not taken into account. They are considered to be negligible compared to R_{deg}.

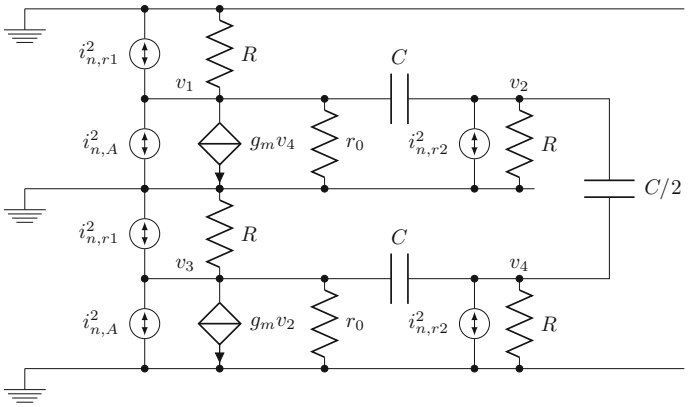

Fig. 5.11 Small-signal schematic of the differential oscillator. The noise contributions of the amplifier are grouped in $i^2_{n,A}$. Note that $v_{out} = v_1 - v_3$

different noise contributions to the output, it is necessary to calculate the transfer function of the feedback system from the noise injection points to the differential output. The small-signal network including the different noise current sources is given in Fig. 5.11. In this figure $i^2_{n,A}$ represents the estimated resulting noise contribution of the amplifier. Starting from this circuit and assuming that the voltage gain of each amplifier is equal to 3, the transfer functions from the noise sources to the output can be derived. The transfer function for the noise source (i^2_{n,r_2}) to the differential output is given by:

$$H_{n1}(s) = \frac{-(s \cdot R \cdot C + 3) \cdot R}{s^2 \cdot R^2 \cdot C^2 + 1} \tag{5.10}$$

The transfer function for a current source at the output of the transconductance amplifier (the noise contribution of the output resistance i^2_{n,r_1} and of the amplifier itself $i^2_{n,A}$) to the differential output is equal to:

$$H_{n2}(s) = \frac{-(2 \cdot s \cdot R \cdot C + 1) \cdot R}{s^2 \cdot R^2 \cdot C^2 + 1} \tag{5.11}$$

Note that in the case of a constant oscillation frequency, the transfer function is proportional to the resistor R in the feedback network. The noise transfer functions are plotted in Fig. 5.12. These transfer functions are also valid for the noise sources in a single-ended system (Fig. 5.13). The differential system contains twice as much noise sources than the single-ended oscillator. Due to the double output amplitude, the SNR at the output is therefore a factor of 2 better in the case of the differential system. Other important benefits of the differential structure compared to the single-ended structure are a lower sensitivity to supply and ground noise and a lower distortion of

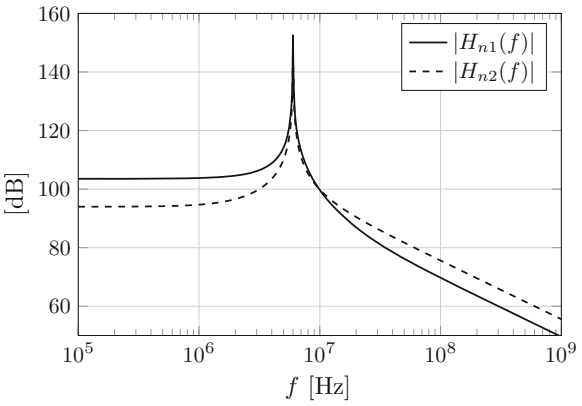

Fig. 5.12 Bode plot of the noise transfer functions. The sharp peak is the resonance frequency of the closed-loop system

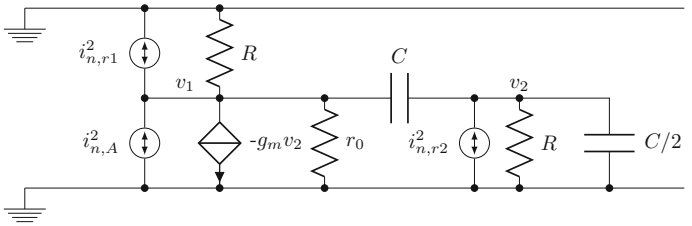

Fig. 5.13 Small-signal schematic of a single-ended Wien bridge oscillator. The propagation of the amplifier noise to the output is proven to be the same as in the differential case. Note that $v_{out} = v_1$

the output signal. Note, however, that the increased SNR is at the cost of an increased power consumption, which results in exactly the same phase-noise FoM.

5.2.4.3 Resulting Output Noise According to Leeson

The noise value at the differential outputs can be calculated as the overall noise power of the different noise sources. Each (quadratic) noise contribution is multiplied by 2 and by its transfer function. The noise at the differential output is then approximated by:

$$\begin{aligned} v^2_{n,diff} = \Big(& \frac{K}{W \cdot L \cdot C^2_{ox} \cdot f} \cdot \frac{g^2_m}{(1 + g_m \cdot R)^2} + \frac{4 \cdot k \cdot T \cdot g^2_m \cdot R_{deg}}{(1 + g_m \cdot R_{deg})^2} \\ & + \frac{8 \cdot k \cdot T \cdot g_m}{3 \cdot (1 + g_m \cdot R)^2} + \frac{4 \cdot k \cdot T}{R} \Big) \cdot 2 \cdot |H_{n2}(s)|^2 \\ & + \frac{4 \cdot k \cdot T}{R} \cdot 2 \cdot |H_{n1}(s)|^2 \end{aligned} \tag{5.12}$$

At high frequencies, the first term in this equation is inversely proportional to the third power of the frequency. Often it is believed that this noise contribution is responsible for the $1/f^3$ spectrum close to the output frequency. This implicitly assumes an up-conversion mechanism of the $1/f$ noise, which is unfortunately not present in the theory of Leeson. In the above equation, close to the oscillation frequency, the first term is negligible. The other contributions are inversely proportional to the square of the frequency and are therefore dominant in this region.

5.2.4.4 Resulting Output Noise According to Hajimiri

When using the LTV theory of Hajimiri instead, a mechanism exists to elucidate the $1/f^3$ behavior close to the oscillation frequency (see Sect. 3.4). To calculate the resulting output spectrum, the ISF must be calculated. When looking at the Wien bridge feedback network, this appears to be a difficult task. The sine wave present on both capacitors is not in phase, which makes the normalization of the state variables (see Sect. 3.4.3) and the definition of $q_{\max}$ non-trivial. Therefore, the ISF has been simulated using a Matlab model of the Wien bridge oscillator. Since the ISF only depends on the waveform, the feedback amplifier can be implemented using a tanh function with a gain around 3 to avoid distortion. Since the definition of $q_{\max}$ is ambiguous in this case, the ISF is normalized to $v_{\max}$, the maximum voltage difference at the output. This number is, naturally, proportional to $q_{\max}$. The simulated ISF is shown in Fig. 5.14. The rms value of both ISF functions is equal to:

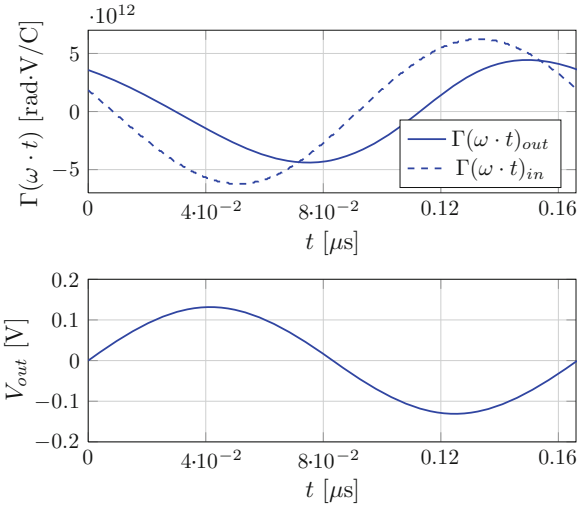

Fig. 5.14 ISF of the Wien bridge oscillator, normalized to the maximum output voltage $v_{\max}$. Two *curves* are shown, one for the input node and one for the output node of the feedback amplifier. In the *lower graph*, the output waveform of the oscillator is shown

$$\Gamma_{rms,out} = 3.10e + 12 \text{ rad} \cdot \text{V/C} \tag{5.13}$$

$$\Gamma_{rms,in} = 4.38e + 12 \text{ rad} \cdot \text{V/C} \tag{5.14}$$

Note that Γ is not dimensionless in this case, due to the different normalization. As expected from the previous section, the ISF at the corresponding nodes in the differential amplifier is exactly equal to that of the single-ended implementation. This was also confirmed by simulations. As can be seen in the figure, the most important contributions come from the noise sources close to the oscillator output frequency. When the distortion at the output node increases, also the contributions around higher harmonics become important (see (3.24)). Interesting to note is the fact that the ratio between both rms values is equal to $\sqrt{2}$, which is exactly the ratio of $H_{n1}(s)$ and $H_{n2}(s)$ in the neighborhood of the output frequency. This means that the resulting phase noise can also be calculated by first transforming all the noise sources to the amplifier output, after which only ISF_{out} needs to be simulated (or equivalently at the input).

The resulting phase noise in the $1/f^2$ region can now be calculated using (3.33):

$$\mathscr{L}(\Delta\omega) = 10 \cdot \log \left(\frac{\overline{\frac{i^2_{n,out}}{\Delta f}} \cdot \Gamma^2_{rms,out}}{2 \cdot v^2_{\max} \cdot \Delta\omega^2} + \frac{\overline{\frac{i^2_{n,in}}{\Delta f}} \cdot \Gamma^2_{rms,in}}{2 \cdot v^2_{\max} \cdot \Delta\omega^2} \right) \tag{5.15}$$

where $i^2_{\text{n,out}}$ and $i^2_{\text{n,in}}$ represent all the physical noise sources at the output and input node of the amplifier respectively (see Fig. 5.11). Note that, similar to the results of the noise model of Leeson, the differential case has a 2-fold increase of the noise power. The output power, however, increases 4 times, which results in a 3 dB increase of the output SNR. The up-conversion of the $1/f$ noise mainly depends on the DC value of the ISF, as shown in (3.35). When assuming a lowly-distorted output waveform, this term is assumed to be negligible. Furthermore, as seen in Sect. 3.6, the $1/f^3$ noise only weakly contributes to the cycle-to-cycle jitter.

5.2.4.5 Impact of the Amplifier Design

An important question is what will happen to a design with a different current in the amplifier. When the frequency is kept constant and the DC voltages of the circuit remain equal, g_m is proportional to the current and inversely proportional to the resistors R and R_{deg} in the amplifiers. As a result, the gain of the amplifiers does not change and the Barkhausen criterion remains fulfilled. Since the frequency is a constant and proportional to $R \cdot C$, R is inversely proportional to C.

$$g_m \sim C \sim I_{ds} \tag{5.16}$$

$$R \sim R_{deg} \sim 1/I_{ds} \tag{5.17}$$

When the biasing current is doubled, the noise transfer functions (Leeson) are divided by two. During simulation it appears that also the ISF is inversely proportional to the size of the capacitors in the feedback network. The current noise density, however,

doubles with the current increase (3.3). Looking at (5.12) and (3.33), this results in both cases in a linear increase of the noise with the increasing current.

Assuming that the active area ($W \cdot L$) of the input transistor scales linearly with the current (the transistor length stays constant), the contribution of the transistor flicker noise is inversely proportional to the power consumption. Moreover, the contributions of the resistors and the transistor to the total noise power are inversely proportional to the drain-source current of the input transistor. To enhance the phase noise performance at frequencies close to the output frequency, the width of the input transistor has to be enlarged. Considering Fig. 5.6, this can be done as long as the amplifier bandwidth is high enough and its phase shift remains negligible. For a fixed power consumption, one can also try to lower the noise by changing the DC biasing of the circuit. By lowering the resistors for a given current, however, the output amplitude is decreased. This keeps the Signal to Noise Ratio (SNR) at the output almost constant. In Sect. 5.2.5.2, the measured phase noise performance will be discussed.

5.2.5 Measurement Results

The complete circuit has been designed and processed in a 65 nm mixed-signal/RF CMOS technology. The capacitors used are MiM-capacitors. Resistors are implemented as a combination of N- and P-poly resistors. Note that no trimming or calibration has been used. The active area of the chip, including biasing and output buffers, measures 200 µm × 150 µm and is shown in Fig. 5.15.

5.2.5.1 Temperature Stability

During measurements, 7 samples from one batch have been characterized. The oscillation frequency is 5.998 MHz with a standard deviation of 53 kHz (0.88 %), both measured at room temperature. Figure 5.16 shows the temperature dependency of the

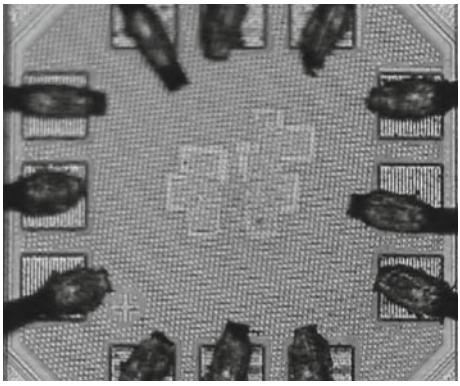

Fig. 5.15 Chip photomicrograph of the implemented Wien bridge oscillator

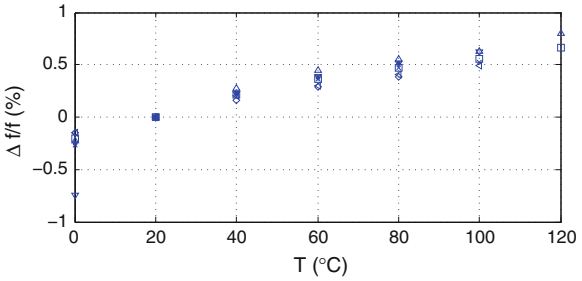

Fig. 5.16 Measured frequency deviation as a function of temperature for different samples. The frequency was normalized at 20 °C; some samples did not work at 120 °C

oscillation frequency for different samples in a temperature range from 0 to 100 °C. A linear frequency dependency of 86.1 ppm/°C exists, which corresponds very well to the simulated value of 81–92 ppm/°C, including process corners. This temperature dependency is mostly due to the input resistance of the amplitude regulator. However, this dependency can be compensated by the resistors (Sect. 5.2.5.3). Note that this is a second-level technique, which makes it vulnerable to mismatch between the actives and passives and possibly has unexpected results. The amplitude of the output signal remains constant, proving the correct operation of the amplitude regulator.

5.2.5.2 Noise Performance

In addition to the frequency stability, the phase noise of the oscillator (as defined by [101, Eq. (2)]) is also extracted with a single-sideband measurement using a Rhode and Schwarz FSIQ26 Spectrum Analyzer. In Fig. 5.17, the measured phase

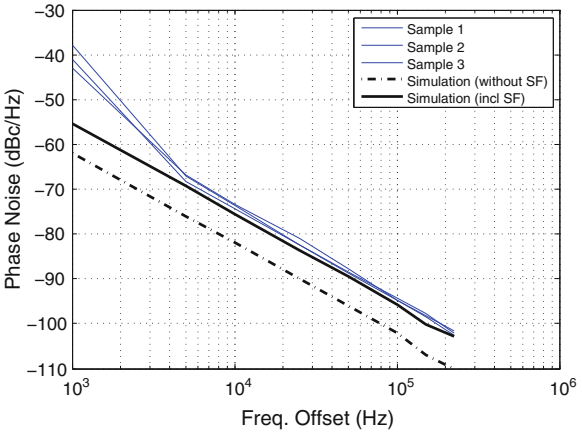

Fig. 5.17 Measured phase noise as a function of the carrier frequency offset for 3 different samples

noise density ($\mathscr{L}(\Delta f)$) is represented as a function of the frequency offset from the carrier (f_0) for three of the measured samples. The noise measurements are done at room temperature. At an offset frequency of 10 kHz and 100 kHz a phase noise of respectively −73, 7 dBc/Hz and −94, 6 dBc/Hz is measured at the output of the chip. On this figure, the simulated noise is also indicated (thick black line). Apparently, the measurements correspond very well to the simulations.

To compare the phase noise performance with other designs, the Figure of Merit (3.70) is calculated. This FoM compares the ratio of the the noise performance at a relative frequency offset to the power consumption $P_{\text{diss, mW}}$ of the circuit. Considering the conclusions of Sect. 5.2.4.3, increasing the oscillator power consumption will not have any influence on the FoM. At a frequency offset of 100 kHz, the following result is obtained:

$$FoM_{PN} = 10 \cdot \log\left(\frac{f_0^2}{\Delta f^2 \cdot \mathscr{L}(\Delta f)} \cdot \frac{1}{P_{\text{diss, mW}}}\right) = 142 \text{ dB} \tag{5.18}$$

Note that the measured data includes the noise added by source followers (SF), used as output buffers, on the chip. Since the noise performance of a source follower is very poor [219], this adds a noise floor to the oscillator output spectrum. However, it is observed that also the simulated noise in the $1/f^2$ region was affected by the addition of the source followers, which makes the results questionable. To the author's believe, this is caused by the fact that these transistors add a load capacitance to the oscillator outputs. This causes extra losses in the tank and an asymmetry in the tank capacitors, resulting in a higher necessary loop gain to preserve the oscillation. Apart from this, it is observed that part of the output noise is coupled through C_{gs} to the oscillator output node. This noise is transformed into an $1/f^2$ spectrum afterwards. The simulated noise of the oscillator itself, without the source followers as output buffer, is 5–8 dB below the phase noise at the output of the source followers. In this case, the equivalent value of the oscillator's phase noise FoM at a frequency offset of 100 kHz is:

$$FoM = 10 \cdot \log\left(\frac{f_0^2}{\Delta f^2 \cdot \mathscr{L}(\Delta f)} \cdot \frac{1}{P_{\text{diss, mW}}}\right) = 148\text{–}150 \text{ dB} \tag{5.19}$$

The question is, however, if this effect is as dominant in the measured prototype as at simulation time. Simulations show that a strong dependence exists on for instance the biasing and load of the output buffers. The deterioration of the noise performance should be avoided by a better design of the output buffers.

5.2.5.3 Possible Improvements

Since the simulated temperature behavior corresponds very well to the measured behavior, an improvement to the temperature dependency of the measured circuit

is simulated. In this circuit, the temperature coefficient of the amplitude regulator is compensated for by adding an opposite, first-order temperature coefficient in the resistors of the feedback network. This results in a simulated temperature dependence of 28–33 ppm/°C, which corresponds to the second-order temperature coefficient of the resistors (36 ppm/°C). Remember that the reported frequency mismatch is far below the predicted values in Sect. 5.1.1.1. However, before implementing this, some more samples should be measured to characterize the wafer-to-wafer mismatch accurately.

5.2.5.4 Comparison to the State of the Art

The most important properties of the circuit are listed in Table 5.1. In Table 5.2, a comparison is made between the presented circuit and some recently published temperature-stable and low-noise oscillators. The proposed topology appears to perform very well in a deep submicron CMOS technology. The temperature stability at an ultra-low power consumption is high compared to the other references. Compared to other low-Q resonators and relaxation oscillators, the phase noise performance is rather good [90, 101, 211]. No trimming or calibration has been used to obtain the reported results.

5.2.6 Conclusion on the Temperature-Independent Wien Bridge Oscillator

An improved Wien bridge topology has been developed, realizing a fully-integrated, low-power (66 μW), precise ($\sigma_{f_0} = 0.88\,\%$), temperature-independent (86.1 ppm/°C) oscillator. Advanced design techniques have been used to obtain a high-performance oscillator, of which the specifications are listed in Table 5.1. The measured temperature dependency and phase noise performance correspond very well to the simulated

Table 5.1 Overview of some key properties

Technology	65 nm CMOS
Frequency	5.998 MHz
Power consumption	66 μW
Temperature coefficient	86.1 ppm/°C
Absolute accuracy	53 kHz (0.88 %)
Phase noise	−73, 7 dBc/Hz @ 10 kHz
	−94.6 dBc/Hz@ 100 kHz
Phase noise FoM	142 dB
Area	200 μm × 150 μm

Table 5.2 Comparison to the state of the art for the temperature-independent oscillator

References	Type	Tech.	f (MHz)	T sens. (ppm/°C)	P (μW)	FoM (dB), (5.18)	Trimming/ Calibration?
This work	RC	65 nm	6	86	66 μW	142	No
[178]	LC	0.35 μm	12	12	31 mW	150	No
[275]	Relaxation	0.5 μm	11.6/21.4	303	400 μW	–	Yes
[231]	Ring	0.6 μm	0.68	106	400 μW	–	No
[244]	Ring	0.25 μm	7	400	1.5 mW	–	No
[90]	Relaxation	65 nm	12	–	90 μW	162	No
[94]	Relaxation	0.8 μm	1.5	–	1.8 mW	150.7	No
[72]	Relaxation	1.2 μm	148	1, 000	1.1 mW	146	No
[225]	Relaxation	65 nm	0.1	103	41.2 μW	–	Ext. PTAT ref.
[195]	Relaxation	0.13 μm	2	417	3 μW	139.7	Yes

values. As already mentioned, the frequency of the oscillator strongly depends on the linearity and output impedance of the amplifier. For high amplitudes, this poses a problem, which results in the need for an amplitude regulation. Similar problems arise when the supply voltage drops. This forces the cascode transistors into the linear region, resulting in a decreasing output resistance. Note that the power consumption and the temperature stability approach the target specifications, previously summarized in Table 1.1. It can, however, be concluded that the transistor stacking used in this design is not suitable for low supply voltages. Moreover, it will be seen that making an oscillation frequency independent of transistor parameters is hard or even impossible at low, varying supply voltages.

5.3 The Supply Voltage-Independent Wien Bridge Oscillator

As shown in the introduction (Chap. 1), one of the main problems in RFID tags using energy scavenging is the power supply, see Fig. 1.15 and [52]. When the RFID tag is operational, the energy reservoir is discharged and the supply voltage drops. Since most of the (digital) circuitry on a tag can run at low speed, this voltage drop and low supply voltage should not be a problem. However, for localization and communication issues, an accurate time reference is needed [157, 272]. Moreover, the lower the minimum operating voltage (V_{min}) and the power consumption of the circuitry, the longer the circuitry is able to work.

In this section, the design of an ultra-low-power, supply-independent clock reference is presented. Similar to the previous design, the circuit is based on a Wien bridge feedback network. Section 5.3.1 describes the problem of the changing supply voltage for different oscillator topologies. Afterwards, the proposed low-power oscillator is discussed in Sect. 5.3.2. Next, Sect. 5.3.3 discusses the used voltage and current regulator. The temperature dependency of the oscillator is briefly investigated in Sect. 5.3.4. In Sect. 5.3.5 the measurement results are presented and compared to state of the art designs. Finally, Sect. 5.3.6 concludes.

5.3.1 The Oscillator Topology

To make a supply-independent time reference, two possibilities exist: (1) make the time reference itself independent of the supply voltage, using for instance voltage-independent RC or LC resonators, or (2) build a voltage regulator serving as a stable voltage source to supply a low-voltage, possibly voltage-dependent, time reference.

5.3.1.1 Voltage-Independent Time References

The problem with a varying supply voltage is that the transistor properties change with it (Sect. 4.2). Switches become slower when the supply voltage drops and amplifier properties such as the transconductance and the output resistance are sensitive to the changing DC biasing conditions. These changing transistor parameters have an influence on the oscillation frequency.

To eliminate the influence of the active components in a harmonic oscillator, an ideal, voltage-independent amplifier is needed or the influence of the amplifier on the oscillation frequency has to be negligible. As shown in Sect. 4.4.1, this can be done using a high-Q LC tank. Unfortunately, this typically results in high frequencies and an increased power consumption [178]. Similar to the previous design, also an RC topology can be used. However, when the supply voltage drops below 0.5 V, the use of cascode transistors and gain-boosting is hardly possible. Furthermore, a high output impedance cannot be obtained because of the low drain-source voltage V_{ds}. Alternatively, also a relaxation oscillator can be used. It is observed, however, that the nonlinear circuitry (using transistors) is also sensitive to the reduced supply voltage, making T_d significant in (4.76). In this way, the frequency is affected by the changing supply voltage, even if the main frequency-determining components (mostly a capacitor and a resistive element) are kept constant.

5.3.1.2 Regulating the Supply Voltage

Another way to build a voltage-independent time reference is by using a low-dropout (LDO) voltage regulator. Typically a regulator consists of a voltage reference, an output transistor and a feedback amplifier (see Fig. 5.18). The output resistance of the regulator is equal to the $r_0 = V_E \cdot L/I$ of the output transistor M_{OUT} divided by the

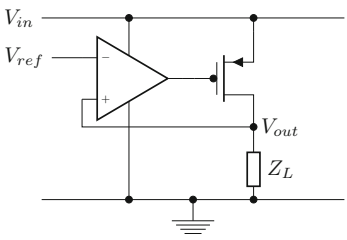

Fig. 5.18 An LDO regulator typically consists of a voltage reference, an output transistor and a feedback amplifier

loop gain. Hence, this output resistance becomes frequency-dependent. Furthermore, since V_{ds} changes drastically as a function of the power supply, the output resistance r_0 changes and also the gain of the feedback amplifier is voltage-dependent. A high loop gain and bandwidth, or a low r_0 is required to keep the output resistance low and diminish the influence of the regulator on the oscillator. This, however, will lead to an increased power consumption.

Still, there is an option to cancel out the influence of the regulator's changing output resistance. When a constant current is drawn from the regulator and the output voltage is kept constant, the output resistance is no longer influential. The challenge is to build an oscillator which has a constant power consumption over time. In the case of a relaxation oscillator, a constant power consumption is difficult or even impossible to achieve due to the non-linear switching. Harmonic oscillators on the other hand can be built with only linear components. Some differential topologies with a constant power consumption are available as demonstrated in the previous section [53, 219]. Therefore, this approach is used now to build a supply-independent time reference.

5.3.2 The Proposed Oscillator

Similar to the previous design, a Wien bridge oscillator is used. The oscillation frequency is given by (5.2). As explained earlier, amplifiers with a high gain and a low output impedance are difficult to realize in low-power and low-voltage operation. Therefore, in the proposed solution, the forward amplifier is a cascade of two inverting common-source amplifiers and the resistors in the feedback network are equal to the output resistance of the amplifiers, see Fig. 5.19. The parallel resistor to ground in the feedback network is implemented by a dummy amplifier. Both the output resistance

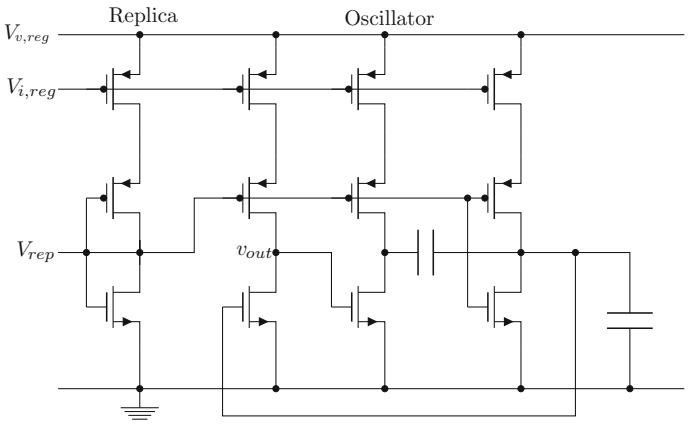

Fig. 5.19 The used Wien bridge oscillator. The resistors in the feedback network are implemented by the output impedance of the amplifiers. $V_{v,reg}$ and $V_{i,reg}$ are biasing voltages, both delivered by the regulator circuitry

and the capacitance of these low-power amplifiers become a part of the feedback network. For the biasing of the circuit, a replica, biased by the regulators (Sect. 5.3.3), is used. As discussed in Sect. 5.3.1.2, the output resistance of the regulators influences the oscillation frequency if the oscillator has a time-varying power consumption.

5.3.2.1 Coupling Two Oscillators

To overcome the problem of the changing regulator's output resistance, a differential structure is proposed: a combination of two oscillators oscillating in opposite phase. In the previous design this differential oscillating structure is built by cascading two amplifiers and two RC feedback networks. In the ideal case, this structure is completely differential. However, any mismatch between the amplifiers or feedback networks disturbs the phase shift of 180° between the two oscillators. Using Simpson's formula, one can easily prove that, for a small deviation, the variation on the drawn current is proportional to the phase shift, $2 \cdot \delta$, between the oscillators:

$$\begin{aligned} \sin(\omega \cdot t + \delta) - \sin(\omega \cdot t - \delta) &= 2 \cdot \sin(\delta) \cdot \cos(\omega \cdot t) \\ &\approx 2 \cdot \delta \cdot \cos(\omega \cdot t) \end{aligned} \tag{5.20}$$

Since in this design a cascade of two inverting amplifier stages is used, it is possible to couple the in-phase nodes of the two oscillators oscillating in opposite phase with coupling capacitors (see Fig. 5.20). To draw a constant current through the biasing current sources, each current source is shared by two differentially oscillat-

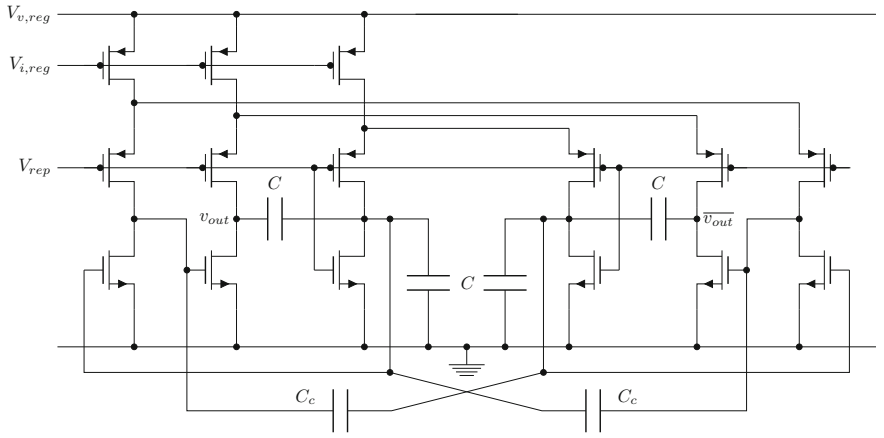

Fig. 5.20 The two oscillators are coupled in opposite phase by the coupling capacitors C_c. Note that the current sources of the differentially oscillating amplifiers are shared to draw a constant current over time. The biasing voltage V_{rep} is delivered by an amplifier replica; $V_{v,reg}$ and $V_{i,reg}$ are biasing voltages, both delivered by the regulator circuitry

ing amplifiers. The coupling capacitors C_c are in the order of 20 fF, which makes careful layout and parasitic extraction necessary. If any mismatch appears between the two oscillators, the resulting oscillation frequency is in between the two individual oscillator frequencies. However, both oscillators are always oscillating in opposite phase and the current consumption stays constant over time. Compared to the previously presented cascaded oscillator, the ripple on the drawn current is much lower for a capacitor mismatch of 10 %. The exact factor depends on the biasing current and so on of both oscillators.

The amplitude is controlled by the output resistance of the amplifiers, which decreases when the output amplitude increases. Because of the highly-regulated supply voltage, this results in a stable output amplitude. Adding an amplitude regulator in this case has little or no impact on the frequency stability, since this regulator has no influence on the temperature stability of the amplifiers' output resistances.

5.3.2.2 Operating in Weak-Inversion

Due to the low-power and low-voltage operation, the transistor devices in the amplifiers have a very low I_{ds} and $V_{gs} - V_{th}$, which makes them operate in weak inversion. In this operating region, I_{ds} has an exponential behavior as a function of $V_{gs} - V_{th}$, instead of the quadratic behavior in the saturation region (4.43 and 4.44). The following equation describes the behavior of a transistor in weak inversion. Note that also the dependency of the transconductance g_m on $V_{gs} - V_{th}$ is exponential [219]:

$$I_{ds,wi} = I_{D0} \cdot \frac{W}{L} \cdot e^{\frac{V_{gs}-V_{th}}{n \cdot k \cdot T/q}} \tag{4.44}$$

where I_{D0} and n are technology constants, T is the absolute temperature, k is the Boltzmann constant and q is the charge of a single electron. An important drawback of a transistor in weak inversion is the sensitivity of the DC biasing to transistor mismatch, process variations and temperature. To counter the process variations, as will be seen in the following sections, replica biasing is used. To improve the matching between the transistors every transistor is split into four parts and laid out in a way that the current flows in four directions (see Sect. 5.3.5). In this way the systematic mismatch is reduced [12, 220]. The temperature dependency on the other hand is a transistor property, which can of course not be solved by layout techniques. Although the temperature dependency of the oscillator is high (Sect. 5.3.4), for now it is assumed not to be a problem in the targeted application, since the temperature stays more or less constant during the short operation period of the tag.

Another drawback of ultra-low-power circuits is the noise. Due to the high impedance on the nodes in the circuit, a lot of noise is observed. Also the use of transistors in weak inversion has an impact [214, 277]. This noise contributes to the noise at the output and is translated to phase noise and jitter. However, in RFID

applications where the UWB pulses are used for localization, the distance measurement is hardly disturbed by the jitter of the oscillator [157, 272].

5.3.3 The LDO Regulator

To obtain a constant supply voltage for the oscillator, a voltage regulator is needed. The used regulator is shown in Fig. 5.21 and is based on the reference circuit on the left [42]. The output voltage of the reference, V_{ref}, is determined by the threshold voltages of M_1 and M_2. The leakage current of the NMOS transistors in cutoff is less than 150 nA. When the supply voltage varies from say 1.4 to 0.4 V the output voltage drops from 337.4 to 334.2 mV. Since this variation is still 1 %, a voltage and a current regulator are combined to further increase the stability.

5.3.3.1 The Voltage Regulator

One of the advantages of the LDO regulator used is the voltage reference which is part of the feedback amplifier (see Fig. 5.21). Due to the extremely low current in the regulator branches, the DC loop gain of this regulator is around 114 dB. The gain-bandwidth of the loopgain in the feedback system is around 820 kHz. Similar to the voltage reference itself, the output voltage of the regulator only drops 3 mV with an input voltage drop from 1.4 to 0.4 V. Figure 5.22 shows how the current regulator is nested within the voltage regulator. To keep the feedback loop of the voltage regulator stable, a Miller capacitor [219] is used to connect the gate of the output transistor to the output.

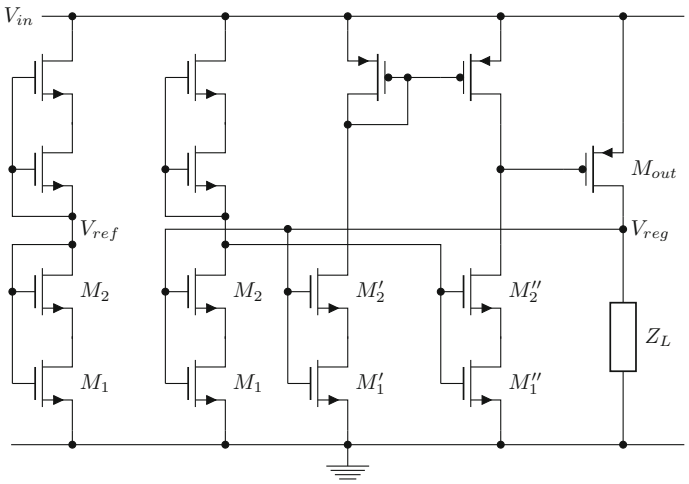

Fig. 5.21 The voltage regulator is based on the V_{th}-based voltage reference *on the left*. The output voltage is determined by the threshold voltages of M_1 and M_2

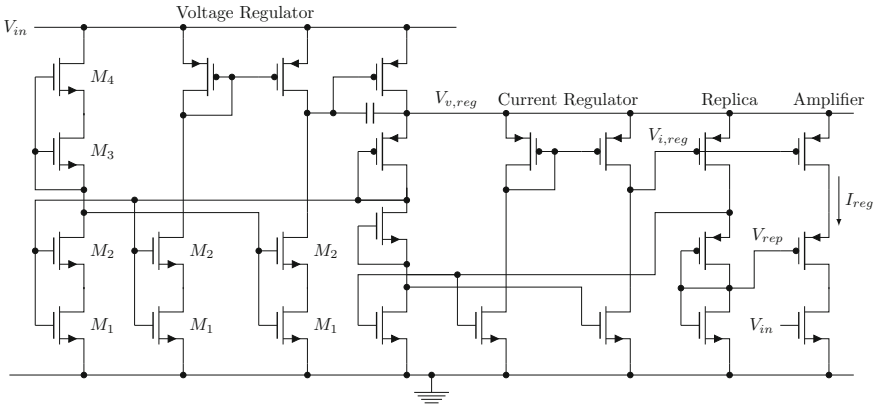

Fig. 5.22 Two regulators are used to provide a stable output voltage and current to the oscillator. The current regulator is directly connected to a replica of the amplifier used in the oscillator. The output current of the regulator only changes 0.02 % over a 1 V voltage drop

5.3.3.2 The Current Regulator

The current regulator has the same topology as the voltage regulator. Because of the lower voltage headroom, the cascodes are left out. This regulator is directly connected to a replica of the amplifier used in the oscillator. In this way the current regulator controls the biasing current sources in the oscillator. The DC loop gain in the current regulator is equal to 43.3 dB and the gain-bandwidth is 978 kHz. Due to the combination of two regulators, the current regulator output voltage and the amplifier's biasing current vary less than 0.02 % over a 1 V supply voltage drop. This is shown in Fig. 5.23. As can be seen, the output frequency variation is extremely low when the supply voltage varies. Around 0.4 V, the failure of both regulators is clearly visible. The frequency curve as a function of the supply voltage is horizontal. The nominal simulated oscillation frequency is around 36.3 MHz. After parasitic extraction, the simulated frequency drops to around 30 MHz. As will be seen when discussing the prototype chip, the measured frequency is even 20 % lower. This is probably caused by process variations and/or the fact that most transistors are biased in an outer corner of the transistor model (also a significant difference was notices between HSpice and Spectre simulations of the same circuit). The dip in the output frequency in Fig. 5.23 around 1 V, is probably caused by similar problems.

The loopgain of both regulators ($T_{v,reg}$ and $T_{i,reg}$) and the power-supply rejection ratio (PSRR) at the oscillator's output are plotted in Fig. 5.24. The current and voltage regulator have a phase margin of 70 and 58° respectively. These graphs are simulated at a supply voltage of 1.0 V. Around 0.4 V, however, the loop gain drops and the PSRR vanishes. Also, in these regulators most of the transistors are biased in weak inversion. The benefit of this is the low power consumption and the high DC gain in the feedback loop. Because of the high sensitivity of the circuit to the threshold

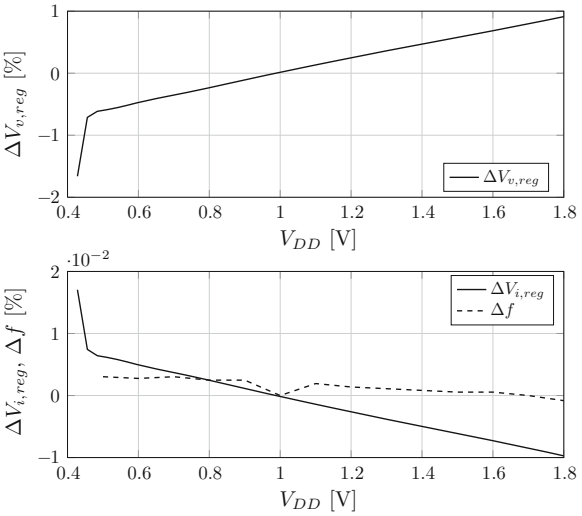

Fig. 5.23 Simulated output of the voltage and current regulator. The relative deviation compared to the output voltage at 1 V is shown. In the *lower graph* also the relative output frequency variation as a function of the supply voltage is shown

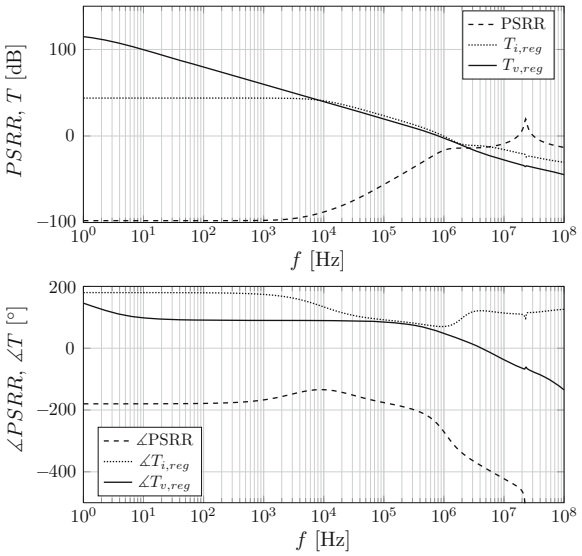

Fig. 5.24 Simulated loop gain of the regulators ($T_{v,reg}$ and $T_{i,reg}$) and the power supply rejection ratio (PSRR) at the output of the oscillator. The supply voltage is 1.0 V. The current and voltage regulator have a phase margin of 70° and 58° respectively

voltage of transistors M_1 and M_2, in this first prototype, the bulk of these transistors can be disconnected from the ground node. In this way, the bulk voltage (and V_{th}) of both the voltage and the current regulator transistors can be controlled from outside. Although a frequency mismatch was measured compared to the simulations, this feature appeared not to be necessary during the measurements to obtain a working oscillator. It was therefore only used for test reasons.

5.3.4 Temperature Dependency of the Voltage-Independent Oscillator

To illustrate the fact that making a temperature-independent frequency based on transistor parameters is difficult at low voltages, also temperature simulations have been carried out. Although it was not the goal to do any measurements on the temperature performance, the simulated behavior learns a lot about the required methodology at measurement time as well as the interpretation of the measurement results. The oscillation frequency is determined by a capacitor and the output resistance of the amplifier. This output resistance, on its turn, depends on the transistor parameters and the DC operating point, determined by the regulators. In Fig. 5.25 the temperature variation of the output voltages of both regulators and of the output current of the current regulator is shown together with the oscillator frequency. Although the

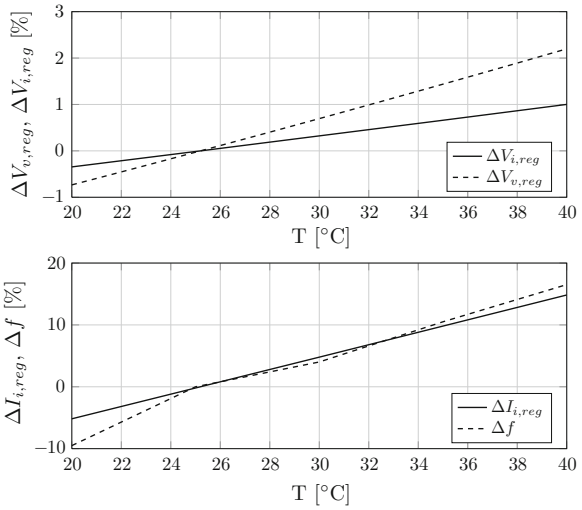

Fig. 5.25 Simulated output deviation of the regulators as a function of temperature. The *upper graph* shows the output voltage of the regulators. In the *lower graph*, the output current and the resulting oscillator frequency are shown

output voltages depend on the threshold voltage of a transistor, they are rather stable. The output current, on the other hand, strongly depends on temperature. This has an impact on the output resistance of the amplifiers. It can be concluded from this graph that this is the main cause of the huge temperature dependency of this oscillator. The temperature dependency is in the order of 10^4 ppm/°C.

To solve this artifact, one can try, instead of putting the replica as a reference load for the current regulator, to use a temperature-independent resistor. The results of these simulations are shown in Fig. 5.26. Hardly any improvement is observed. The output voltage as well as the current through the replica are still sensitive to the temperature. Furthermore, due to the mismatch between the resistor and the replica, the effect on the frequency is much more unpredictable. No significant influence, however, is noticed on the voltage sensitivity of the oscillator.

This temperature dependency has a huge impact on the measurement setup. It seems hardly possible to measure the oscillator output frequency without taking the impact of the temperature into account. Therefore, a measurement setup has been built to (1) generate fast (down to 1 to 10 ms) supply voltage transients of which the results are averaged over a high number of sweeps and/or cycles, and (2) to control the temperature accurately. To obtain this, the samples are bonded in a DIL-package, which results in a significant thermal mass. Furthermore, a PIC-controller and digital-to-analog converter (DAC) are used to generate the fast supply voltage drops. Note that in the intended Pinballs application, a wireless RFID tag which transmits short (0.5 ms) bursts, the temperature can be assumed to be constant during each burst operation.

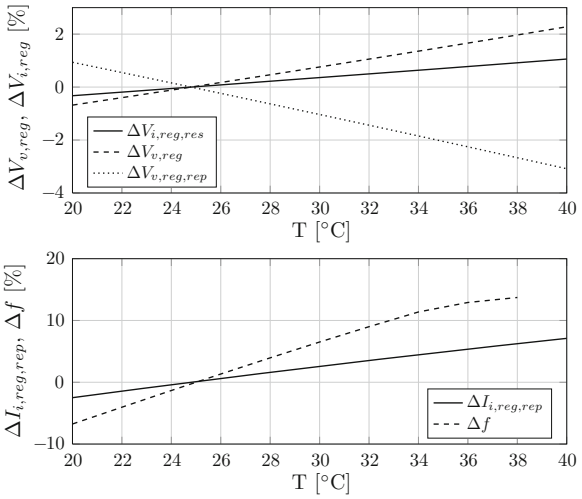

Fig. 5.26 Simulated output deviation of the regulators as a function of temperature when a resistor is used as the reference load of the current regulator. The *upper* graph shows the output voltage of the regulators and the voltage over the replica. In the *lower* graph, the output current through the oscillator replica and the resulting oscillator frequency are shown

5.3.5 Measurement Results

The oscillator has been designed in a triple-well 0.13 µm CMOS technology with low-threshold devices and 1.5 fF/µm^2 MiM-capacitors. A chip photomicrograph is shown in Fig. 5.27; the active area measures 200 µm × 150 µm. Due to the mismatch between the devices in weak inversion (Sect. 5.3.2.2), upscaling the devices was necessary. A point-symmetric layout, with every current flowing in four directions, was drawn to improve the matching, see Fig. 5.28.

Twelve samples of the same batch have been measured in a temperature-controlled measurement setup and worked over a supply voltage range from 0.4 to 0.4 V. The maximum frequency variation was only 104 ppm over this span, when averaged over a high number of supply voltage sweeps to obtain the required resolution and smooth curves. The measured oscillation frequency was 24 MHz, which is suitable for UWB

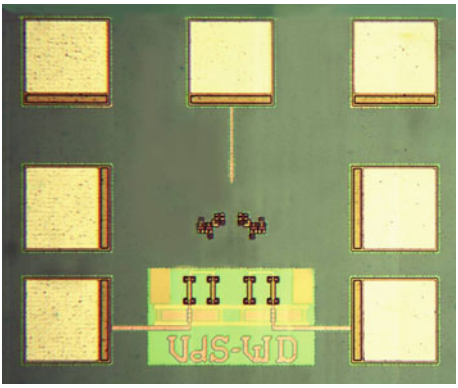

Fig. 5.27 Chip photomicrograph of the proposed voltage-independent oscillator; the active area measures 200 µm × 150 µm

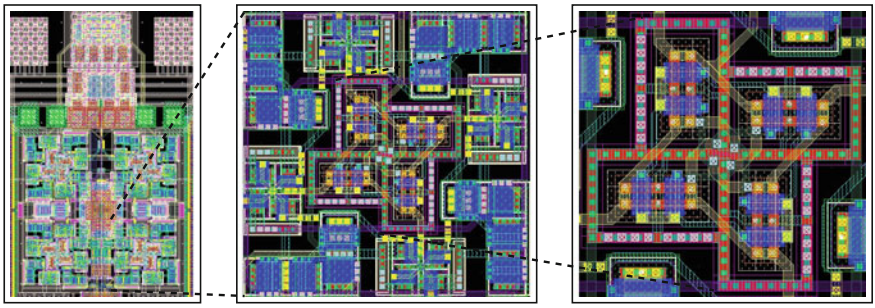

Fig. 5.28 The layout of the oscillator core is built completely point-symmetrically. Every current is flowing in four directions to reduce the systematic influence of the silicon crystal and other non-isotropic influences

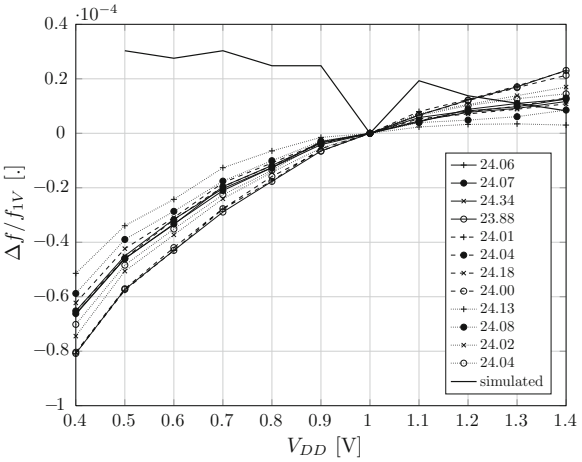

Fig. 5.29 Relative frequency deviation of the measured oscillator samples. *On the right*, the oscillation frequency of each sample at 1 V is reported. The maximum frequency variation is 104 ppm over the 0.4–1.4 V supply voltage span

applications. Figure 5.29 shows the normalized frequency of the different samples as a function of the supply voltage. Also the simulated frequency drift is shown on this graph. Although the temperature of the measurement setup is held constant, the measured frequency drift can possibly be explained by an (intra-die) temperature drift due to the increased power dissipation in the regulators. In the insertion on the right, the center frequency at 1 V is given for each sample. The measured difference between the oscillation frequencies at 1 V is 466 kHz or 2 % over the 12 samples. When a higher absolute accuracy is needed, this can be achieved by trimming the center frequency. However, unless a better temperature behavior is implemented first, this is of no use. The oscillator works without any external biasing except for the supply voltage. No trimming or calibration was used to obtain the reported results.

Since the oscillator (including the regulators) has a constant current consumption of 37 µA, the power consumption decreases proportionally with the supply voltage. If the supply is delivered by a capacitor, the voltage on the capacitor decreases linearly due to the constant current. The average power consumption of the oscillator from 1.4 to 0.4 V is then 33 µW. A separate supply voltage was used for the on-chip output buffers, as these are not needed in a real RFID-tag. In Table 5.3, a comparison is made with other state of the art oscillators. Only [178], a high-Q LC oscillator, has a lower voltage sensitivity. Due to the ultra-low-voltage capabilities, however, the power consumption of our design is the lowest compared to the other designs. Note that this is also the only implementation working over this wide voltage range.

Table 5.3 Comparison to the state of the art for the voltage-independent oscillator

References	Tech. (μm)	Oscillator	f (MHz)	V sens. (ppm/V)	I (μA)	V-range (V)	Rel. V-range (%)[a]	Trimming/Calibration
This work	0.13	Harmonic, RC	24	104	37	0.4–1.4	111	No
[250], ISSCC09	0.18	Relaxation, RC	14	16e3	24	1.7–1.9	22	No
[192], SBCCI03	0.5	Relaxation, RC	12.8	5.5e3	133	2.5–5.5	75	Yes
[178], JSSC07	0.35	Harmonic, LC	12	38	9.5 mA	4.5–5.5	20	Yes
[244], JSSC06	0.25	Ring	7	17.3e3	600	2.4–2.75	14	No

[a] $\Delta V_{rel} = 2 \cdot (V_{\max} - V_{\min})/(V_{\max} + V_{\min}) \cdot 100\,\%$

5.3.6 Conclusion on the Voltage-Independent Oscillator

In this section, a supply voltage-independent oscillator has been developed. Because of its intended application, i.e. use on an autonomous RFID tag, the available energy is extremely limited. The fact that it can work at low supply voltages (down to 0.4 V), makes it suitable for use in applications where for instance RF scavenging is used. Two nested regulators are used to generate a 230 mV stable supply voltage for the oscillator, resulting in a 104 ppm/V supply voltage dependency. This supply voltage dependency closely approaches the target specifications which were previously summarized in Table 1.1. The most important drawback is the temperature dependency, which is in the order of 10^4 ppm/°C.

5.4 General Conclusion

This chapter has described the development of two Wien bridge oscillators. During the first design it has been shown that a temperature-independent frequency reference can be obtained by making the oscillation frequency independent of the transistor parameters. For this purpose, a novel amplifier topology has been developed starting from a common-source amplifier. Cascode transistors and gain-boost amplifiers have been used to obtain an extremely high output impedance, which is negligible compared to the frequency-determining resistors in the feedback network. In order to control the signal amplitude, an amplitude regulator is used. This prevents the cascode transistors to come out of the saturation region.

The second design is intended for use on an autonomous wireless sensor node. Therefore, it needs low-voltage operation, which makes cascoding and gain-boosting impossible. This results in an oscillation frequency which does depend on the transistor parameters. It is mainly the output resistance of the used amplifiers which is dominant in this case. Two regulators are used to keep the DC biasing of the amplifiers constant over a changing supply voltage. This has resulted in a highly supply voltage-independent oscillator. The output resistance of the amplifier, however, strongly depends on temperature. Therefore, also the application field of this oscillator is limited.

Because of the different specifications of both oscillators, they have been compared to other state of the art implementations at the end of each section (see Tables 5.2 and 5.3). At the end of this work, in the conclusion chapter, a comparison is performed between all designed oscillator implementations and the target specifications (Table 1.1). In the following chapter, an oscillator topology is demonstrated which overcomes both the temperature and the supply voltage dependency. As will be seen, a high-Q resonator makes it much easier to get rid of temperature- and voltage-dependent transistor parameters, be it at the expense of chip area and/or non-complete monolithic integration.

Chapter 6
The Pulsed Oscillator Topology

When the director of an orchestra wants to know the correct tone height, he takes his tuning fork out of his pocket and hits it to his lectern. Although the tuning fork is only excited during a very short time, it can be used as an extremely accurate frequency reference. Due to the lack of any amplifying components, the frequency only depends on the mechanical properties of the high-Q resonant tank. When a small flute is used instead, the tone height is affected by the applied air flow, which results in a less accurate frequency reference.

6.1 Introduction

In the previous chapters, it has been shown that making an output frequency independent of PVT variations costs a lot of effort. Generally speaking, this is not caused by the variations of the tank components themselves (passives), but by voltage- and/or frequency-dependent parasitics in the feedback amplifier. To reduce the influence of the amplifier, a high-Q tank can be used. In this way, the energy losses in the tank are low, and the amplifier only has a minor impact on the resulting output waveform. In standard CMOS, the only available high-Q tank is an LC tank. This, however, typically results in a high-frequency oscillator, which drastically increases the power consumption of the oscillator circuitry. Furthermore, as shown in Sect. 4.4.1.1, for reasons of linearity, bandwidth, symmetry and supply noise, this often results in a differential topology, which doubles the power consumption. In this chapter, to counter these drawbacks, an alternative LC oscillator topology is investigated. The target specifications of the designed oscillator were previously summarized in Table 1.1.

Instead of using a standard harmonic oscillator, a pulsed-harmonic oscillator topology is proposed. The high-Q LC tank is not driven continuously. Instead, it is pulsed, after which a decaying oscillation appears at its output. As soon as the output amplitude drops below a certain level or when a certain number of cycles is

V. De Smedt et al., *Temperature- and Supply Voltage-Independent Time References for Wireless Sensor Networks*, Analog Circuits and Signal Processing 128,
DOI 10.1007/978-3-319-09003-0_6

counted, a new pulse is applied to the tank. As a result of this driving technique, the power consumption of the oscillator circuitry can be lowered tremendously. This is mainly because the continuously driving feedback amplifier is avoided. Also, the dependency on voltage- and temperature-dependent transistor parameters is lowered further since the driving transistors are only active in a small part of the oscillation period. During the remainder of the oscillation period, the LC tank is free-running.

When only looking at the free-running cycles of the oscillator, the phase noise is mainly determined by the quality factor of the LC tank. However, when a pulse is applied to the tank, the oscillation period is affected. Not only the phase noise performance suffers from this event, but also the output frequency of the oscillator is disturbed. The main drawbacks of this oscillator topology are therefore, depending on the application, the shape of the output waveform and its impact on the phase noise performance. Both of them are investigated below.

The chapter is organized as follows. The next section briefly describes the working principle and building blocks of a pulsed-harmonic oscillator. Section 6.3 focuses on the possible tank topologies, their transfer function and transient behavior. Next, in Sect. 6.4, the influence of the applied pulses on the frequency of the oscillator is investigated. Section 6.5 discusses the phase noise behavior of a pulsed oscillator. The implemented LC oscillator is presented in Sect. 6.6. In Sect. 6.7 the measurement results are presented. Conclusions are drawn in Sect. 6.8.

6.2 The Pulsed-Harmonic Oscillator Topology

Figure 6.1 shows a block diagram of a generic pulsed-harmonic oscillator. The main components of the oscillator are the tank, the amplifier and a counter to count the tank's output periods. After a certain number of cycles, the digital logic activates the pulse generator. The generated pulse is injected in the tank, typically this is done by an NMOS switch. This results in a waveform similar to Fig. 6.2.

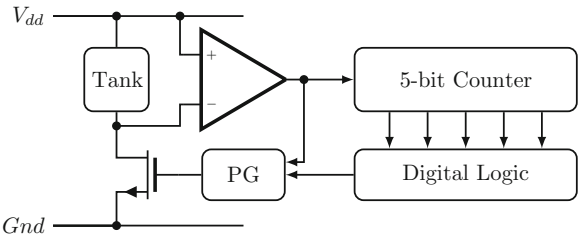

Fig. 6.1 Block diagram of a pulsed-harmonic oscillator. Instead of a negative resistance or g_m, only an NMOS switch is used to drive the tank. PG is the pulse generator

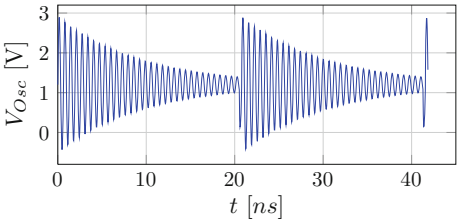

Fig. 6.2 Simulated output waveform of a pulsed LC oscillator. Between pulses the amplitude is decaying due to the losses in the LC tank

6.2.1 The Energy Tank

The frequency-determining component of the oscillator is the energy tank. Most integrated electronic energy tanks are RC or LC tanks. Other, external, tanks can be based on a ceramic resonator, e.g. a quartz crystal, or MEMS. Some commonly used tuned networks are shown in Fig. 6.3. Without loss of generality, the crystal can also be modeled as a series RLC tank in parallel with a capacitor [219, 278], as shown in Fig. 6.4. How and if the different tanks can be used in a pulsed-harmonic oscillator topology depends on the implementation of the tank and the Q factor. Apart from that, also the temperature and supply voltage dependency is determined by the tank. In Sect. 6.3, a more detailed analysis of the tank is performed.

6.2.1.1 The Amplifier

The function of the amplifier is to detect the oscillation signal and to amplify it towards the input of the counter. Besides the tank, this amplifier is the most energy-consuming part of the oscillator. As will be seen in Sect. 6.6.2, a very simple amplifier design is used in order to save energy. The main drawback of the used amplifier, which is a cascade of an NMOS differential pair and two differentially biased CMOS inverters,

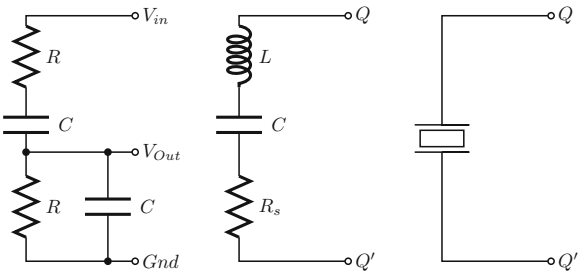

Fig. 6.3 Some of the possibilities to build a tuned network. RC and LC networks are commonly used in fully integrated oscillator implementations. Crystals can only be used as an external component

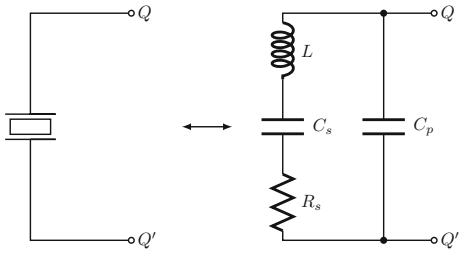

Fig. 6.4 A crystal can be modeled by a series LRC circuit with a capacitor in parallel [219]. This parallel capacitor C_p is mainly caused by the parasitics of the casing

is the limited gain and gain-bandwidth. This results in a limited capability to detect the small signals of the tank. On the other hand, by putting more effort in the amplifier design, by using a more complex, regulated topology or by improving the gain-bandwidth for the same output load, the power consumption will increase. Therefore, a trade-off exists between the number of free-running cycles, corresponding to a smaller output signal of the tank, lower supply voltages and a more low-power opamp design.

6.2.1.2 The Counter

The counter counts the periods of the amplified tank signal. Also for this building block many topologies are available in literature. Since the operation of the oscillator only depends on the toggling speed of the least significant bit, in most cases a down-counting ripple counter can be used. As will be seen, a feed-forward signal path is implemented in order to control the pulse length and the moment of impact more accurately. This, together with the output switch, will be discussed in more detail in Sect. 6.6.4. The flip-flop specifications are not that important except for the power consumption and the clock speed, which for the first flip-flop is equal to the frequency of the tank. The used TSPC flip-flop has a power benefit and, as will be explained in Sect. 6.6, can work with a clock signal which is not full swing [135]. This choice therefore relaxes the specifications of the preceding amplifier.

6.3 Transient Behavior of the Energy Tank

To understand and predict the behavior of the tank, a more detailed study is needed. In a first step, an n-th-order transfer function is analyzed. In the remainder of this section, the focus is on second-order, real energy tanks. For the case of a pulsed-harmonic oscillator, the transfer function or impulse response is an almost exact prediction of the oscillator's behavior.

6.3.1 The n-th Order Transfer Function

A resonant tank can be described by its current to voltage transfer function, i.e. its complex impedance. The most commonly used harmonic tanks can be described by a second-order transfer function. There are, however, many higher-order tanks available too. Therefore, a general n-th-order approach is taken here. The general equation of an n-th-order transfer function looks as follows:

$$H(s) = \frac{P(s)}{Q(s)} = \frac{a_m s^m + a_{m-1} s^{m-1} + \cdots + a_1 s + a_0}{b_n s^n + b_{n-1} s^{n-1} + \cdots + b_1 s + b_0} \tag{6.1}$$

It can be assumed that $n > m$; if not, $P(s)$ can be divided by $Q(s)$ to obtain a quotient and a remainder [114]. The zeros of the system are determined by the quotient and the remainder; the poles are only determined by the denominator of the remainder. Note that the number of poles always equals the number of zeros; $m > n$ means that there are $m - n$ poles at infinity. Since the quotient, which is a polynomial in s, translates to a sum of Dirac impulses and its derivatives in the time-domain impulse response, the oscillatory behavior of a harmonic tank is determined by the poles of the system. Moreover, for real electronic systems with limited output swing, the question is if a Dirac impulse and its derivatives are a valid output and the missing poles are really at infinity. Real systems always have a finite output swing and bandwidth. Without loss of generality it is therefore assumed that $n > m$. Before performing the inverse Laplace transform on the transfer function, $H(s)$ is split in partial fractions. In the general case, the denominator has real roots, p_i, as well as pairs of complex conjugate roots c_i and c_i^*. Each of these can have a multiplicity r_i or s_i. When writing the partial fraction form of (6.1) with $n > m$, this results in:

$$H(s) = \sum_i \sum_{j=1}^{r_i} \frac{K_{ij}}{(s - p_i)^j} + \sum_i \sum_{j=1}^{s_i} \left[\frac{L_{ij}}{(s - c_i)^j} + \frac{L_{ij}^*}{(s - c_i^*)^j} \right] \tag{6.2}$$

where K_{ij} and L_{ij} are called the residues. Using the inverse Laplace transform, the impulse response in the time domain can be written as:

$$\begin{aligned} h(t) = &\sum_i \sum_{j=1}^{r_i} \frac{K_{ij} t^j e^{p_i t}}{j!} \\ &+ \sum_i \sum_{j=1}^{s_i} \left[\frac{L_{ij} t^k e^{c_i t}}{j!} + \frac{L_{ij}^* t^j e^{c_i^* t}}{j!} \right] (t \geq 0) \end{aligned} \tag{6.3}$$

To interpret this impulse response, one has to understand the meaning of the different terms it contains. To obtain a stable system, which is always the case for a passive energy tank, it is clear that all the poles are located in the complex negative half plane, i.e. $p_i < 0$ and $\Re(c_i) < 0$ for all i and j. This means that all real exponential

envelopes in the impulse response are decaying. The real poles of the system only result in exponential (decaying) functions, which do not overshoot nor oscillate. Hence, since the focus is on oscillators, these decaying terms are neglected. The complex poles on the other hand result in exponential functions with a complex exponent. Using Euler's formula these terms are understood to be exponentially decaying oscillations.

6.3.1.1 Bode Plot Versus Impulse Response

The question at this moment is whether it is possible to predict the behavior (impulse response) of a pulsed tank from the Bode plot of the system. One can conclude from (6.2) that the poles close to the imaginary axis have more influence on the amplitude behavior than the poles with a more negative real part [78]. This is because of the exponential functions in the impulse response which decay rapidly. However, in [173] it is stated that the dominance of a pole is determined by the absolute value of the so-called residues K_{ij} or L_{ij}. When taking a closer look at (6.2), it is observed that around the pole frequency ω_i corresponding to $c_i = \sigma_i + j\omega_i$, the Bode plot is mainly determined by the terms with c_i in the denominator:

$$\begin{aligned} H(j \cdot \omega_i) &= \frac{L_{i1}}{(j \cdot \omega_i - c_i)} + \frac{L_{i2}}{(j \cdot \omega_i - c_i)^2} + \cdots + \frac{L_{is_i}}{(j \cdot \omega_i - c_i)^{s_i}} \\ &= \frac{L_{i1}}{\Re(c_i)} + \frac{L_{i2}}{\Re(c_i)^2} + \cdots + \frac{L_{is_i}}{\Re(c_i)^{s_i}} \end{aligned} \tag{6.4}$$

It appears that for a pole with single multiplicity not only the real part of the pole is determining the Bode plot, but the modulus of $L_{i1}/\Re(c_i)$ [216]. Poles with a higher multiplicity need a more careful approach by observing the combination of the different terms in (6.4). Similarly, it is also possible that more than one pole c_i has the same angular frequency ω_i. In this case a similar reasoning can be made by taking the terms of both poles into account. Again, it is the combination of the terms $L_{ij}/\Re(c_i)$ instead of only the residues, which is determining the Bode plot.

The question is now if it is possible to draw the same conclusions for the impulse response in the time domain? To analyze the impulse response (6.3), two different cases are observed: the behavior for t close to zero and for t higher than several time constants $-1/\Re(c_i)$. For t close to zero, the impulse response is mainly determined by the residues K_{ij} and L_{ij}. Frequencies with a high residue will be more present in the output signal than other frequencies. However, when t increases, the exponential functions decay rapidly. After some time, only the terms with the lowest negative real part will survive; by then, the influence of the residues has completely faded out. The difference between the Bode plot and the impulse response can be understood as the difference between the particular steady-state solution of the corresponding differential equation and the homogeneous solution or transient effects. In the case of a pulsed oscillator only the transient effects are important to discuss. To illustrate this,

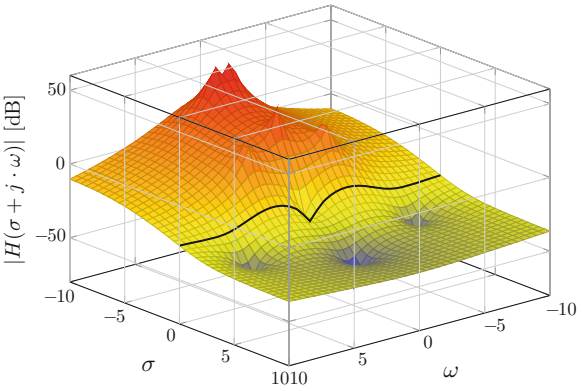

Fig. 6.5 When drawing the magnitude of a transfer function in the complex plane, it is seen that the Bode plot is the cross-section of this surface with the (*positive*) imaginary axis. Therefore, a Bode plot only shows the steady-state response of a system

Fig. 6.5 shows the relationship between a Bode plot and its corresponding transfer function: a Bode plot only contains the steady-state response of a system.

6.3.1.2 Usable Energy Tanks

To conclude this section, some required properties of usable tanks and transfer functions are listed. First of all, the tank must have complex conjugate pairs of poles with a low damping (a low real negative part). As can be seen in (2.66), this corresponds to a high Q factor. In this way, the oscillation at the pole's frequency will last for several cycles in the impulse response.[1] In the next section, some quantitative figures are connected to this property. Secondly, since the working principle of the pulsed oscillator is based on counting a certain numbers of oscillation cycles, it can be useful to limit the number of complex pole pairs in the transfer function. When one oscillation mode has a dominant residue (low t) and the smallest negative real part, the oscillation coming from this mode is always observable and probably the easiest to count. It is therefore advisable to design a tank with a controllable number of poles. In the next section this general approach will be applied to existing second-order tanks.

6.3.2 Realistic Second-Order Tanks

From the previous section it is clear that the behavior of a pulsed oscillator is determined by pairs of complex conjugate poles. Therefore, the following discussion is

[1] Ideally $\sigma_i = 0$, which means that there are no losses and the oscillation lasts forever.

limited to the case of a 2-pole system, which possibly can be part of a higher-order system. In the case of a dominant pole, the behavior around the pole frequency and also the impulse response are determined by the properties of this pole only. Similar to (6.1), a generic second-order transfer function is written as:

$$\begin{aligned} H(s) = \frac{P(s)}{Q(s)} &= \frac{a_1 \cdot s + a_0}{b_1 \cdot s^2 + b_1 \cdot s + b_0} \\ &= \frac{a_1/b_2 \cdot s + a_0/b_2}{s^2 + b_1/b_2 \cdot s + b_0/b_2} \\ &= \frac{a_1/b_2 \cdot s + a_0/b_2}{s^2 + \omega_n/Q \cdot s + \omega_n^2} \end{aligned} \tag{6.5}$$

where Q is the quality factor of the pole pair and ω_n the natural angular frequency of the tank (see also Sect. 2.5.1). In the case of an oscillation without losses or when all the losses are compensated by an amplifier, the tank oscillates very closely to its natural frequency, weakly depending on the zero in the numerator. Depending on the architecture or layout of the tank, a_1 or a_0 can equal zero, which means that the zero shifts to infinity or to DC. The poles of (6.5) are equal to:

$$\begin{aligned} c_1 &= \frac{-\omega_n}{2Q} + \frac{\omega_n\sqrt{1-4Q^2}}{2Q} \\ c_1^* &= \frac{-\omega_n}{2Q} - \frac{\omega_n\sqrt{1-4Q^2}}{2Q} \end{aligned} \tag{6.6}$$

The damping of the pole pair is inversely proportional to Q. To obtain oscillation (see Sect. 2.5.1), this means that Q must be larger than 0.5. Since an RC network can only exchange energy through a resistor as an exponential decay, Q is always lower than or equal to 0.5 and no oscillations will occur. RC tanks are therefore not usable to implement a pulsed oscillator.

6.3.2.1 LC Tanks

Since LC networks can have, at least in theory, an infinitely high Q-factor, these resonators are very suitable to build low-noise and low-power oscillators. Series as well as parallel LC networks can be used as a frequency-dependent or tuned network. In this chapter, the parallel network shown in Fig. 2.9c with a series resistor R_s in the inductor is discussed. The current to voltage transfer function of such network is (2.67):

$$Z_{eq} = H(s) = \frac{\frac{s}{C} + \frac{R_s}{L \cdot C}}{s^2 + \frac{R_s}{L} \cdot s + \frac{1}{L \cdot C}} = \frac{\omega_n \cdot \sqrt{\frac{L}{C}} \cdot s + \omega_n^2 \cdot R_s}{s^2 + \frac{\omega_n}{Q} \cdot s + \omega_n^2} \tag{6.7}$$

$$\text{where } Q = \sqrt{\frac{L}{C}} \cdot \frac{1}{R_s}$$
$$\text{and } \omega_n = 1/\sqrt{L \cdot C} \tag{6.8}$$

Splitting this function in partial fractions results in:

$$H(s) = \frac{1}{2} \cdot \frac{\omega_n R_s Q \left(1 + \frac{1}{\sqrt{1-4Q^2}}\right)}{s - \frac{-\omega_n(1-\sqrt{1-4Q^2})}{2Q}} + \frac{1}{2} \cdot \frac{\omega_n R_s Q \left(1 - \frac{1}{\sqrt{1-4Q^2}}\right)}{s - \frac{-\omega_n(1+\sqrt{1-4Q^2})}{2Q}} \tag{6.9}$$

Since this is a 2-pole system, the impulse response contains only one dominant angular frequency equal to:

$$\omega = \omega_n \cdot \sqrt{1 - \frac{1}{4 \cdot Q^2}} = \sqrt{\frac{1}{L \cdot C} - \frac{R_s^2}{4 \cdot L^2}} \tag{6.10}$$

The time constant of the amplitude decay is equal to:

$$\tau = \frac{2 \cdot Q}{\omega_n} = \frac{2 \cdot L}{R_s} \tag{6.11}$$

Note that the time constant is proportional to the oscillation period which means that the Q factor is a measure of the number of cycles it takes to half the amplitude. The higher Q, the slower the amplitude decay and the higher the number of free-running cycles can be in a pulsed-harmonic oscillator, which results in a lower power consumption. Bondwire inductors can reach a Q factor of 45, which corresponds to an amplitude decrease of a factor of 10 over 32 cycles.

6.3.2.2 Quartz Crystal Tanks

The behavior of a quartz crystal resembles that of the LC tank, although it is more complex due to the extra capacitor in parallel, according to the model of Fig. 6.4. Furthermore, the Q factor of a crystal is several orders of magnitude higher than that of an LC tank. The current-to-voltage transfer function of a crystal is given by:

$$Z(s) = H(s) = \frac{1}{sC_p} \cdot \frac{s^2 + \frac{R_s}{L} \cdot s + \frac{1}{LC_s}}{s^2 + \frac{R_s}{L} \cdot s + \frac{C_s + C_p}{LC_sC_p}} \tag{6.12}$$

Also in this system the order of the denominator is higher than that of the numerator. In this transfer function a pair of poles and a pair of zeros is distinguished. Both of them have a Q factor and a natural angular frequency, given by:

$$Q_s = \frac{1}{R_s} \cdot \sqrt{\frac{L}{C_s}} \tag{6.13}$$

$$\omega_s = \frac{1}{\sqrt{L \cdot C_s}} \tag{6.14}$$

$$Q_p = \frac{1}{R_s} \cdot \sqrt{\frac{L \cdot (C_s + C_p)}{C_s \cdot C_p}} \tag{6.15}$$

$$\omega_p = \sqrt{\frac{C_s + C_p}{L \cdot C_s \cdot C_p}} \tag{6.16}$$

Therefore, (6.12) can be rewritten as:

$$H(s) = \frac{1}{s \cdot C_p} \cdot \frac{s^2 + \frac{\omega_s}{Q_s} \cdot s + \omega_s^2}{s^2 + \frac{\omega_p}{Q_p} \cdot s + \omega_p^2} \tag{6.17}$$

Although Q_p is somewhat higher than Q_s in this model, a series oscillation is preferred. This is because the parallel capacitance C_p mainly depends on parasitics and in a design cannot be defined as accurately as the series capacitance C_s. The series resonance frequency ω_s only depends on the crystal parameters; ω_p also depends on the parasitics of the package [219].

Injecting energy in the tank by charging or discharging the parallel capacitor will result in a parallel resonance.[2] Due to the high Q factor of the tank, which can easily be 100–1000 times higher than for an LC tank, the number of free-running cycles between pulses can also be much higher. Unfortunately, however, C_p and C_s form a capacitive divider:

$$V_{out} = V_{tank} \cdot \frac{C_s}{C_s + C_p} \tag{6.18}$$

which results typically in a 200 times lower output swing than the total tank voltage. As shown in [219], increasing the size of the external parallel capacitors (to ground), pushes the oscillator frequency closer towards the series resonance frequency. However, this also decreases the output swing at the crystal terminals.

Another way to make use of the series oscillation in a pulsed oscillator, is eliminating the parallel capacitance by shorting the crystal terminals. To drive the oscillator, one has to make use of the voltage-to-current transfer function instead. The pulse applied to the tank is then a low-impedant voltage pulse, whereas, in the case of the LC tank, a current (or charge) pulse is injected. In between two pulses the tank must be shorted with an extremely low resistance in combination with a current

[2] Typically this is implemented by adding two grounded capacitors in series with the crystal. The correct value of these external parallel capacitors needed to obtain an accurate reference is in most cases provided by the manufacturer.

instead of a voltage output. A pulsed series crystal oscillator with a high Q factor seems therefore extremely difficult, even impossible, to implement.

Recently an ultra-low-power crystal oscillator was published, which injects a charge pulse in the external parallel capacitors every cycle [112].[3] This shows that a pulsed resonance is indeed feasible, however, several cycles (pulses) are needed to obtain a sufficiently high output swing at the tank's terminals. In [112] an extra feedback amplifier is used to overcome this difficulty during startup. Once the desired amplitude is reached, it is possible to reduce the number of pulses by interleaving them with some free-running cycles. While doing so, the limited impact of each pulse on the output swing needs to be taken into account when trying to retain a stable oscillation. Since the impact of each pulse decreases when the size of the parallel capacitor is increased, this will also increase the power consumption. In a low power application, the grounded parallel capacitors can best be small, which results in an oscillation close to the parallel resonance frequency.

To fully benefit from the high Q factor, it is necessary to directly access the dominant tank capacitor (C_s) as is the case in a pulsed LC tank. This capacitance is, however, only a model parameter! For this reason it is difficult to use quartz crystals in a 'sparsely' pulsed oscillator. Furthermore, a crystal cannot be integrated on chip, which results in an increased assembly cost. In the following sections the discussion focuses on pulsed LC oscillators without using a quartz crystal.

Although also MEMS resonators can be produced with an increasingly high Q factor, the use of a high-Q MEMS resonator is not discussed here. Note, however, that the circuit model of a MEMS resonator is often similar to that of a quartz crystal [120] (think for instance about a tuning fork quartz crystal). Using this model, the suitability of a MEMS resonator in a pulsed oscillator topology can be determined. The fact that in a microelectromechanical structure the driving electrodes can often be separated from the output contacts introduces an extra degree of freedom. This makes pulsed MEMS oscillators an interesting topic for future research.

6.4 Behavior of the Pulsed LC Oscillator

The behavior of a pulsed oscillator is determined by the tank and the pulses applied to the circuit. Since the tank is a linear network, the superposition principle can be applied. This means that, when perturbing the tank with a Dirac impulse at exactly the right moment every n cycles, it is possible to keep the instantaneous frequency of the oscillator constant. From (6.9) it follows that the impulse response of the LC tank is equal to:

[3] Note that this technique, apart from its different hardware, closely approaches the use of a class-C amplifier.

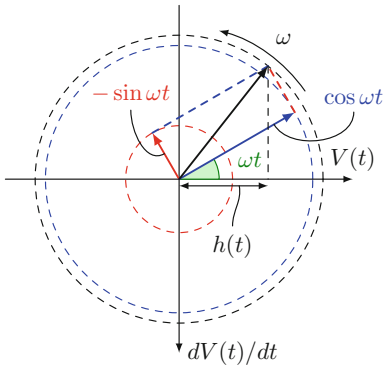

Fig. 6.6 Phasor diagram of the impulse response. To keep the period constant, a new Dirac impulse must be applied at the zero crossing of the cosine and *not* at the maximum of $h(t)$

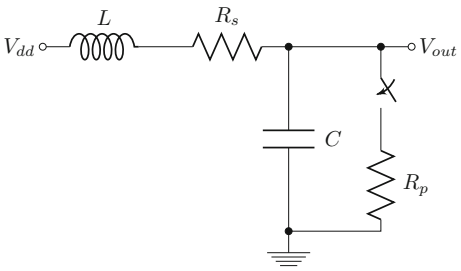

Fig. 6.7 Schematic model of the tank. This model is numerically simulated in Matlab; the switch is closed (*pulsed*) once every n cycles

$$h(t) = \omega_n R_s Q e^{\frac{-\omega_n}{2Q}t}\left[\cos\left(\frac{\sqrt{4Q^2-1}}{2Q}\omega_n t\right) - \frac{\sin\left(\frac{\sqrt{4Q^2-1}}{2Q}\omega_n t\right)}{\sqrt{4Q^2-1}}\right] \quad (6.19)$$

Since the resulting waveform is a sum of a cosine and a sine, the oscillation does not start at phase 0. The negative sine leads the cosine by $\pi/2$ and represents a small part of the impulse response. This is shown in Fig. 6.6. The timing of the applied pulses is crucial to avoid jitter in the output signal. Only when a pulse is applied exactly at the $n \cdot 2 \cdot \pi$ crossing of $\omega \cdot t$ (the zero-degree crossing of the cosine phasor), the output period stays constant. Only for $Q \gg 1$ this moment is equal to the zero crossing of the resulting output phasor or the maximum of the output voltage.

In a real system, instead of a Dirac impulse, pulses with a finite pulse width are applied. To simulate this, the RLC-tank was modeled in Matlab. A pulse is applied by connecting a resistor to discharge the tank capacitor once every n cycles.[4] The schematic is shown in Fig. 6.7. For a given tank, the pulses are determined by 3 parameters which can be controlled independently: the switch resistance R_p, the pulse width (PW) and the moment of impact (MoI), as defined in Fig. 6.8. Figure 6.9 shows the impact of the pulses at the moment of the zero crossings as a function of PW and MoI. Also the output amplitude is affected by these two parameters,

[4] n can be chosen depending on the properties and losses in the tank.

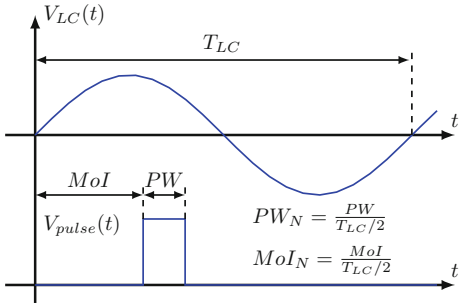

Fig. 6.8 Illustration of PW and MoI compared to the tank output waveform

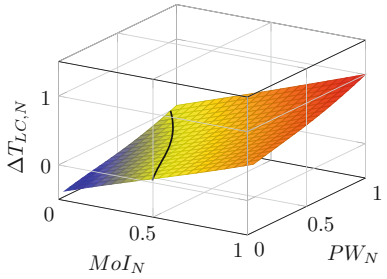

Fig. 6.9 Impact of a real pulse applied to the network of Fig. 6.7. When the right combination of pulse width (PW) and moment of impact (MoI) are applied (indicated by the *black line*), the time between the zero crossings is not biased. All the values are normalized to half the LC tank oscillation period

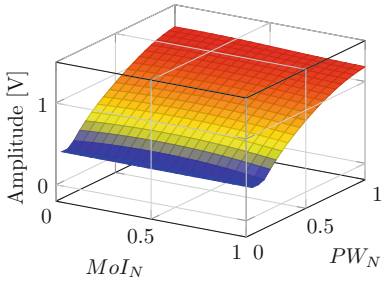

Fig. 6.10 Oscillation amplitude as a function of the pulse width (PW) and the moment of impact (MoI). A longer pulse leads to a higher amplitude, but also the moment of impact has a small influence on the output amplitude of the tank. All the values are normalized to half the LC tank oscillation period

as shown in Fig. 6.10. It is observed that by choosing the correct combination of PW and MoI, the timing of the zero crossings is not affected. Figure 6.11 shows these optimal combinations for different values of the switch resistance R_p. While designing the oscillator, the results of these simulations will be used since a zero-

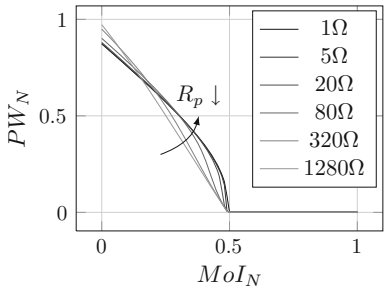

Fig. 6.11 Optimal width ($\Delta T = 0$) of the applied pulses (PW) as a function of the moment of impact (MoI) for different switch resistances R_p. Both axes are normalized to $T_{LC}/2$, half the LC tank oscillation period

impact operating point is preferred to avoid spurs in the output spectrum. Note that the case of infinitely short pulses (Dirac impulses, $PW = 0$) fits exactly with the simulation results of Fig. 6.9.

These results can also be obtained analytically, by solving the differential equation of the network for an open and a closed switch. Afterwards, the different regimes can be coupled by their start and stop conditions. The analytical solution to this, however, leads to complex and lengthy expressions, which makes using the numerical solution method much more straightforward and useful.

When simulating these curves for different values of R_s, the differences are negligible. For a high-Q resonator, the discharge of the capacitor is dominated by the $R_p \cdot C$ time constant. This was also expected from Fig. 6.6 and (6.19): the size of the sine component is small for a high-Q resonator. Note, however, that R_s has a small influence on the oscillation frequency itself. The number of free-running cycles and the supply voltage have no influence on the optimal PW-MoI combinations. This means that, while designing a pulsed LC oscillator, the pulse generator circuit can be designed independently of these parameters. The optimal combination of PW and MoI, both normalized to the oscillation period, is independent of the tank properties. This, however, only holds for a constant impedance of the switch, independent of the voltage V_{out}. Although for each transistor an optimal PW-MoI combination can be found, it is advisable to keep the switch in the linear region to benefit from the described independencies.

6.4.1 Sensitivity to PW and MoI

When designing the pulse generator, the sensitivity of the oscillation period to PW and MoI is important to keep in mind. This is simulated for the optimal PW-MoI combinations. Figures 6.12 and 6.13 show the sensitivity of the oscillation period to PW and MoI. Both graphs are normalized to half the oscillation period. It can clearly be seen that for a small series resistor of the switch, the impact of applying an inaccurate pulse is higher than for switches with a high series resistance. The oscillation period is somewhat less sensitive to PW than to MoI. These simulated

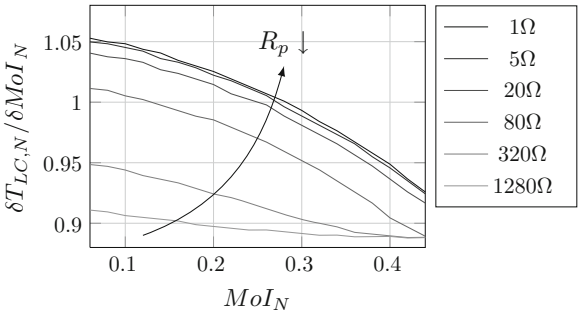

Fig. 6.12 Sensitivity of the oscillation period to the moment of impact. The derivative is calculated for the optimal PW-MoI combinations. All axes are normalized to half the oscillation period since this is the time span in which the pulse is applied

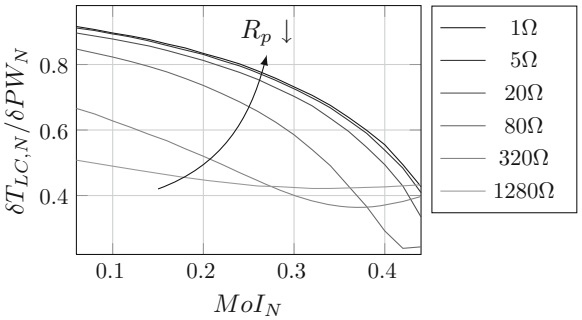

Fig. 6.13 Sensitivity of the oscillation period to the pulse width. The derivative is calculated for the optimal PW-MoI combinations. All axes are normalized to half the oscillation period since this is the time span in which the pulse is applied

sensitivities will be useful when estimating the impact of an inaccurate pulse due to changes in temperature or other external factors. It will be seen that these results correspond with the ISF, calculated in Sect. 6.5, and are therefore expected to be amplitude dependent.

6.4.1.1 Estimation of the Impact of Temperature and Supply Voltage Changes

The calculation of the impact of inaccurate applied pulses is rather straightforward. Since a complete oscillation period T_0 contains n free-running cycles and one cycle which is influenced by the pulse, one oscillation period can be written as:

$$T_0 = n \cdot T_{LC} + T_{LC} \cdot (1 + \Delta T_{LC,N}/2) \tag{6.20}$$

$$= (n+1) \cdot T_{LC} + T_{LC}/2 \cdot \frac{\Delta T_{LC}}{T_{LC}/2} \tag{6.21}$$

where T_0 is the pulse frequency, n is the number of free-running cycles and $\Delta T_{LC,N}$ is the relative deviation of the half LC tank period due to the applied pulse. When the sensitivities of the period to MoI and to PW are known, the relative impact of an inaccurate pulse on T_0 can be calculated as follows:

$$\frac{\Delta T_0}{T_0} = \frac{\frac{\delta T_{LC}}{\delta MoI} \cdot \Delta MoI + \frac{\delta T_{LC}}{\delta PW} \cdot \Delta PW}{(n+1) \cdot T_{LC}} \tag{6.22}$$

$$= \frac{\frac{\delta T_{LC,N}}{\delta MoI_N} \cdot \Delta MoI_N + \frac{\delta T_{LC,N}}{\delta PW_N} \cdot \Delta PW_N}{2 \cdot (n+1)} \tag{6.23}$$

where all the values with subscript N are normalized to half the LC tank period. From this equation it is clearly visible that the oscillation period suffers only weakly from inaccurate pulsing. From Fig. 6.9 one can conclude that this linear approach is a reasonable approximation, even for high values of ΔMoI_N and ΔPW_N. When, for instance, PW varies over temperature with 30 %, this has only an impact of around 0.5 % on the frequency in the case of 31 free-running cycles. A more detailed calculation of the expected temperature and supply voltage dependency is performed in Sect. 6.6.4, where the implemented circuit is discussed.

6.4.2 Energy Losses During Oscillation

One of the benefits of the pulsed topology is the reduced energy consumption. This reduction is partially caused by the reduced losses in the tank itself (due to the smaller average amplitude). As will be seen, however, this reduced amplitude also has a negative impact on the noise performance. The other part of the reduction is caused by the lack of a feedback amplifier with high gain-bandwidth to compensate for the losses in the LC tank, as needed in a commonly used differential LC topology. Note that this amplifier also has a (negative) impact on the noise performance.

6.4.2.1 Oscillation with a Constant Amplitude

When the amplitude of the oscillator is kept constant, the energy losses in the tank can be calculated using the first definition of the Q factor (2.56). The energy losses in the tank after N oscillation cycles can then easily be calculated, resulting in:

$$E_{Cte}(N) = N \cdot 2 \cdot \pi \cdot \frac{V_A^2 \cdot C}{2 \cdot Q} \tag{6.24}$$

wherein V_A is the voltage amplitude of the oscillation. To keep the amplitude of the oscillation constant, a transconductance amplifier g_m is required to cancel the inductor's series resistance R_s. The required gain G or g_m can be calculated (Chap. 2):

$$G = \frac{1}{Q} \cdot \sqrt{\frac{C}{L}} = \frac{C \cdot R_s}{L} \tag{6.25}$$

Obtaining this g_m turns out to consume a lot of power since a large bandwidth and therefore a large $V_{gs} - V_{th}$ is required [219]. Also note that in the proposed application, a low-frequency oscillator for use in an impulse UWB transmitter, the LC output clock must be divided to a low-frequency output anyway.

6.4.2.2 Oscillation with *N* Free-Running Cycles

In this case the amplitude of the oscillation will decay. Despite the changing amplitude, Eq. (6.19) shows that the angular frequency remains stable and is somewhat *higher* than in the case with constant amplitude (see Chap. 2).[5] The dissipated energy in the tank after N oscillation cycles is then calculated to be:

$$E_{Decay}(N) = \frac{V_A^2 \cdot C}{2} \left(1 - e^{\frac{-2\pi N}{Q\sqrt{1-1/4Q^2}}}\right) \tag{6.26}$$

$$\approx \frac{V_A^2 \cdot C}{2} \left(1 - e^{\frac{-2\pi N}{Q}}\right) \tag{6.27}$$

To first order, i.e. for a small N and a high Q, this expression is equal to expression (6.24). For high N, however, the power losses in the free-running tank decrease drastically as a result of the decreased amplitude. A high number of free-running cycles N is therefore preferable.

6.5 Phase Noise in the Pulsed LC Oscillator

To describe the phase noise behavior of the pulsed LC oscillator, a distinction must be made between the two phases in the oscillation cycle. The most easy part is the free-running phase, which is basically a decaying LC tank. The pulsed phase, however, is somewhat more difficult to describe. The results from the previous section are useful to predict the worst-case phase noise behavior.

6.5.1 Noise Injection During the Free-Running Period

The noise of the oscillator during the free-running period is closely related to that of a harmonic LC oscillator. The main difference is the decaying amplitude, which

[5] This is opposite to the conclusions that are drawn when using the parallel resistor tank model [212].

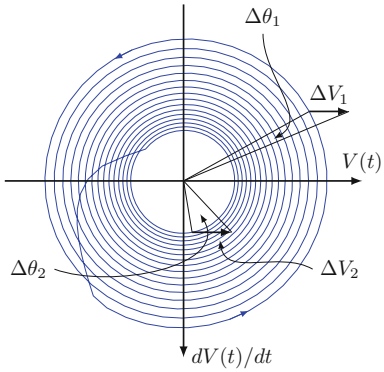

Fig. 6.14 Phase portrait of a pulsed oscillator. The LC network is similar to Fig. 6.7 with a switch discharging the state capacitor. An equal noise voltage ΔV is added at two different moments in the oscillation, causing a different phase shift $\Delta\theta$ in the output wave

has a significant influence. As explained in Sect. 3.4, oscillators can be described as a Linear Time-Variant (LTV) System [101, 151]. In Fig. 6.14 the phase portrait of a pulsed oscillator with 15 free-running cycles is shown. Similar to Fig. 3.4 an equal charge is injected at two different moments in the oscillator. This causes a ΔV over the capacitor, which is also equal in both cases ($\Delta V_1 = \Delta V_2$). The induced phase shift is, however, different in both cases: when the charge is injected around the maximum of the output voltage, a much smaller phase shift is caused than in the case of an injection at the zero crossing. Obviously, this is the same conclusion as in Sect. 6.4 about the injection of a Dirac impulse. As a result, the amplitude of the ISF is indeed expected to increase with the decaying amplitude.

As shown in Sect. 3.4, this ISF is used to calculate an impulse response for the excess phase (3.19). When several pulses or a noise spectrum is applied, the superposition integral (3.20) is used to calculate the total excess phase. Previously, the normalization factor q_{max} was defined as the maximum charge difference on the capacitor compared to the equilibrium state. For a finite pulse width PW, this can either be the minimum during the applied pulse or the first maximum after the pulse. To avoid any confusion, in the remainder of the text q_{max} is always assumed to be the charge difference at the first minimum. In the case this is not the real minimum, an extrapolated value of q_{max} is assumed to be used. This value can be calculated from the first maximum and the tank decay. In case of a Dirac impulse, the tank is pulsed almost exactly at this minimum.

A second difference with the strategy described in Sect. 3.4, is the normalization of the ISF. According to [101, 151] the ISF is normalized to a complete oscillation period T_0. Here, the response of the phase is normalized to T_{LC} instead. This results in exactly the same conclusions but simplifies the calculations.

6.5.1.1 Calculation of the ISF

The ISF of the oscillator during the free-running cycles can be calculated analytically. Since the LC tank is a second-order system, with 2 state variables, (3.46) can be used:

$$\Gamma_i(\omega t) = \frac{f'}{f'^2 + f''^2} \tag{3.46}$$

where the normalized capacitor voltage is the first state variable and its first derivative is the normalized current through the inductor, which is the second state variable. A detailed derivation of this formula is found in [101]. The normalized waveform [as defined by (2.35)] of the first state variable can be calculated starting from (6.19), typically $\omega_n \cdot t$ is substituted by x:

$$h_n(x) = e^{\frac{-1}{2Q}x}\left[\cos\left(\frac{\sqrt{4Q^2-1}}{2Q}x\right) - \frac{\sin\left(\frac{\sqrt{4Q^2-1}}{2Q}x\right)}{\sqrt{4Q^2-1}}\right] \tag{6.28}$$

$$\approx \frac{2Q \cdot e^{\frac{-1}{2Q}x}}{\sqrt{4Q^2-1}}\cos\left(\frac{\sqrt{4Q^2-1}}{2Q}x + \theta\right) \tag{6.29}$$

where, for high Q:

$$\theta \approx \tan(\theta) = \frac{1}{\sqrt{4Q^2-1}} \tag{6.30}$$

At $t = 0$ the maximum is reached and equal to 1. Starting from (6.29), the first derivative can be calculated as:

$$h_n'(x) = \frac{-1}{\sqrt{4Q^2-1}}e^{\frac{-x}{2Q}}\cos\left(\frac{\sqrt{4Q^2-1}}{2Q}x + \theta\right) - e^{\frac{-x}{2Q}}\sin\left(\frac{\sqrt{4Q^2-1}}{2Q}x + \theta\right) \tag{6.31}$$

$$\approx \frac{-2Q}{\sqrt{4Q^2-1}}e^{\frac{-x}{2Q}}\sin\left(\frac{\sqrt{4Q^2-1}}{2Q}x + 2\theta\right) \tag{6.32}$$

where the last step is using (6.30). Similarly, the second derivative can be calculated to be equal to:

$$h_n''(x) = \frac{1}{\sqrt{4Q^2-1}}e^{\frac{-x}{2Q}}\sin\left(\frac{\sqrt{4Q^2-1}}{2Q}x + 2\theta\right) - e^{\frac{-x}{2Q}}\cos\left(\frac{\sqrt{4Q^2-1}}{2Q}x + 2\theta\right) \tag{6.33}$$

$$\approx \frac{-2Q}{\sqrt{4Q^2-1}}e^{\frac{-x}{2Q}}\cos\left(\frac{\sqrt{4Q^2-1}}{2Q}x + 3\theta\right) \tag{6.34}$$

Squaring and adding both derivatives, leads to:

$$f'^2 + f''^2 \approx \frac{4Q^2}{4Q^2-1} e^{\frac{-x}{Q}} \sin^2\left(\frac{\sqrt{4Q^2-1}}{2Q}x + 2\theta\right) + \frac{4Q^2}{4Q^2-1} e^{\frac{-x}{Q}} \cos^2\left(\frac{\sqrt{4Q^2-1}}{2Q}x + 3\theta\right) \tag{6.35}$$

$$= e^{\frac{-x}{Q}}\left[\frac{2Q^2}{4Q^2-1} + \frac{2Q^2}{4Q^2-1} + \frac{4Q^2}{4Q^2-1}\cos\left(\frac{\sqrt{4Q^2-1}}{Q}x + 4\theta\right) - \frac{4Q^2}{4Q^2-1}\cos\left(\frac{\sqrt{4Q^2-1}}{Q}x + 6\theta\right)\right] \tag{6.36}$$

Using Simpson's formula, keeping in mind that $\sin(\theta) \approx \theta$ for small θ, this results in:

$$f'^2 + f''^2 \approx \frac{4Q^2}{4Q^2-1} e^{\frac{-x}{Q}}\left[1 - \frac{1}{\sqrt{4Q^2-1}}\sin\left(\frac{\sqrt{4Q^2-1}}{Q}x + 5\theta\right)\right] \tag{6.37}$$

Substituting (6.37) and (6.32) in (3.46), the ISF during the free-running period results in:

$$\Gamma(x) \approx \frac{-e^{\frac{x}{2Q}} \cdot \sin\left(\frac{\sqrt{4Q^2-1}}{2Q}x + 2\theta\right)}{\frac{2Q}{\sqrt{4Q^2-1}} - \frac{2Q}{4Q^2-1} \cdot \sin\left(\frac{\sqrt{4Q^2-1}}{Q}x + 5\theta\right)} \tag{6.38}$$

which is independent of the oscillation amplitude and the natural frequency. To get a complete picture of the ISF, this result needs to be combined with the impulse sensitivity during the moment of the applied pulse.

6.5.1.2 ISF of a Harmonic Oscillator

It is interesting to compare this ISF to that of a continuously driven harmonic oscillator. The calculation is rather straightforward. Since the normalized waveform is in the latter case equal to:

$$h_n(x) = \cos(x) \tag{6.39}$$

the ISF is calculated to be, using (3.46):

$$\Gamma(x) = -\sin(x) \tag{6.40}$$

It will be shown that this more symmetrical (regular) waveform leads to a better phase noise performance as a result of the lower rms value compared to the peak amplitude.

6.5.2 Noise Injection During the Applied Pulse

The calculation of the ISF during the applied pulse is not an easy task. Although the curve in the state diagram of Fig. 6.14 can be calculated exactly for a resistive switch, the result strongly depends on the boundary conditions, i.e. the exact value of the state variables at the starting and ending point of the applied pulse. Therefore, the numerical simulation method proposed in Sect. 3.4.3 is used.

6.5.2.1 Simulation of the ISF

The numerical Matlab model of Fig. 6.7 was used to simulate the ISF. It is interesting that a comparison can be made between the two calculation methods. Figure 6.15 shows the simulated ISF together with the previously calculated ISF during the free-running period. Also the output waveform of the tank is shown. Both calculation methods result in an almost identical waveform of the ISF. Furthermore, the ISF during the applied pulse is much smaller than the ISF during the free-running period. This is mainly caused by the small switch resistance which is in parallel with the tank during the applied pulse. During the free-running period noise is only injected by the series resistor of the inductor. An extra noise source is introduced during the pulse coming from the switch resistance. However, since the ISF is small during this applied pulse, this extra noise source is neglected. An exact calculation of the noise by the switch resistance makes the introduction of cyclostationary noise sources necessary, but it is, luckily, superfluous.

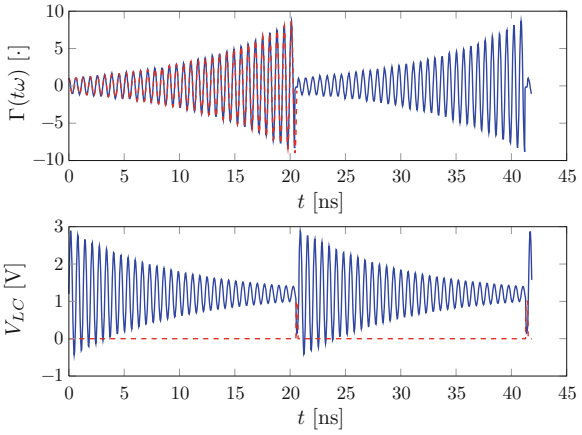

Fig. 6.15 *Top* The ISF of the pulsed oscillator. The *blue curve* is the numerically simulated ISF; the *red dashed curve* represents the analytically calculated ISF during the free-running period. Both curves are almost identical. *Bottom* The corresponding output waveform of the LC tank. The *red dashed line* shows the pulses applied to the LC tank

6.5.3 Impact of the Different Noise Sources

Using the ISF of the entire period, it is possible to calculate the resulting phase noise and jitter caused by the different noise sources. During the free-running period, two noise sources are identified: thermal noise from the tank and supply noise. Another strategy, based on the conclusions of the first section, is used to calculate the influence of the noise in the applied pulse caused by noise in the oscillator circuit.

6.5.3.1 Phase Noise in the Pulsed Oscillator

The jitter caused by the noise sources of the tank can now be calculated easily. Hajimiri and Lee [101] states that the noise in the $1/f^3$ region is caused by the up-conversion of the pink $1/f$ noise. The noise in the $1/f^2$ region around the carrier is an up-conversion of the white noise sources. The noise source in this case (the series resistance of the inductor) is a white noise source, therefore there is no $1/f^3$ contribution. The noise power spectral density of the series resistance is equal to:

$$\frac{\overline{v_n^2}}{\Delta f} = 4 \cdot k \cdot T \cdot R_s \tag{3.2}$$

where k is the Boltzmann constant and R_s is the series resistance of the inductor. The noise source is in series with the inductor L and the series resistance R_s (see Fig. 6.7). To estimate the impact of this noise source on the oscillator jitter, this source needs to be translated to a corresponding current source at the output node. This results in a current source with amplitude:

$$i_n = \frac{v_n}{R_s + s \cdot L} \tag{6.41}$$

This current noise source has a frequency dependency which makes the calculation of the resulting phase noise more complicated. However, as explained in [101], it is the noise around integer multiples of the oscillation frequency f_0 which is determining the phase noise. Therefore, the Fast Fourier Transform of the ISF is calculated and shown in Fig. 6.16. Since 31 free-running cycles are assumed in this calculation, the most important frequency component of the ISF is located at 32 times the oscillation frequency. It is therefore assumed that the noise at this frequency is dominant and determines the phase noise of the oscillator. Using (6.41), the noise power spectral density at the tank's oscillation frequency is equal to:

$$\frac{\overline{i_n^2}}{\Delta f} = \frac{4 \cdot k \cdot T \cdot R_s \cdot C}{L} \tag{6.42}$$

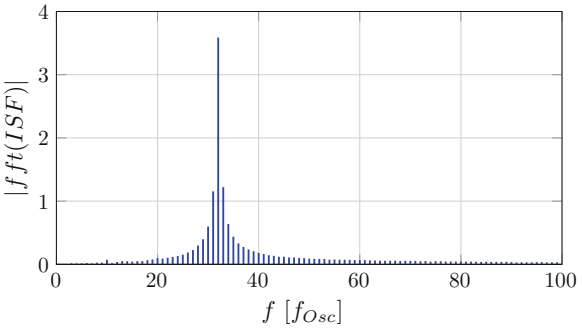

Fig. 6.16 Fast Fourier transform of the ISF. The most important frequency component is at $32 \cdot f_0 = f_{LC}$

Exactly the same result is obtained when using the equivalent parallel resistor R_p as a noise source instead of calculating the equivalent output noise of the series resistor R_s. The resulting phase noise can be calculated using (3.33), which makes use of the rms value of the ISF (calculated from the simulated waveform):

$$\Gamma_{rms} = 2.98 \tag{6.43}$$

From Fig. 6.7 it is seen that also the supply noise is in series with the inductor and has the same transfer function to the output. The properties of this noise source, its spectrum and amplitude, are unfortunately not known, which makes a proper estimation of its impact impossible. In the next section, based on the particular oscillator implementation, the resulting phase noise will be calculated.

6.5.3.2 Phase Noise in a Harmonic Oscillator

This result of the pulsed oscillator needs to be compared to the noise in a continuously driven oscillator. The amplitude is chosen in such a way that the average of the losses in the tank are the same as in the pulsed oscillator. Using (6.24) and (6.27) this makes:

$$\frac{q_{Cte}}{q_{Pulsed}} = \frac{V_{Cte}}{V_{Pulsed}} \tag{6.44}$$

$$= \sqrt{Q \cdot \frac{1 - e^{\frac{-2\pi N}{Q\sqrt{1-1/4Q^2}}}}{2 \cdot \pi \cdot N}} = 0.47 \tag{6.45}$$

when 31 free-running cycles are used. This means that, the amplitude of the harmonic oscillator is 2 times lower than in the case of a pulsed oscillator with the same tank losses. The numerical results of the resulting noise are found in the next section where the implementation details are discussed.

6.6 Implementation of the Pulsed LC Oscillator

In this section the results of the previous sections are applied to a real implementation of a pulsed-harmonic oscillator. The working principle of the pulsed oscillator was already briefly discussed in Sect. 6.2. Therefore, this section focuses on the remaining design choices.

6.6.1 Design of the LC Tank

From the previous sections it is clear that the Q factor is determining the damping in the LC tank. A high Q factor means that the losses in the tank are low, which reduces the energy dissipation and improves the noise behavior of the oscillator [see Eq. (6.38)]. As elaborately discussed in Sect. 4.2.4.2, integrated tanks suffer from different losses related to their integration close to or on top of a conducting silicon substrate. When a bondwire inductor is used instead, these effects are diminished slightly. As shown in Sect. 2.5.1, using a MiM-capacitor, the Q factor of the complete tank is dominated by the losses in the inductor:

$$Q = \sqrt{\frac{L}{C}} \cdot \frac{1}{R_s} \tag{2.60}$$

The Q factor of the tank can be increased by using a larger inductor and a smaller capacitor for the same natural angular frequency. The limit to the inductor size in integrated applications is often the available chip area. As shown in [285], the inductance and series resistance can be calculated by hand. However, finite-element simulations using FastHenry or other tools show results which are more accurate [124]. The resulting simulated inductance and series resistance of the bondwire inductor of $1{,}750 \times 1{,}500\,\mu\text{m}$, together with the tracks to the MiM capacitors at 1.54 GHz, are:

$$L = 30.4\ \text{nH} \tag{6.46}$$

$$R_s = 6.48\ \Omega \tag{6.47}$$

Connected to a total capacitance of 351 fF (MiM capacitor and parasitics), this leads to a Q factor and natural frequency of:

$$Q = 45.4 \tag{6.48}$$

$$\omega_n = 9.651\ \text{Grad/s} = 2 \cdot \pi \cdot 1.54\ \text{GHz} \tag{6.49}$$

In these simulations, the influence of a $300\,\mu\text{m}$ thick, highly-doped substrate is taken into account. This is expected to be an overestimation of the real substrate losses since typically only the top layer of a wafer is heavily doped. Note, however,

that in the case of large bondwire inductors, the parasitic capacitance is not negligible. This results in extra losses and lowers the self-resonance frequency of the inductor. Therefore, during measurements, different L-C configurations were tested. Decreasing the inductor size, has only a minor impact on the Q factor but increases the power consumption due to the increased tank capacitor.

6.6.1.1 Resulting Noise During the Free-Running Period

For $V_{dd} = 1.6$ V (which is the maximum applied supply voltage), the maximum charge in the tank is equal to:

$$q_{max} = V_{dd} \cdot C = 5.62e{-}13 \text{ C} \tag{6.50}$$

$$k = 1.38e{-}23 \text{ m}^2 \text{ kg/s}^2\text{/K} \tag{6.51}$$

At room temperature the estimated phase noise close to the carrier frequency is then equal to:

$$\mathscr{L}\{\Delta\omega\}_{dB} = 10 \cdot \log\left(\frac{17.44}{\Delta\omega^2}\right) \tag{6.52}$$

To translate this to the jitter on the oscillator output signal, (3.63) can be used:

$$\sigma_{LC} = \sqrt{\frac{\Delta f^2 \cdot \mathcal{L}\{\Delta f\}}{f_0^3}} = 1.10e{-}14 \text{ s} = 11.0 \text{ fs} \tag{6.53}$$

The ISF was normalized to T_{LC} instead of T_0. Therefore, to obtain the jitter on the total oscillation period (which contains 32 tank cycles), the standard deviation needs to be multiplied by $\sqrt{32}$, resulting in:

$$\sigma_c = 6.22e{-}14 \text{ s} = 62.2 \text{ fs} \tag{6.54}$$

6.6.1.2 Resulting Noise in a Harmonic Oscillator

The maximum charge in the circuit is, according to (6.45) and (6.50), equal to $2.65e{-}13$ C. Since the tank itself is the same in both cases, the injected noise current is also assumed to be the same. Using (3.33) and (3.63), this results in a tank jitter of:

$$\sigma_{LC,Cte} = 5.52e\text{-}15 \text{ s} = 5.5 \text{ fs} \tag{6.55}$$

Although the maximum charge in the tank is a factor of two lower than in the case of the pulsed tank, the jitter is also much lower. This is caused by the irregular waveform of the ISF of the pulsed oscillator, which results in a higher rms value and therefore also a higher noise sensitivity. In [6] it is shown that in a well-designed oscillator

the noise added by the active devices is of the same order of magnitude. Due to the high-Q tank, a good noise performance is therefore expected. Also note that when using the tank differentially (as mostly done), the size of the tank is divided by two. This, however, leads to similar conclusions.

6.6.2 Design of the Differential Amplifier

The smaller the signals the amplifier can detect, the more oscillation periods the tank can be free-running. The chosen topology for the amplifier is a differential pair in combination with two differentially biased CMOS inverters. This topology results in a low power consumption and a stable DC biasing of the first stage in combination with a high gain of the two inverters. The schematic of the amplifier is shown in Fig. 6.17. Since the input signal of the amplifier is not differential, an extra capacitor C_c connects the source of the differential transistors to the ground. In this way the gain is large at high frequencies without losing the self-biasing benefits of a differential pair at DC. The two CMOS inverters are used to amplify the waveform to a (digital) clock signal. As will be seen this signal does not have to be rail to rail in order to trigger the clock input of the TSPC flip-flops, which also reduces the power consumption drastically. To make the behavior of the amplifier independent of the supply voltage, the biasing circuit shown on the left-hand side of Fig. 6.17 is used. This circuit keeps the current through the differential pair constant at different supply voltages [188, 219]. The resistor in this network is connected to a bondpath in order to be able to adapt the current externally. In Fig. 6.18 the delay and peak-to-peak output signal is shown as a function of the input amplitude. For a falling edge at the input (to trigger the counter), the delay increases because the first stage slews. Rising edges cause a quick discharge of the first stage's output into C_c, which increases the speed of

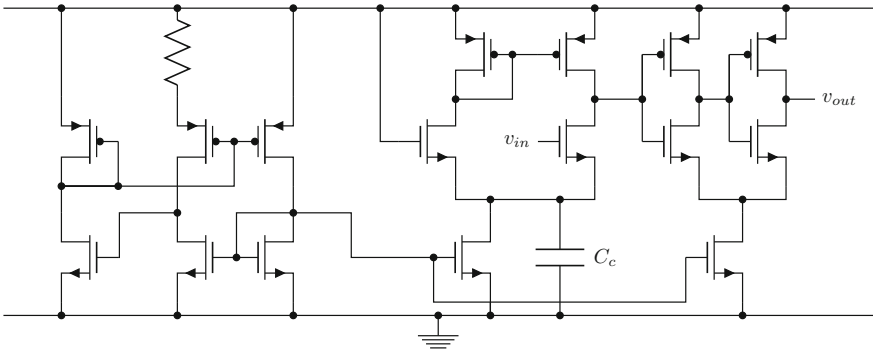

Fig. 6.17 The amplifier used to detect the LC output signal is a differential pair in combination with 2 differentially biased CMOS inverters. The differential pair is shown (*right*) together with the supply-independent biasing circuit (*left*) [188]

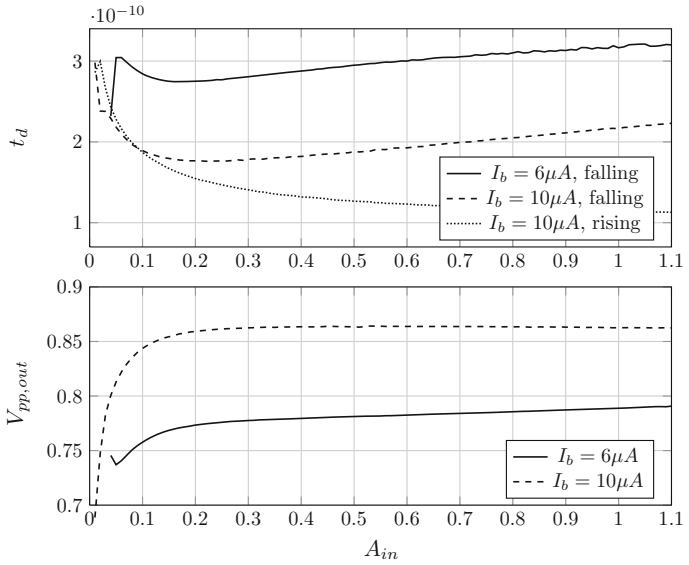

Fig. 6.18 Delay and peak-to-peak output signal of the amplifier for different input amplitudes at $V_{dd} = 1.1$ V and for a falling and a rising edge at the input. The circuit is able to detect a 10 mV signal when the biasing current is 10 µA. When the current is decreased, the sensitivity also decreases

the critical path (see Sect. 6.6.4.1). This, however, has no impact at low amplitudes, when the tank is pulsed. A last measure to decrease the power consumption is by reducing the left side of the differential pair. The total current consumption of the amplifier is then around 10 µA, while a 30 mV tank amplitude can be detected (10 mV for a 16 µA amplifier), be it at the cost of an increased noise sensitivity.

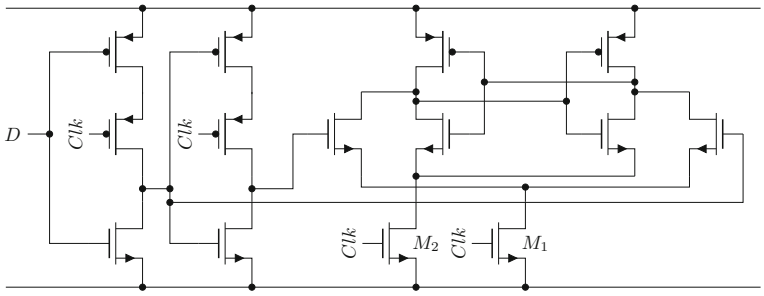

Fig. 6.19 The ripple counter is built out of 5 modified TSPC flip-flops

6.6.3 The Counter

The ripple counter is built out of 5 modified TSPC flip-flops. The schematic of the used flip-flop is shown in Fig. 6.19. The steepness of the applied clock edge to the flip-flop is crucial to prevent it from data loss or ripple-through. This, however, does not pose any problem using the steep edges of the 1.5 GHz tank output. Different measures were taken to reduce the power consumption of the counter. One of them is the addition of a current source at the ground node, which limits the current at high supply voltages. Furthermore, due to the resulting ground lift, the clock at the input does not need to be rail-to-rail. The resulting power consumption of the counter is below 10 μW at 1.1 V.

6.6.4 The Pulse Generator

As shown previously, the PW as well as the MoI have an influence on the zero crossings of the LC-tank's output voltage. The delay to control the PW of the pulse generator is controlled by a chain of differentially biased inverters and a capacitor at the output of the first inverter. This is shown in Fig. 6.20. The combination of inverters is very similar to the structure of the previously discussed amplifier. The use of current sources allows the pulse generator to be switched off most of the time and makes the PW stable under a changing supply voltage and temperature. The biasing circuit shown in Fig. 6.17 is shared between the inverters and the differential amplifier. Due to process variations, it is difficult to predict the precise series resistance of the NMOS switch which has to discharge the tank's capacitor. Therefore the capacitor is sized to generate a pulse of 30 % of the oscillation period. From Fig. 6.11 it appears that at this PW the curves of optimal MoI-PW combinations for different switch resistances cross each other. Furthermore, from Figs. 6.12 and 6.13 the sensitivity for both the MoI and the PW are rather constant and therefore have no important impact on the chosen PW. This PW is long enough to discharge the capacitor sufficiently and to result in a maximum amplitude close to the supply voltage (see Fig. 6.10).

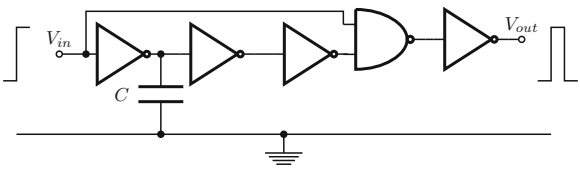

Fig. 6.20 The pulse width of the pulse generator is controlled by the inverter delay in combination with the output capacitor

6.6.4.1 The Influence of Inaccurate Pulses

For the implemented 1.54 GHz tank, the desired optimal PW is around 195 ps. This value corresponds to a MoI of 81 ps after the zero crossing of the tank output signal. Unfortunately, in the used technology (130 nm CMOS), keeping the critical path between the tank and the output of the pulse generator lower than 100 ps is a real challenge. According to [106], in 130 nm CMOS, inverter delays are in the order of magnitude of 20–30 ps. Simulations of an inverter chain using standard-V_{th} transistors in the used technology at the nominal supply voltage of 1.2 V, show a minimum delay of 16.5 and 12.41 ps for a falling and rising input edge respectively (t_{lh} and t_{hl}). At 0.6 V the very same inverter chain has a unit delay of around 50 ps.[6] Therefore, the pulse generator is not triggered by the falling edge, but by the preceding rising edge of the tank's output signal. In this way, the total delay of the critical path is designed to be 414 ps. This, of course, has a significant drawback on the accuracy of the MoI: temperature and voltage variations have a constant relative impact on the delay of the critical path. In absolute numbers, this has a 5 times higher impact on the MoI than in the case the pulse was triggered by the corresponding falling edge!

Circuit simulations were performed to estimate the variation of PW and MoI over temperature and supply voltage. From Figs. 6.12 and 6.13, the worst-case relative sensitivities of MoI and PW are estimated to be 1.02 and 0.8 respectively. These simulation results due to temperature variations are shown in Fig. 6.21 together with the impact on the pulsed period. Similar simulations were performed to estimate the impact of the supply voltage, with a constant biasing current. From Eq. (6.23) $\Delta T_{LC,N}$ must be divided by two times the number of free-running cycles to obtain the temperature and supply voltage sensitivity of T_0:

$$T_{Sens} = 43.6 \text{ ppm/°C} \tag{6.56}$$

$$V_{Sens} = 59.2 \text{ ppm/V} \tag{6.57}$$

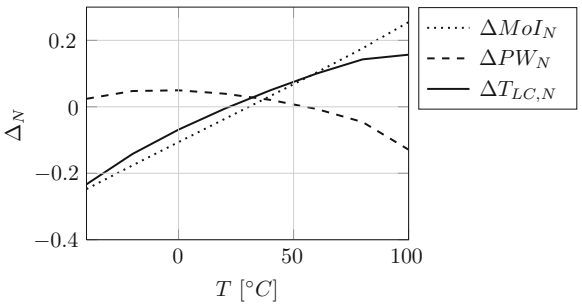

Fig. 6.21 Impact of the changing temperature on the output PW and MoI. The combined impact on the pulsed period is also shown

[6] Similar simulations in a 40 nm CMOS technology at a 0.9 V supply voltage result in a stage delay of $t_{lh} = 5.34$ ps and $t_{hl} = 1.43$ ps, which makes a 100 ps delay of the critical path perfectly feasible.

Note that this deviation in both cases is mainly determined by the variation of the MoI which is much higher than the variation of the PW.

6.6.4.2 Noise in the Pulse Generator

To calculate the noise on the injected pulses, transient noise simulations were performed. The noise in the pulse generator but also the noise generated in the amplifier have an influence on the MoI and/or the PW. Therefore, both circuits were connected, with an ideal sine wave at the input, which simulates the tank's output signal. The variation on MoI as well as PW were monitored over 10,000 noise samples. First of all, it is important to note that the noise on both output variables is uncorrelated. When taking a closer look at the pulse generator topology, this can be expected indeed. When the output values of the PW and the MoI are analyzed, both values have a normal distribution. Using again the worst-case sensitivities of the MoI and the PW (Eq. (6.23)) the relative standard deviation on the zero crossing of the pulsed T_{LC} and on T_0 is calculated to be:

$$\sigma_{LC,Pulsed,N} = 0.0069 \tag{6.58}$$

$$\sigma_0/T_0 = 1.08 \times 10^{-4} \tag{6.59}$$

$$\sigma_0 = 2.15 \times 10^{-12}\ \text{s} \tag{6.60}$$

These values clearly show that the noise in the pulse generator is dominant compared to the tank noise. Although the ISF during the applied pulse is very low, the inaccurate pulses have a serious impact on the noise performance. This can be understood by noting that a different PW also changes the ISF. The extra charge which is injected during a longer pulse, must in fact be convolved with the ISF right after the applied pulse (3.20). When simulating the jitter of the complete oscillator (including biasing circuitry, etc.), similar figures are obtained: $3.60e{-}12$ s for the applied pulses and $4.14e{-}12$ s at the low-frequency output of the counter, which is *not* in the critical path. However, as a result of the single-ended structure of the implemented oscillator, the circuitry is vulnerable to supply noise, which will be discussed in the next section.

6.7 Measurement Results

The key measured properties of the oscillator are listed in Table 6.1. A chip photomicrograph is shown in Fig. 6.22. The large chip area is an important drawback of bondwire inductors. However, as can be seen on the chip photograph, other circuitry can be laid out under the inductor. Furthermore, at higher frequencies, this technique can also be implemented with high-Q monolithic inductors. Figures 6.23 and 6.24 show the measured output frequency as a function of the temperature and the supply voltage respectively. Both the measured temperature and supply voltage sensitivity

Table 6.1 Overview of the measured key properties (12 samples)

Technology	130 nm CMOS
Area	1,750 µm by 1,500 µm
Power consumption at 1.1 V	46 µW
Max. temp. coefficient (−40–100 °C)	92 ppm/°C
Max. voltage coefficient (0.6–1.6 V)	74 ppm/V
Frequency	47.3 MHz
Abs. accuracy (σ, automatically bonded)	0.76 % (359 KHz)

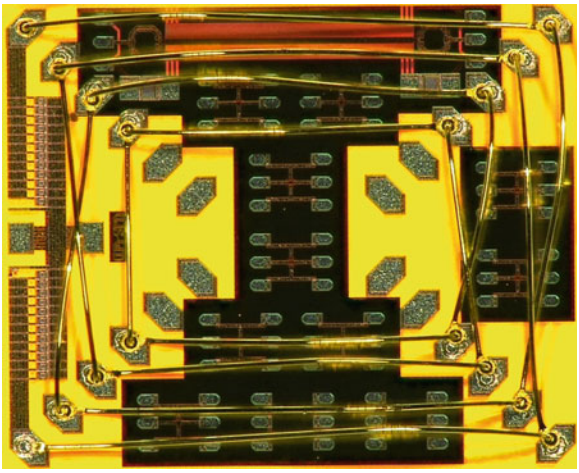

Fig. 6.22 Photomicrograph of a pulsed LC oscillator. Some other unrelated test circuitry is laid out under the inductor. The chip area is 1,750 µm by 1,500 µm

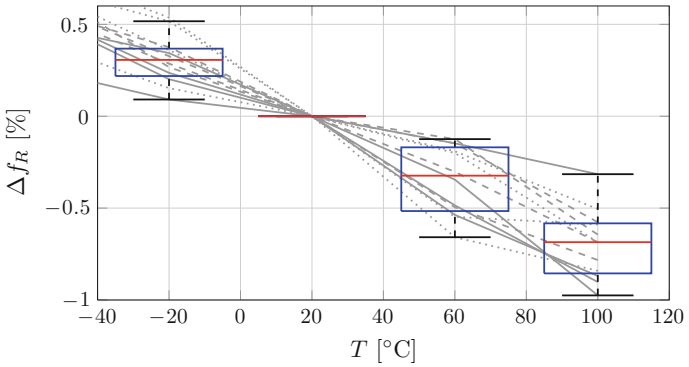

Fig. 6.23 Measured relative frequency error of the twelve measured samples. As predicted in Sect. 6.6.4.1, the frequency drops with increasing temperature

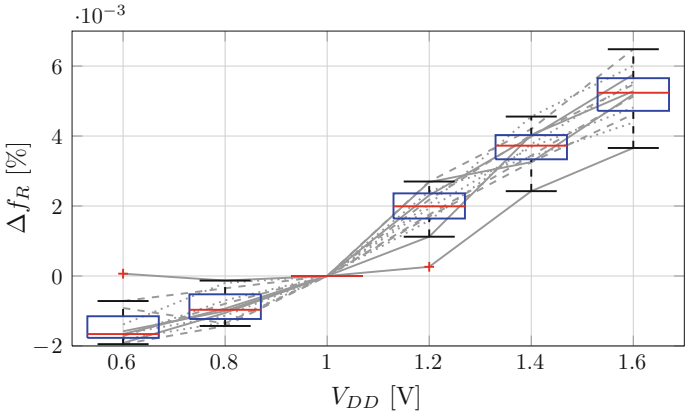

Fig. 6.24 Measured relative frequency error over different supply voltages of the twelve samples

are similar to the predictions of Sect. 6.6.4.1. The difference between measurements and simulations are likely caused by the fact that no temperature dependency was modeled in the inductor. Due to the parasitic capacitance of the inductor, the Q factor is lower as predicted. A reduction of the freerunning cycles is therefore required to improve the robustness of the circuit. When the number of free-running cycles is lowered, lower supply voltages and biasing currents can be used, reducing the power consumption. This, however, has a negative impact on the temperature and voltage behavior. The minimum measured power consumption at 1.1 V is equal to 46 µW.

Using (6.27) the power losses in the tank are estimated to be 10 µW. Almost the same amount of energy is lost in the NMOS switch. The remaining 26 µW at 1.1 V is consumed in the oscillator circuit. The power consumption of the circuitry increases almost linearly up to 79 µW at 1.6 V. Due to the amplitude dependence of the amplifier delay, the duty cycle of the different outputs of the counter is not equal to 0.5 and is slightly beating in some outputs. This causes spurs in the spectrum of the higher frequency outputs.

The measured output jitter is 12–15 times higher than the simulated value. In Fig. 6.25 the histogram of the measured output jitter is shown. The two peaks are most likely caused by supply and/or substrate coupling of the unused (but switching) sixth bit of the counter and its output buffers. This extra bit is present in this prototype for testing reasons. This switching noise can also be propagated through the lifted ground node of the ripple counter. Simulation results with and without this coupling are also shown in Fig. 6.25 and fit quite well with the measurements. The estimated phase noise FoM is 142.7 dB [using (3.63)]. It is therefore assumed that supply coupling is the main reason for the decreased noise performance. When looking at only the odd periods, the effects of the supply coupling are (partially) canceled out and a more correct estimate of the random cycle-to-cycle jitter is obtained. This is also shown in Fig. 6.25 and results in a 6 dB increase of the estimated phase noise FoM. The random effects result in a phase noise spectrum (side lobs); the

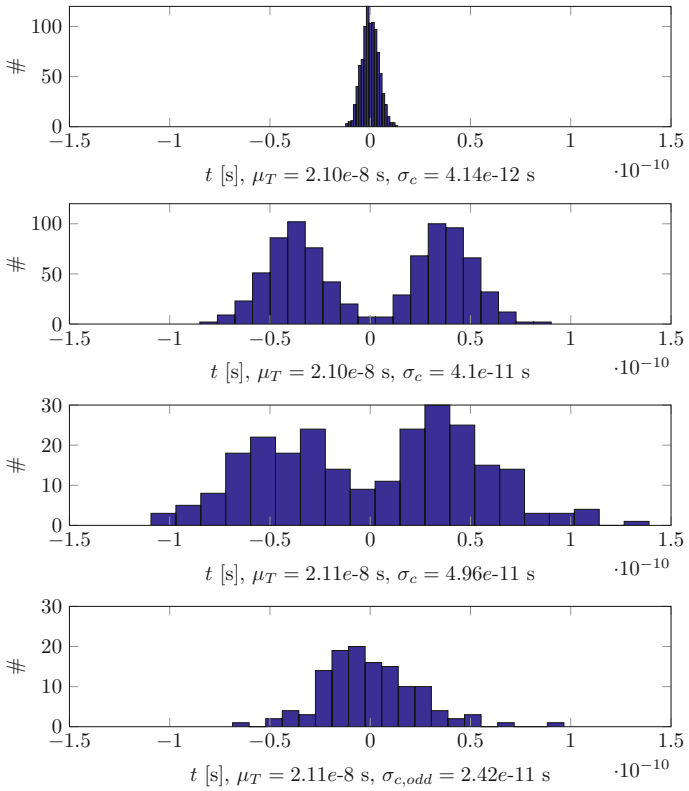

Fig. 6.25 Output jitter of the oscillator. The *upper plot* shows the simulated jitter, without supply noise. In the *second plot*, supply noise is added to simulate the noise injection of the digital circuitry as well as thermal noise to match the measured output jitter, which is shown in the *third plot*. The last plot shows the jitter on only the odd periods, since this is a more correct representation of the random (accumulated) noise in the system

deterministic jitter results in spurs. An extensive supply decoupling and/or a more optimized differential structure are needed to overcome this artifact. A comparison to the state of the art is shown in Table 6.2. Only the LC oscillator presented in [178] has a better temperature and supply voltage behavior, be it at the cost of a higher power consumption. The proposed pulsed topology is a stable, low-power oscillator alternative that can be used over a wide voltage and temperature range.

Table 6.2 Comparison of the oscillator to the state of the art

Ref.	Tech. (µm)	Oscillator	f (MHz)	T sens. (ppm/°C)	V sens. (ppm/V)	P (µW)	V-range (V)	Rel. V-range (%)[a]	Trimming/ calibration	Area (core) (mm^2)
This work	0.13	Pulsed-harmonic	47.3	92	74	46	0.6–1.6	91	No	2.63 (2.63)
[178], JSSC07	0.35	Harmonic, LC	12	12	38	31 mW	4.5–5.5	20	Yes	(0.22)
[55], ESSCIRC09	0.13	Harmonic, RC	24	–	104	33	0.4–1.4	111	No	(0.03)
[54], JSSC09	65 nm	Harmonic, RC	6	86	–	66	1.08–1.32	20	No	(0.03)
[250], ISSCC09	0.18	Relaxation, RC	14	107	16e3	43	1.7–1.9	22	No	(0.04)
[192], SBCCI03	0.5	Relaxation, RC	12.8	625	5.3e3	>400	2.5–5.5	**75**	Yes	(0.18)
[244], JSSC06	0.25	Ring	7	400	8.8*e*3	1.5 mW	$2.4 - 2.75$	14	No	1.6

[a] $\Delta V_{rel} = 2 \cdot (V_{max} - V_{min})/(V_{max} + V_{min}) \cdot 100\,\%$

6.8 Conclusion

A novel pulsed oscillator topology based on an LC tank has been analyzed in this chapter. Due to the high-Q LC tank and the pulsed driving technique, a low-frequency oscillator has been obtained with a low power consumption compared to other integrated LC oscillators. Furthermore, a low supply voltage dependency of 74 ppm/V and a temperature dependency of 92 ppm/°C were measured over a wide supply and temperature range. These measured properties lie within the target specifications in Table 1.1. The impact of the oscillator circuit on the frequency stability and the output noise has been discussed elaborately. It has been shown that the irregular pulsed waveform results in an increase of the noise sensitivity. The intrinsic noise of the oscillator is dominated by the pulse generator. However, in this single-ended implementation, it is the supply noise which seriously degrades the performance. This can drastically be improved using a differential structure and/or a better supply decoupling. A possible improvement is to connect the tank capacitor to the supply rail instead of the ground node. This, however, makes a startup circuit necessary, while the presented oscillator starts when switching on the supply voltage.

A possible drawback of bondwire inductors is mechanical resonance of the bondwires as a result of electric fields and/or mechanical vibrations. This effect, which can cause higher-order noise in the output spectrum (see Sect. 4.2.4 and 3.3), was, however, not observed during the measurements. Another drawback is the large chip area needed for the high-Q bondwire inductor. Since the Q factor is proportional to the oscillation frequency, in high-frequency applications both drawbacks can be addressed by using monolithic inductors instead. The use of high-Q MEMS resonators is possibly also a more robust and cost-efficient solution at lower frequencies. The power consumption of the presented implementation at 1.1 V is 46 μW, which makes the presented pulsed oscillator suited for applications such as autonomous sensor networks, requiring a low-frequency, low-energy and PVT-independent oscillator.

Chapter 7
Injection-Locked Oscillators

The first person to notice the phenomenon of injection locking was Christiaan Huygens, the inventor of the pendulum clock [213, 232]. *He was surprised to notice that different pendulum clocks attached to the same wooden beam are running perfectly synchronously. Obviously, these pulling effects between clocks are not limited to mechanical clocks. Electrical oscillators also influence each other, and even the generation of a laser beam can be injection-locked to an accurate reference laser. In literature, also many biological locking phenomena are reported, going from pulsing fireflies to our locking to the day and night rhythm* [189].

7.1 Introduction

In the previous chapters, different autonomous (free-running) time references have been presented. All of them are designed to withstand temperature and/or supply voltage variations. Also in literature, different autonomous solutions are available (Chap. 4). It has, however, been observed that the proposed free-running solutions have drawbacks going from a high power consumption to integration issues. Furthermore, in applications where wireless communication is needed, the delivered accuracy is often insufficient. An example of such communication is pulsed ultra-wideband (UWB), where pulses need to be transmitted at an accurate frequency [271] (detailed target specifications are summarized in Table 1.1). To overcome this, some solutions make use of extra synchronization pulses [39]. However, this goes together with an increased power consumption at both the transmitter and the receiver side [274]. In this chapter a different synchronization technique is presented, based on injection locking. Two implementations are discussed. The first non-coordinated implementation locks to a wirelessly injected carrier frequency. In the second implementation, which locks to an AM-modulated signal instead, also a receiver is added to facilitate network coordination. This receiver can be used to avoid collisions between data bursts of different nodes in the network.

V. De Smedt et al., *Temperature- and Supply Voltage-Independent Time References for Wireless Sensor Networks*, Analog Circuits and Signal Processing 128,
DOI 10.1007/978-3-319-09003-0_7

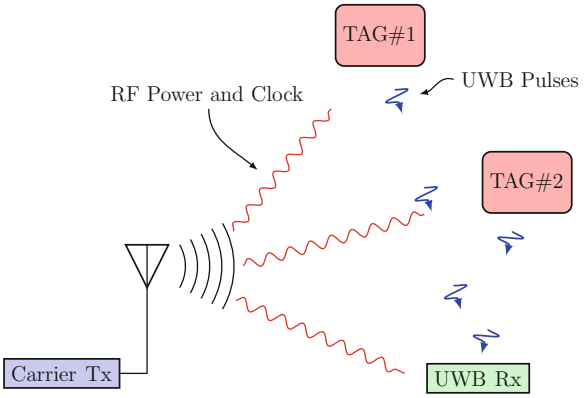

Fig. 7.1 System overview of the wireless sensor network (*WSN*) with RF clock distribution. The specifications of the clock carrier in terms of temperature and supply voltage stability are unimportant as long as the different network components can lock to the carrier

Both topologies start from a low-Q RC oscillator. For energy reasons, injection locking was used instead of a high-frequency input amplifier and phase-locked loop (PLL). As can be seen in the system overview of Fig. 7.1, the UWB transmitter in the tags as well as the UWB receiver can lock to the RF carrier. In this way, any frequency offset between both nodes can be reduced to zero. As a result, in the UWB uplink, the preamble is only needed to detect the initial phase offset and can be shortened drastically. This reduces the power consumption at both the transmitter and the receiver side. In the case of RF-powered tags, the system can use the same signal for power and clock distribution [52].

This chapter is organized as follows. In Sect. 7.2, the basic principles of injection locking and the expected lock range are discussed. In order to better understand the working principle of the receiver, also the dynamic behavior of the pull-in process is discussed. In Sect. 7.3 the influence of the injected signal on the oscillator noise is figured out. The first injection-locked time reference is discussed in Sect. 7.4. After that, in Sect. 7.4.2, the use of a phase detector to increase the lock range and to detect a lock is discussed. In Sect. 7.4.3, the measurement results of the 130 nm test chip are presented. The 40 nm implementation is presented in Sect. 7.5. The receiver, which is part of the 40 nm implementation is presented in Sect. 7.5.2. Afterwards, in Sect. 7.5.3 the measurement and simulation results of both the oscillator and the receiver are discussed. Finally, in Sect. 7.6, conclusions are drawn.

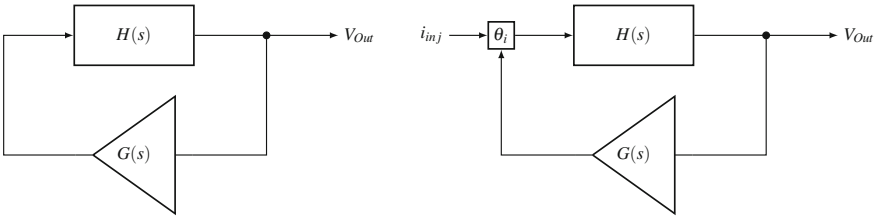

Fig. 7.2 Generic model of an oscillator, $H(s)$ is the tuned feedback network and $G(s)$ represents the amplifier. When a small current i_{inj} is injected, a phase shift is caused at the input of the feedback network

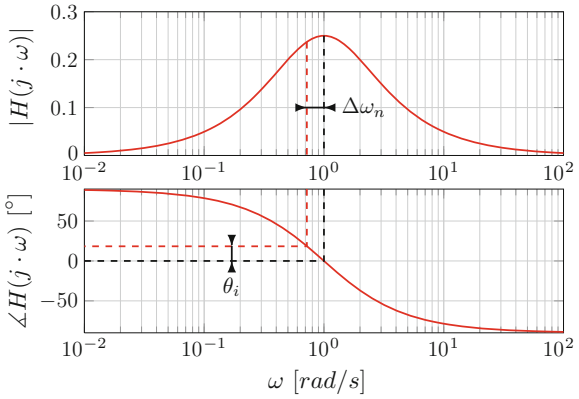

Fig. 7.3 Amplitude and phase of the generic transfer function of the oscillator. The angular frequency is normalized to ω_n and the amplifier needs a gain of 4 to obtain a stable oscillation. A frequency shift causes a nonzero phase shift in the feedback network

7.2 Injection Locking of an Oscillator

To examine the behavior of an injection-locked oscillator, a generic oscillator model is shown in Fig. 7.2. When a small current i_{inj} with an amplitude A_{inj} and an angular frequency ω_i, which slightly differs from the natural frequency ω_n, is injected at the input of the feedback network, the oscillator locks to this injected signal. However, as can be seen in Fig. 7.3, this leads to a non-zero phase shift caused by the feedback network. This phase shift must be compensated by the injected current to fulfill the Barkhausen criterion. This is indicated by the θ_i block in Fig. 7.2.

7.2.1 Lock Range of the Oscillator

The lock range of an injection-locked oscillator depends on different parameters. Apart from the amplitude of the injected signal, also the oscillator topology plays an important role. Two classes of oscillators can be distinguished, harmonic and

relaxation oscillators. Although a linear approach is taken to determine the lock range of the oscillator, note that injection locking can only occur in a (slightly) nonlinear system [213].[1]

7.2.1.1 Lock Range of a Harmonic Oscillator

On the phasor diagram in Fig. 7.4, it can be seen that in order to introduce a phase shift, the injected current must be out of phase with the transistor current. When the introduced phase shift is positive, the oscillator current leads the injected current and $\omega_n > \omega_i$.[2] From Fig. 7.4 it can easily be shown that:

$$\frac{\sin\theta_i}{A_{inj}} = \frac{\sin(180^\circ - \phi_i)}{A_r} = \frac{\sin\phi_i}{A_r} \tag{7.1}$$

where A_{inj} and A_r are the amplitude of the injected current and of the resulting current respectively. The resulting current A_r can be substituted, which results in:

$$\sin\theta_i = \frac{A_{inj}\cdot\sin\phi_i}{\sqrt{A_{osc}^2 + A_{inj}^2 + 2\cdot A_{inj}\cdot A_{osc}\cdot\cos\phi_i}} \tag{7.2}$$

The introduced phase shift θ_i reaches a maximum when the angle between i_{inj} and i_r is equal to 90°. This corresponds to $\sin(\theta_i)_{\max} = A_{inj}/A_{osc}$. When taking the sign of the phasor i_{inj} into account, note that a positive angle ϕ_i results in a negative induced phase shift and vice versa (a factor -1 needs to be added). To calculate the lock range of the oscillator for a given injected current, the definition of the Q factor based on the phase shift is used (2.69). For small injected currents, the lock range is small compared to ω_n. When looking at Fig. 7.3, it is clear that the phase shift of the feedback network can be linearly approximated by:

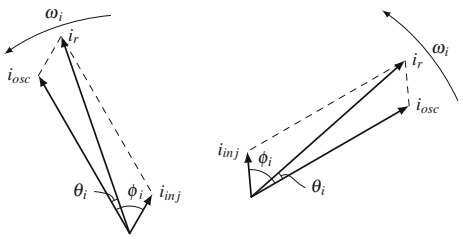

Fig. 7.4 Phasor diagram of the different currents in locked condition. *On the left*, the oscillator current i_{osc} leads the injected current i_{inj}, introducing a positive phase shift ($\omega_i < \omega_n$). *On the right*, i_{osc} lags i_{inj}, introducing a negative phase shift ($\omega_i > \omega_n$)

[1] This is easily understood using superposition in a linear system.

[2] Note that in [57] another sign convention is used!

$$\angle H(j \cdot \omega_i) = \frac{d\angle H(j \cdot \omega)}{d\omega}\Big|_{\omega_n} \cdot (\omega_i - \omega_n) \tag{7.3}$$

$$= -\frac{2 \cdot Q}{\omega_n} \cdot (\omega_i - \omega_n) \tag{7.4}$$

The sum of this phase shift and the phase shift caused by the injected current must exactly be equal to zero. This means that the lock range is calculated as:

$$\frac{2 \cdot Q}{\omega_n}(\omega_n - \omega_i) = \arcsin\left(\frac{A_{inj}}{A_{osc}}\right) \approx \frac{A_{inj}}{A_{osc} \cdot \sqrt{1 - \frac{A_{inj}^2}{A_{osc}^2}}} \tag{7.5}$$

$$\Leftrightarrow (\omega_n - \omega_i) = \frac{\omega_n}{2 \cdot Q} \cdot \frac{A_{inj}}{A_{osc} \cdot \sqrt{1 - \frac{A_{inj}^2}{A_{osc}^2}}} \tag{7.6}$$

which is similar to the result in [213]. Note that the total lock range is twice the one-sided lock range predicted by (7.6).

7.2.1.2 Lock Range of a Relaxation Oscillator

In the case of harmonic oscillators, one parameter, Q, determines the most important properties of the oscillator. In the case of a relaxation oscillator, this parameter is not available. Although for some topologies time-domain models are available in literature [89], the lock range of a relaxation oscillator strongly depends on the topology and the waveform of the oscillator. To illustrate this, one specific oscillator with a parameterized waveform is discussed, resulting in a remarkable conclusion.

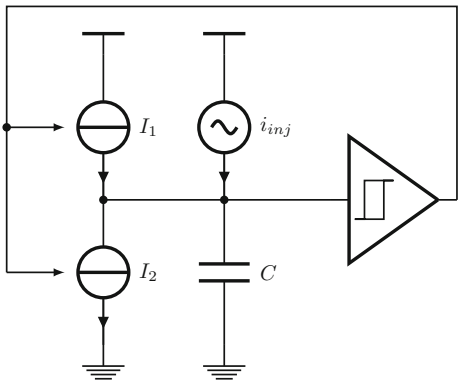

Fig. 7.5 Schematic of a relaxation oscillator using a Schmitt trigger. The current sources are switched on and off by the output signal of the Schmitt trigger. This results in a *triangular* output waveform V_C

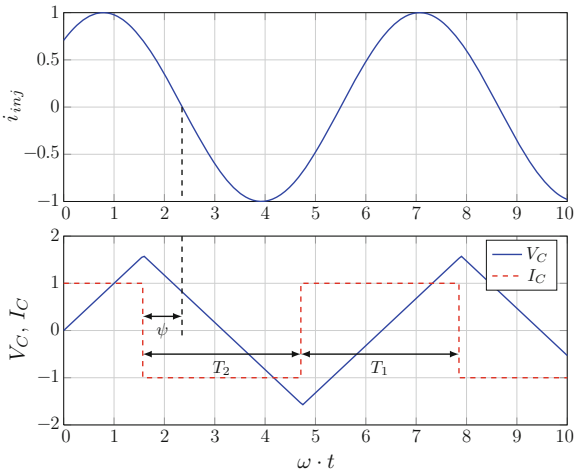

Fig. 7.6 Waveforms in the relaxation oscillator. V_C is the voltage on the capacitor while I_C is the current from the current sources. All waveforms are scaled to be able to denote the necessary time parameters

Example 7.1 The schematic of a generic relaxation oscillator using a Schmitt trigger is shown in Fig. 7.5. When the trigger levels are chosen symmetrically around zero ($V_{T,+} = -V_{T,-} = V_T$), the output waveform V_C will be a triangular wave. This is shown in Fig. 7.6. From both figures it appears that the period of the free-running oscillator can be calculated as:

$$T = T_{1,0} + T_{2,0} \tag{7.7}$$

$$= \frac{2 \cdot V_T \cdot C}{I_1} + \frac{2 \cdot V_T \cdot C}{I_2} \tag{7.8}$$

When a current is injected, the situation becomes somewhat more complicated. In this case, the length of the period must be calculated by integrating the current that flows in the capacitor. The injected current is written as:

$$i_{inj}(t) = A_{inj} \cdot \sin(\omega_i \cdot t + \psi) \tag{7.9}$$

where ψ is the phase shift between the injected current and I_C. Implicitly, without losing generality, it is assumed that at $t = 0$, $V_C = -V_T$. This results in the following system of equations:

$$\begin{cases} \int_{T_1} \frac{I_1 + i_{inj}(t)}{C} dt = 2 \cdot V_T \\ \int_{T_2} \frac{-I_2 + i_{inj}(t)}{C} dt = -2 \cdot V_T \end{cases} \tag{7.10}$$

with three unknown parameters: T_1, T_2 and ψ. Since the oscillator is assumed to be in lock with the injected signal, a third equation can be added to this system:

$$T = T_1 + T_2 = \frac{2 \cdot \pi}{\omega_i} \tag{7.11}$$

Introducing the parameter α to denote the ratio between both half periods, $0 \leq \alpha \leq 1$, translates (7.10) into:

$$\int_0^{\alpha \cdot T} \frac{I_1 + i_{inj}(t)}{C} dt = 2 \cdot V_T \tag{7.12}$$

$$\int_{\alpha \cdot T}^{T} \frac{-I_2 + i_{inj}(t)}{C} dt = -2 \cdot V_T \tag{7.13}$$

After solving both integrals, this results in:

$$T_{1,0} - \frac{\alpha \cdot 2 \cdot \pi}{\omega_i} = \frac{A_{inj} \cdot [\cos(\psi) - \cos(2 \cdot \pi \cdot \alpha + \psi)]}{\omega_i \cdot I_1} \tag{7.14}$$

$$T_{2,0} - \frac{(1-\alpha) \cdot 2 \cdot \pi}{\omega_i} = \frac{A_{inj} \cdot [\cos(\psi) - \cos(2 \cdot \pi \cdot (1-\alpha) + \psi)]}{\omega_i \cdot I_2} \tag{7.15}$$

from which α and ψ can be calculated. Calculating a generic solution for all combinations of A_{inj}, I_1 and I_2 is not possible for this equation. It is, however, interesting to study two special cases.

- $\mathbf{I_1 = I_2 = I}$: In this case the original waveform is symmetric. Since the injected waveform is also symmetric, there is no reason to assume that the resulting waveform is not. This means that $\alpha = 0.5$ and the two equations are identical:

$$T_{1,0} - \frac{\pi}{\omega_i} = \frac{2 \cdot A_{inj}}{\omega_i \cdot I} \cdot \cos(\psi) \tag{7.16}$$

  It is clear that the right-hand side of the equation has an optimum for $\psi = 0$, which results in a simple expression for the single-sided lock range:

$$T_{1,0} - \frac{T}{2} = \frac{2 \cdot A_{inj}}{\omega_i \cdot I} \tag{7.17}$$

  Similar to the case of a harmonic oscillator, ω_i can be approximated by ω_n for small injected signals. As expected, the lock range increases with an

increased injected current and decreases when the current in the oscillator is increased.

- $\mathbf{I_2} = \infty$: this means that the capacitor is flushed immediately to its lowest value and the free-running oscillation period is only determined by I_1. Since this discharging happens immediately, $\alpha = 1$, and there is no reason why a small injected signal would change this. Inserting this in both equations, results in a remarkable conclusion. Both equations reduce to zero, which means that the lock range does not exist. This is understood by the fact that, in case the frequencies of the oscillator and of the injected signal are exactly the same, the phase shift ψ has no influence on the period T_1 because the complete injected period is integrated resulting in an injected charge equal to zero. This means that a perfect sawtooth oscillator cannot be locked to an injected sine wave.

7.2.2 Dynamic Behavior of the Locking Process

The linear approach in the previous section allows to calculate the lock range of the oscillator. Also the steady-state phase shift of the oscillator and the injected signal can be calculated. However, when designing the injection-locked receiver, also the dynamic behavior of the locking process and the so-called frequency pulling are important to understand.

7.2.2.1 Adler's Equation

One of the first persons to extensively describe the phenomenon of injection locking was Adler [2]. Afterwards, many others continued his work and refined his results [196, 213]. However, the different approaches mostly lead to similar conclusions. Here, the approach of [196] is taken, since this results in an equation which is also valid for large injected signals. From (2.69) and Fig. 7.3, it can be seen that the phase shift of a tuned feedback network can be approximated by:

$$\theta_n = \arctan\left(-\frac{2 \cdot Q \cdot (\omega - \omega_n)}{\omega_n}\right) \tag{7.18}$$

where ω is the instantaneous angular frequency and ω_n is the natural angular frequency of the injected oscillator. Note that the oscillator is not necessarily in lock condition at this moment. The phase angle θ_n (which has to compensate for the induced phase shift θ_i) can at the same moment also be calculated from the phasor diagram in Fig. 7.4:

$$\tan(\theta_i) = \frac{A_{inj} \cdot \sin(\phi_i)}{A_{osc} + A_{inj} \cdot \cos(\phi_i)}. \tag{7.19}$$

Combining both equations results in:

$$\frac{2 \cdot Q}{\omega_n} \cdot [(\omega - \omega_i) - (\omega_n - \omega_i)] = -\frac{A_{inj} \cdot \sin(\phi_i)}{A_{osc} + A_{inj} \cdot \cos(\phi_i)} \tag{7.20}$$

where $(\omega_n - \omega_i) = \Delta\omega_n$ is the difference between the natural oscillator frequency and the frequency of the injected signal and where $(\omega - \omega_i)$ is the instantaneous frequency difference between the injected signal and the oscillator signal, equal to $d\phi_i/dt$. This results in:

$$\frac{d\phi_i}{dt} = \Delta\omega_n - \left(\frac{\omega_n}{2 \cdot Q} \cdot \frac{A_{inj}}{A_{osc}}\right) \cdot \frac{\sin(\phi_i)}{1 + (A_{inj}/A_{osc}) \cdot \cos(\phi_i)} \tag{7.21}$$

which is called the locking equation or Paciorek's equation. For small injected signals, the factor (A_{inj}/A_{osc}) is close to zero and Adler's equation is obtained [2]:

$$\frac{d\phi_i}{dt} = \Delta\omega_n - \left(\frac{\omega_n}{2 \cdot Q} \cdot \frac{A_{inj}}{A_{osc}}\right) \cdot \sin(\phi_i) \tag{7.22}$$

Both equations have been proven to be very useful. In [213] it is shown that exactly the same equation can be obtained by taking a nonlinear approach, which will be used when discussing the noise of an injection-locked oscillator. The lock range can also be calculated using (7.21): when the oscillator is in lock, $d\phi_i/dt = 0$. $\Delta\omega_n$ then reaches a maximum when $\cos(\phi_i) = -A_{inj}/A_{osc}$, which results in exactly the same formula as (7.6).

7.2.2.2 The Pull-in Process for Small Initial Angles

The pull-in time an oscillator needs to lock to an injected signal, depends on different parameters. Based on the equations in the previous section, different formulas can be found to calculate the lock time. In [196], (7.21) is solved exactly resulting in a complex expression. However, in some situations, the result can drastically be simplified to gain more insight in the locking process. For small frequency differences and a small initial angle $\phi_{i,0}$:

- $\mathbf{A_{inj}/A_{osc} \ll 1}$ and $\boldsymbol{\Delta\omega_n \approx 0}$: In this case, since the frequency difference is small, the time to lock strongly depends on the initial phase difference $\phi_{i,0}$. For small injected signals $(A_{inj}/A_{osc} \ll 1)$:

$$\phi_i(t) = 2 \cdot \arctan\left[\tan(\phi_{i,0}/2) \cdot e^{-B \cdot t}\right] \tag{7.23}$$

where:

$$B = \frac{A_{inj}}{A_{osc}} \cdot \frac{\omega_0}{2 \cdot Q} \tag{7.24}$$

when $\boldsymbol{\phi_{i,0}}$, the initial phase shift with the injected signal, is small:

$$\phi_i \approx \phi_{i,0} \cdot e^{-B \cdot t}. \tag{7.25}$$

Hence, the phase difference between the oscillator signal and the injected signal approaches zero exponentially.

- $\mathbf{A_{inj}/A_{osc}} \gg \mathbf{1}$ and $\boldsymbol{\Delta\omega_n} \approx \mathbf{0}$: When $\phi_{i,0} < \pi$, this results in:

$$\phi_i(t) = \arcsin\left[\sin(\phi_{i,0}) \cdot e^{[-\omega_0/(2 \cdot Q)] \cdot t}\right]. \tag{7.26}$$

When $\boldsymbol{\phi_{i,0}}$, the initial phase shift with the injected signal, is small:

$$\phi_i(t) \approx \phi_{i,0} \cdot e^{[-\omega_0/(2 \cdot Q)] \cdot t}. \tag{7.27}$$

Note that this expression is completely independent of the signal amplitude.

This shows that the final phase angle between the injected signal and the original waveform is approached exponentially.

7.2.2.3 The Pull-in Process for Large Initial Angles

To make a correct estimation on the lock time in the case when the initial angle is higher or close to 180°, another approach is taken using (7.22). This expression and also the solutions derived further, however, are only valid for signals of which:

- $\omega_n/(2 \cdot Q) \gg \Delta\omega_n$: this follows from (7.18), since this is only a linear approximation of the phase shift of the network.
- $A_{inj}/A_{osc} \ll 1$: otherwise, (7.21) must be used instead.
- The amplitude control mechanism should be quite fast compared to $\Delta\omega_n$, such that no significant amplitude effects are induced. If not, the amplitude and frequency can behave quite unpredictably.

In the following, it is assumed that the injected signal indeed has a small amplitude and is within the lock range of the oscillator. The steady-state angle between the injected signal and the oscillator signal is then, using (7.22):

$$\phi_\infty = \arcsin\left[2 \cdot Q \cdot \frac{A_{osc}}{A_{inj}} \cdot \frac{\Delta\omega_n}{\omega_n}\right] \tag{7.28}$$

From this, since the argument on the right-hand side must be between -1 and $+1$ to be a valid expression, a simplified expression for the lock range is obtained:

$$|\Delta\omega_n| < \frac{A_{inj}}{A_{osc}} \cdot \frac{\omega_n}{2 \cdot Q} = \omega_L \tag{7.29}$$

which is indeed, taking the above conditions into account, equivalent to (7.6). Solving (7.22) for $\phi_i(t)$ results in:

$$\tan\left(\frac{\phi_i(t)}{2}\right) = \tan\left[\frac{\sqrt{4 \cdot Q^2 \cdot \frac{\Delta\omega_n^2}{\omega_n^2} \cdot \frac{A_{osc}^2}{A_{inj}^2} - 1}}{4 \cdot \frac{A_{osc} \cdot Q}{A_{inj} \cdot \omega_n}} \cdot (t - t_0)\right] \cdot \frac{\sqrt{4 \cdot Q^2 \cdot \frac{\Delta\omega_n^2}{\omega_n^2} \cdot \frac{A_{osc}^2}{A_{inj}^2} - 1}}{2 \cdot Q \cdot \frac{\Delta\omega_n}{\omega_n} \cdot \frac{A_{osc}}{A_{inj}}} + \frac{\omega_n \cdot A_{inj}}{2 \cdot Q \cdot \Delta\omega_n \cdot A_{osc}} \tag{7.30}$$

where t_0 is an integration constant depending on $\phi_{i,0}$, the initial phase angle at $t = 0$. Since the injected signal is within the lock range, (7.29) is valid and the arguments of the square roots in the right-hand side become imaginary. Using the identity:

$$\tanh(x) = -j \cdot \tan(j \cdot x) \tag{7.31}$$

and using (7.28), within the lock range, (7.30) can be simplified to:

$$\tan\left(\frac{\phi_i(t)}{2}\right) = \frac{1}{\sin\phi_\infty} - \frac{\cos(\phi_\infty)}{\sin(\phi_\infty)} \cdot \tanh\left[\frac{\Delta\omega_n \cdot \cos(\phi_\infty)}{2 \cdot \sin(\phi_\infty)} \cdot (t - t_0)\right]. \tag{7.32}$$

Note that $\cos(\phi_\infty)$ is always positive within the lock range, so that $\sqrt{1 - \sin(\phi_\infty)^2} = |\cos(\phi_\infty)| = \cos(\phi_\infty)$. The time needed to reach a lock condition can then be calculated by rearranging the terms and using (7.28) and (7.29):

$$t - t_0 = \frac{2}{\omega_L \cdot \cos(\phi_\infty)} \cdot \tanh^{-1}\left[\frac{1 - \sin(\phi_\infty) \cdot \tan\left(\frac{\phi_i(t)}{2}\right)}{\cos(\phi_\infty)}\right] \tag{7.33}$$

This expression is the same as the one used in [26]. In a first step, t_0 must be calculated by substituting $\phi_i(0) = \phi_{i,0}$. As seen previously, the final phase angle ϕ_∞ is approached exponentially, which means that the result of this formula is ∞ when ϕ_∞ is substituted. Hence, an interval around the final phase shift ϕ_∞ must be substituted to calculate t_L, the time needed for the phase angle to enter the interval. This formula holds as long as $\sin(\phi_{i,0}) > \sin(\phi_\infty)$; if not, the tanh must be substituted by a coth, [2], otherwise, the lock time would become a complex number.

The pull-in or lock time is determined by three parameters: $\phi_{i,0}$, ϕ_∞ and ω_L. The initial angle can be anything between 0 and $2 \cdot \pi$. In most practical applications, it is the worst-case lock time which is of interest and often determining the system design. The initial angle plays a crucial role in this. In Fig. 7.7, the pull-in time to

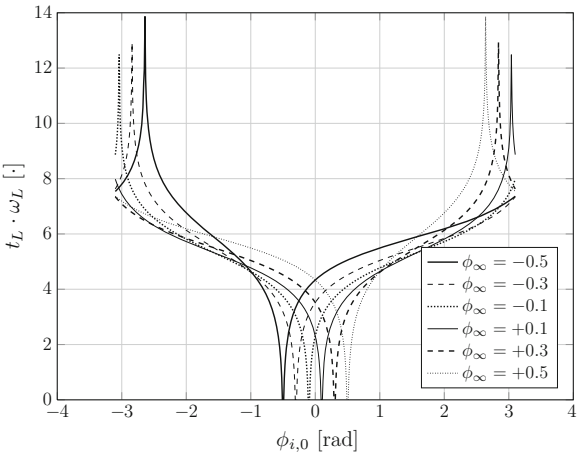

Fig. 7.7 Pull-in time for an injection-locked oscillator as a function of the initial angle $\phi_{i,0}$ and the steady state angle ϕ_∞. The time, normalized to $1/\omega_L$, to enter the interval $\phi_\infty - 0.01 < \phi_i(t) < \phi_\infty + 0.01$ is shown since the actual pull-in process occurs exponentially

reach the ± 0.01 interval around ϕ_∞ is shown for different values of ϕ_∞ and $\phi_{i,0}$. At one point, the pull-in time goes to infinity because of an unstable equilibrium. In practice, this will never occur due to noise in both the oscillator and the injected signal.

7.2.3 Frequency Beating

Up till now, the oscillator was assumed to be in lock with the injected signal. However, (7.21) and (7.22) can also be used to predict the oscillator behavior when the injected signal is outside the lock range (or the injected signal is too weak). Again, (7.22) is used, rather than (7.21), to manage the complexity of the results. Keep in mind that the conditions depicted in the previous section need to be met in order to obtain quantitatively correct results.

The discussion starts from the solution to Adler's equation (7.30). Hence, the injected signal is outside the lock range of the oscillator, which means that the arguments of the square roots in the right-hand side stay positive. Using (7.29), the solution can be simplified to:

$$\tan\left(\frac{\phi_i(t)}{2}\right) = \tan\left[\Delta\omega_n \cdot \frac{\sqrt{\frac{\Delta\omega_n^2}{\omega_L^2} - 1}}{2 \cdot \frac{\Delta\omega_n}{\omega_L}} \cdot (t - t_0)\right] \cdot \frac{\sqrt{\frac{\Delta\omega_n^2}{\omega_L^2} - 1}}{\frac{\Delta\omega_n}{\omega_L}} + \frac{\omega_L}{\Delta\omega_n} \tag{7.34}$$

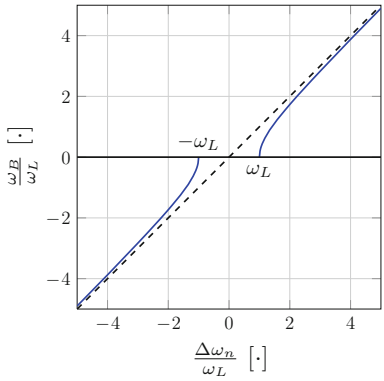

Fig. 7.8 Normalized beating frequency as a function of the normalized offset frequency. The influence of the injected signal is the largest when approaching the lock range. At the borders of the lock range, the beating frequency is equal to zero

The right-hand side of this equation is periodic due to the increasing argument of the tangent function. This means that the left-hand side is also periodic with the same period. When looking at the arguments of both tangent functions, keeping in mind that a tangent function is periodic over π, it can be seen that the so-called beating frequency is equal to:

$$\omega_B = \Delta\omega_n \cdot \frac{\sqrt{\frac{\Delta\omega_n^2}{\omega_L^2} - 1}}{\frac{\Delta\omega_n}{\omega_L}} \tag{7.35}$$

The influence of the injected signal on the oscillator frequency and phase outside the lock range of the oscillator can now be explained as follows:

- $|\boldsymbol{\Delta\omega_n}| > \boldsymbol{\omega_L}$ and $|\boldsymbol{\Delta\omega_n}|/\boldsymbol{\omega_L} \gg \mathbf{1}$: When $|\Delta\omega_n|$ increases, the beating frequency (7.35) converges to $\Delta\omega_n$. This means that the influence between the injected signal and the oscillator is low.
- $|\boldsymbol{\Delta\omega_n}| > \boldsymbol{\omega_L}$ and $|\boldsymbol{\Delta\omega_n}|/\boldsymbol{\omega_L} \approx \mathbf{1}$: In this case, the influence of the injected signal is higher. Because the frequency of the injected signal is close to the lock range, the oscillator will 'try to follow' the injected signal but cannot follow and will fall back to its original frequency. In the next cycle, the clock edges will stick again, and eventually fall back again. The closer the injected frequency to the edge of the lock range is, the higher the influence on the oscillator and the lower the beating frequency will be compared to $\Delta\omega_n$.

This effect is clearly visible in Fig. 7.8: for frequencies close to the edges of the lock range, the beating frequency is close to zero. For higher frequency offsets, the beating frequency approaches the nominal frequency difference between the oscillator frequency and the injected frequency. In Fig. 7.9 the evolution of the phase angle between the injected signal and the oscillator signal as well as the frequency beating is shown. Note that the tangent at both sides of (7.30) goes to infinity when t increases. The effects shown in these graphs are important for the design of the phase detectors, and can be used to extend the lock range of the oscillator.

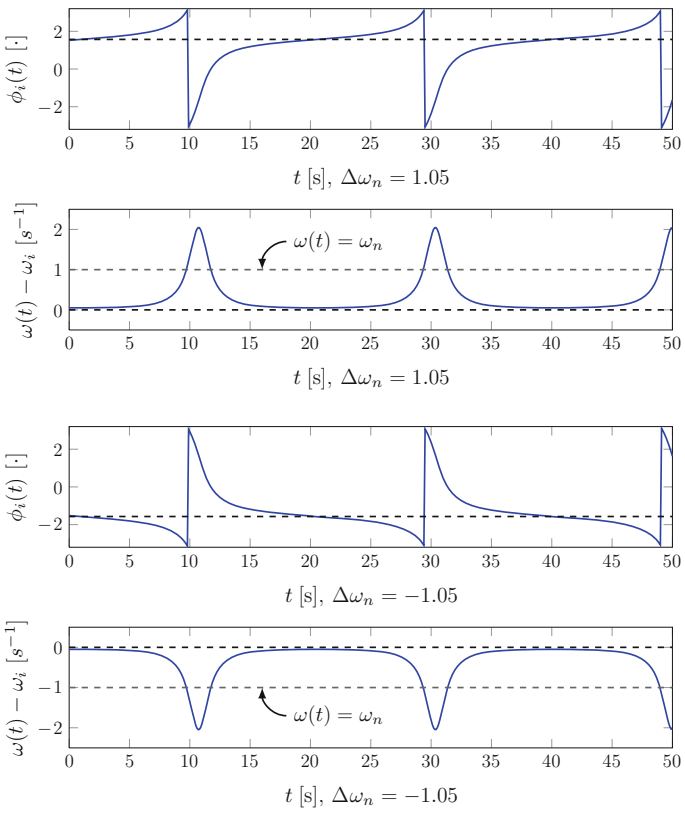

Fig. 7.9 Phase difference between the injected signal and the oscillator output when the injected signal is just out of the lock range ($\omega_L = 1$). The frequency difference between the injected signal and the oscillator output is also shown. When the phase shift is around 90° (−90°), the influence is the highest and the oscillator output 'tries to follow' the injected signal. From the moment the phase shift increases (decreases) further, the oscillator frequency falls back until the next clock edge arrives. The nominal oscillator frequency, ω_n, is also shown in the graph

7.3 Phase Noise in the Injection-Locked Oscillator

When looking at the noise in a free-running oscillator, the uncertainty on the phase increases over time. This is the result of the accumulation of random noise injections, which results in phase drift, see (3.59) and Sect. 3.6. This accumulation or integration of the noise creates the $1/f^2$ phase noise profile close to the carrier (in the case of colored noise, this is $1/f^3$ or higher order). However, in a locked oscillator, this phase drift is not possible. When a waveform is injected of which the phase noise does not accumulate (containing only white noise) and the oscillator locks to this signal, the oscillator output is not able to drift. Every phase error caused by an injected noise pulse will be corrected for as long as the oscillator stays in lock with

the injected signal. It is clear that, since the influence of the injected signal decreases with increasing frequency offset, the impact is the highest when $\omega_i \approx \omega_n$. To calculate the mechanism behind this effect on the spectrum of the oscillator, different theories are available. This goes from numerical methods [210, 230] to highly theoretical models, which are, similar to nonlinear phase noise models, often (too) complex to use at design time [76]. Although the nonlinear models often result in the best quantitative results, two more intuitive models are used to gain maximum insight in the noise shaping process. The first model is based on the noise model of Leeson; the second makes use of a PLL model.

7.3.1 Noise Model Using a Decreased Tank Impedance

Up till now, the fact was ignored that also the amplitude of the oscillator is affected by the injected signal. To take this into account, a slightly nonlinear oscillator model is used; otherwise it is impossible to take an amplitude control mechanism into account (see Sect. 2.2.3). A one-port representation of the oscillator is shown in Fig. 7.10 [213]. The behavior of this system is described by the differential equation (see also Sect. 4.2):

$$\frac{d^2 v_{osc}(t)}{dt^2} + \frac{1}{C} \cdot (G - G_m(v_{osc}) \cdot \frac{dv_{osc}(t)}{dt} + \frac{v_{osc}(t)}{L \cdot C} = \frac{di_{inj}(t)}{dt} \tag{7.36}$$

where $G_m(v_{osc})$ is the nonlinear amplifier and G represents the losses in the tank. Now assume that:

$$i_{inj}(t) = A_{inj} \cdot e^{j \cdot \omega_i \cdot t} \tag{7.37}$$

$$v_{osc}(t) = A_{env}(t) \cdot e^{j \cdot \omega_i \cdot t + j \cdot \phi_i} \tag{7.38}$$

where $A_{env}(t)$ is the envelope of the resulting oscillator signal. Substituting these terms in the above equation results in two equations, one for the real and one for the imaginary part:

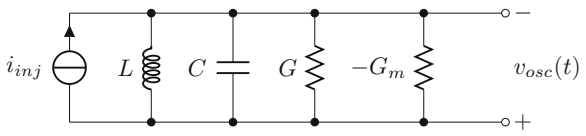

Fig. 7.10 One-port representation of an oscillator. The negative G_m is slightly nonlinear to implement an amplitude control mechanism

$$C \cdot \frac{d^2 A_{env}(t)}{dt^2} - C \cdot A_{env}(t) \cdot \left(\omega_i - \frac{d\phi_i}{dt}\right)^2 + (G - G_m) \cdot \frac{dA_{env}(t)}{dt} + \frac{1}{L} \cdot A_{env}(t) = A_{inj} \cdot \omega_i \cdot \sin(\phi_i) \tag{7.39}$$

$$2 \cdot C \cdot \frac{dA_{env}(t)}{dt} \cdot \left(\omega_i + \frac{d\phi_i}{dt}\right) + C \cdot A_{env}(t) \cdot \frac{d^2\phi_i}{dt^2} + (G - G_m) \cdot A_{env}(t) \cdot \left(\omega_i + \frac{d\phi_i}{dt}\right) = A_{inj} \cdot \omega_i \cdot \cos(\phi_i) \tag{7.40}$$

These equations can be simplified when making the following assumptions, which in most practical cases are fulfilled:

- The envelope $A_{env}(t)$ varies slowly and by a small amount. The magnitude of the envelope $A_{env,DC}$ can therefore be approximated as the tank peak current A_{osc}, multiplied by $G^{-1} = Q \cdot L \cdot \omega_n$.
- $\omega_n^2 - \omega_i^2 \approx 2 \cdot \omega_n \cdot (\omega_n - \omega_i)$
- The phase $\phi_i(t)$ and its derivatives vary slowly.

Note that the corresponding assumptions in [213] contain several errors, which are corrected here. Solving (7.39) and (7.40) results in the following two equations:

$$\frac{d\phi_i}{dt} = \omega_n - \omega_i - \frac{\omega_0 \cdot A_{inj} \cdot \sin\phi_i}{2 \cdot Q \cdot A_{osc}} \tag{7.41}$$

$$\frac{dA_{env}}{dt} + \frac{G - G_m}{2 \cdot C} = \frac{A_{inj} \cdot \cos\phi_i}{2 \cdot C} \tag{7.42}$$

The first equation, expressing the phase behavior, is Adler's equation (7.22). The second equation describes the behavior of the envelope. Within the lock range, $\frac{dA_{env}}{dt} = \frac{d\phi_i}{dt} = 0$. Using the fact that $\cos(\phi_i)^2 + \sin(\phi_i)^2 = 1$, this results in an interesting identity:

$$\left(\frac{\omega_n - \omega_i}{\omega_L}\right)^2 + \left(\frac{G - G_m}{A_{inj}} \cdot A_{env,DC}\right)^2 = 1 \tag{7.43}$$

which means that for $\omega_i = \omega_n$:

$$G_m = G - \frac{A_{inj}}{A_{env,DC}} \tag{7.44}$$

This can be understood as that the circuit is lowering its gain G_m as a result of the injection of in-phase energy. When moving to the edges of the lock range, the

gain G_m increases to G since the injected power is no longer in-phase with the oscillator signal. This also means that the closer the injected frequency is to the original oscillator frequency, the more G_m is weakened or the less time the oscillator is in the linear regime. This is another way to understand why a linear oscillator can not be injection-locked.

This Eq. (7.44) for the decrease of the tank impedance and the oscillator model in Fig. 7.10 can help to make an estimation of the noise reduction of an oscillator injection-locked with a noiseless source. The noise of the tank and the amplifier G_m can be modeled as a current source I_n in parallel with the other tank components. When there is no injection, G_m cancels the tank impedance, and the noise source experiences an impedance equal to [similar to (3.13)]:

$$\Re\{Z(\omega_n + \Delta\omega)\} \approx \frac{1}{|2 \cdot \Delta\omega \cdot C|} \tag{7.45}$$

This means that the noise current is amplified by an increasingly higher gain when the frequency is approaching ω_n. When a finite signal is injected in the oscillator at $\omega_i = \omega_n$, (7.44) predicts a tank admittance equal to $G - G_m = A_{inj}/A_{env,DC}$, which is a significant increase compared to the injectionless case where the admittance is equal to zero. When the frequency deviates from ω_n, the admittance $A_{inj}/A_{env,DC}$ stays dominant until the point where it is equal to the impedance of the free-running oscillator. This happens at:

$$|\Delta\omega| = \frac{\omega_n}{2 \cdot Q} \cdot \frac{A_{inj}}{A_{osc}} = \omega_L, \tag{7.46}$$

which means that the influence of the injected signal on the noise holds within the lock range of the oscillator. For an injected signal with a frequency offset from ω_n, the effect is less pronounced [see (7.43)]. At both edges of the lock range, $G - G_m$ is equal to zero, which is the same as for the free-running oscillator.

Although this theory gives an intuitive and easy-to-calculate description of the noise reduction due to injection locking, it is probably not the most realistic noise mechanism. This is mainly caused by the fact that its working principle is based on the noise theory of Leeson (Sect. 3.3.1).

7.3.2 A PLL-Based Noise Model

To some extent, the working principle (or at least the behavior) of an injection-locked oscillator can be compared to that of a PLL. It is therefore intuitive to model them similarly [35, 123]. In a PLL, the different building blocks help to understand the selective filtering of the noise coming from the reference of the oscillator itself. In an injection-locked oscillator, however, the only building block is the oscillator itself.

This severely complicates the possibility to obtain insight in the mechanisms behind the noise shaping and the system parameters involved.

The model starts from Paciorek's equation describing the phase of an injection-locked oscillator (7.21). When locked to a frequency within the lock range, the oscillator always compensates for the injected perturbations. This, however, strongly depends on the magnitude and timing of the perturbation. Since the injected noise is considered to be a small signal, its effect can be described using small-signal analysis. The factor A_{inj}/A_{osc} is therefore substituted by ε in (7.21):

$$\frac{d\phi_i}{dt} = \Delta\omega_n - \varepsilon \cdot \frac{\omega_n}{2 \cdot Q} \cdot \frac{\sin(\phi_i)}{1 + \varepsilon \cdot \cos(\phi_i)} \tag{7.47}$$

As long as the envelope of the oscillator signal does not change, ε can be considered to be constant. When a perturbation is applied to the circuit in steady state ($\phi_i(t) = \phi_\infty$), the behavior of the incremental phase shift $\Delta\phi_i(t)$, appears in the linearized equation:

$$\frac{d[\Delta\phi_i(t)]}{dt} \approx \Delta\omega_{inj} - \Delta\omega_{nn} - \frac{\omega_n}{2 \cdot Q} \cdot \frac{\varepsilon^2 + \varepsilon \cdot \cos(\phi_\infty)}{[1 + \varepsilon \cdot \cos(\phi_\infty)]^2} \cdot \Delta\phi_i(t) \tag{7.48}$$

where $\Delta\phi_i(t) = \Delta\phi_{inj}(t) - \Delta\phi_{osc}$, the difference of the phase shift on the injected signal and the phase shift on the (locked) oscillator signal. Similarly $\Delta\omega_{inj} = d\phi_{inj}(t)/dt$ is the frequency perturbation on the injected signal. $\Delta\omega_{nn} = d\phi_{nn}(t)/dt$ is the frequency perturbation on the *free-running oscillator signal*. Note that this signal is not equal to the locked oscillator signal! The steady-state terms in this equation are omitted since they are zero at both sides. This equation contains the noise on the injected signal as well as the noise of the oscillator. The equation is then transformed to the Laplace domain:

$$s \cdot [\phi_{inj}(s) - \phi_{osc}(s)] = s \cdot \phi_{inj}(s) - s \cdot \phi_{nn}(s) - K_{ILO}(\phi_\infty) \cdot [\phi_{inj}(s) - \phi_{osc}(s)] \tag{7.49}$$

where K_{ILO} is called the *injection-locked oscillator gain* and is equal to:

$$K_{ILO}(\phi_\infty) = \frac{\omega_n}{2 \cdot Q} \cdot \frac{\varepsilon^2 + \varepsilon \cdot \cos(\phi_\infty)}{[1 + \varepsilon \cdot \cos(\phi_\infty)]^2} \tag{7.50}$$

This equation corresponds to the equation of a first-order PLL, as drawn in Fig. 7.11. Using this model the noise transfer function for the different noise sources can easily be calculated. For respectively the noise on the injected signal and the oscillator noise, the magnitude of the transfer function to the oscillator output is calculated to be:

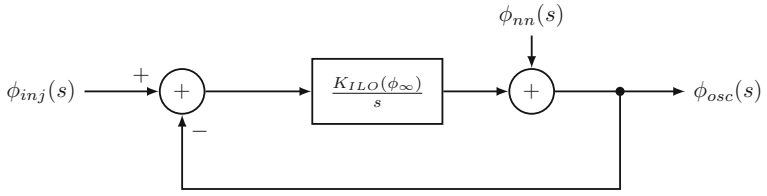

Fig. 7.11 Block diagram of a first order PLL, used to model an injection-locked oscillator

$$|H_{inj}(j \cdot \Delta\omega)| = \left| \frac{K_{ILO}(\phi_\infty)}{j \cdot \Delta\omega + K_{ILO}(\phi_\infty)} \right| = \frac{K_{ILO}(\phi_\infty)}{\sqrt{\Delta\omega^2 + K_{ILO}^2(\phi_\infty)}} \tag{7.51}$$

$$|H_{nn}(j \cdot \Delta\omega)| = \left| \frac{j \cdot \Delta\omega}{j \cdot \Delta\omega + K_{ILO}(\phi_\infty)} \right| = \frac{|\Delta\omega|}{\sqrt{\Delta\omega^2 + K_{ILO}^2(\phi_\infty)}} \tag{7.52}$$

This means that the noise in the source is low-pass filtered, while the noise of the oscillator is high-pass filtered towards the output. The bandwidth of both filters is completely determined by the value of K_{ILO}, which on its turn (when normalized to the lock range) is a function of ϕ_∞ and ε (respectively the steady-state phase shift and the ratio of the injected signal and the oscillator signal). In Fig. 7.12 the filter characteristic is shown for different values of ω_n as a function of the normalized frequency offset. The effect of an increasing ω_n is more visible in Fig. 7.13, where K_{ILO} is plotted as a function of ω_n. The -3 dB bandwidth is quite constant over the lock range, with a sudden drop at the edges. The fact that the noise reduction vanishes for an oscillator locked at the edge of its lock range, can be understood by the fact that any perturbation possibly causes the oscillator to lose its lock condition.

Finally, when both noise sources are uncorrelated, the expression for the resulting output noise can be written as:

$$S_{osc}(\Delta\omega) = \frac{K_{ILO}^2(\phi_\infty) \cdot S_{inj}(\Delta\omega) + \Delta\omega^2 \cdot S_{nn}(\Delta\omega)}{\Delta\omega^2 + K_{ILO}^2(\phi_\infty)}, \tag{7.53}$$

which results in the output (noise) spectrum of the injection-locked oscillator. An example of such a spectrum is shown in Fig. 7.14. Even when the injected frequency is close to the edge of the lock range ($\phi_\infty = 0.9 \cdot \pi/2$), the spectrum within the lock range is mainly determined by the spectrum of the injected signal S_{inj}. As can be seen, the noise level $S_{nn}(\omega_L)$ determines the minimum noise level of the injection-locked oscillator within the lock range.

Both discussed noise models of the injection-locked oscillator clearly show that the phase noise within the lock range of the oscillator is mainly determined by the noise on the injected signal. Outside the lock range, the phase noise of the oscillator itself is dominant. This is exactly what is expected: the low frequency variations in the injected signal are tracked by the injection-locked oscillator, while the high-

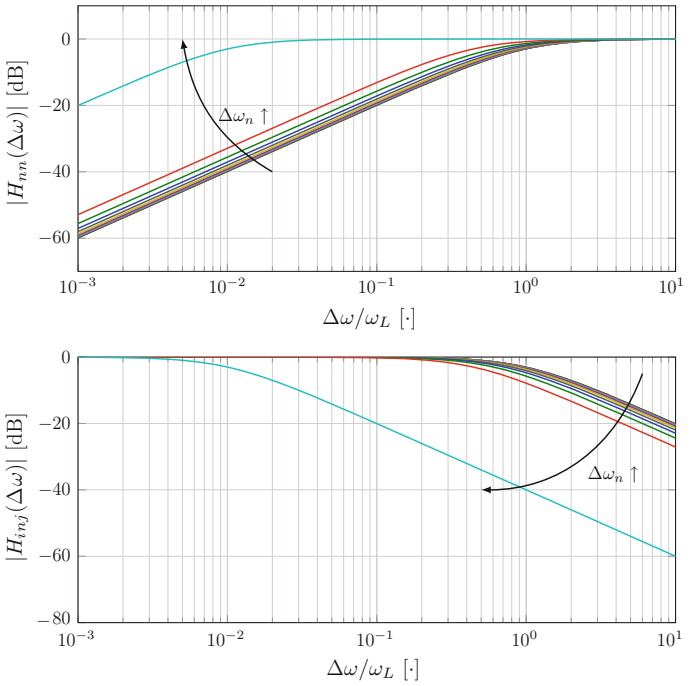

Fig. 7.12 Transfer characteristic for both the oscillator noise (*top*) and the noise on the injected signal (*bottom*). When the frequency difference $\Delta\omega_n$ between the natural oscillator frequency and the injected signal increases, the -3 dB filter frequency $K_{ILO}(\phi_\infty)$ decreases

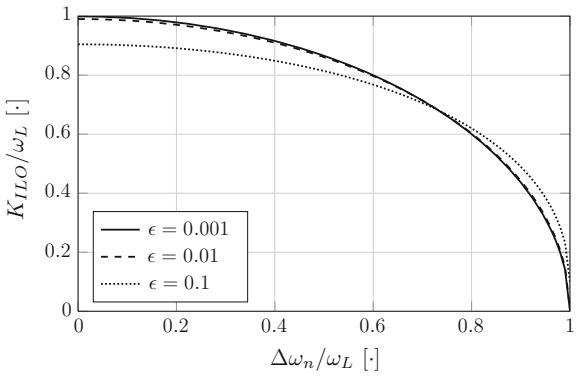

Fig. 7.13 Normalized -3 dB frequency of the filter characteristic as a function of the normalized frequency difference between the natural oscillator signal and the injected signal $\Delta\omega_n$. The different *curves* are for different injection levels and are all normalized to their corresponding lock range ω_L

frequency variations are filtered. Or, vice versa, due to the locking process, the low-frequency variations of the oscillator, caused by for instance colored noise or amplitude variations, are corrected by the injected signal, while the high-frequency phase variations stay visible at the output. In practice, the main (low-frequency) part

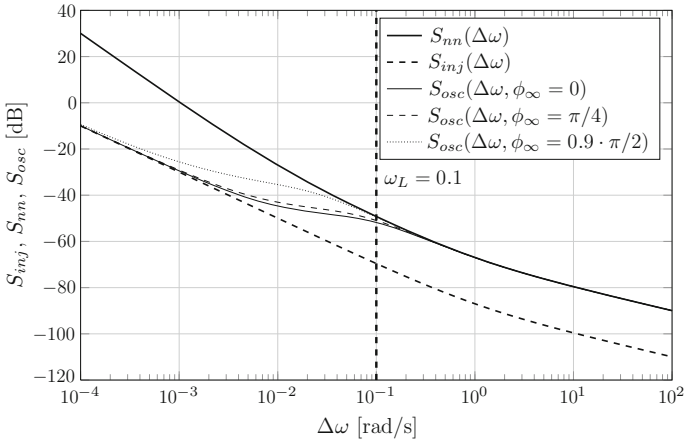

Fig. 7.14 Example noise spectrum of an injection-locked oscillator as a function of the injected noise spectrum S_{inj} and the oscillator spectrum S_{nn} for different values of ϕ_∞. The spectrum within the lock range is mainly determined by the injected spectrum and the oscillator noise at the edge of the lock range. The frequency is normalized to ω_n and $\omega_L = 0.1$

of the jitter is therefore caused by the injected signal and correlated between all injection-locked sensor nodes.

7.4 The Wirelessly-Locked Oscillator in 130 nm

In the previous sections the phenomenon of injection locking has been investigated elaborately. The obtained principles and relationships will now help to better understand the design decisions for the injection-locked oscillator. The principle of injection locking is mainly preferred above that of a conventional PLL for power reasons. As previously pointed out, the power budget on the wireless tags is extremely limited. A block diagram of the first implementation developed in this thesis is shown in Fig. 7.15. As will be seen in Sect. 7.4.1.1, the oscillator acts as a 2-fold frequency divider for the buffered antenna signal. Finally, also a phase detector is implemented (Sect. 7.4.2) for use as a lock detector and/or to increase the oscillator lock range.

7.4.1 The Oscillator Topology

The used RC feedback network, shown in Fig. 7.16, is based on the feedback network of a Wien bridge oscillator (see Chap. 5). By separating one pole of the feedback network, the two stages are oscillating 45° out of phase. This has some benefits for the phase detector described in Sect. 7.4.2. The current-voltage transfer function of

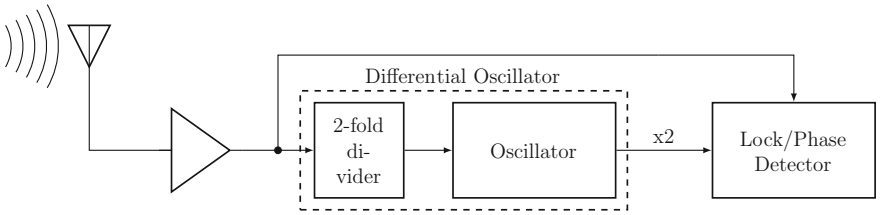

Fig. 7.15 Block diagram of the injection-locked oscillator system. After buffering the antenna signal, it is injected to the differential oscillator which acts as a 2-fold frequency divider. Also a phase detector is implemented to detect a lock condition or to further increase the lock range

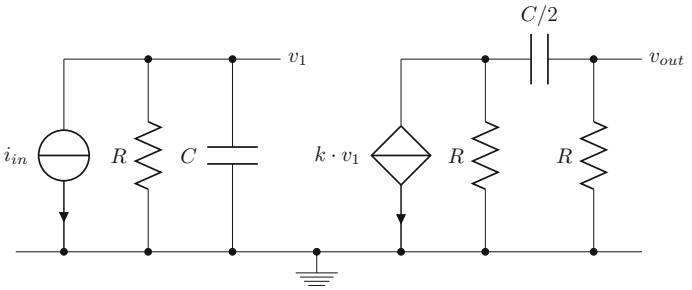

Fig. 7.16 Schematic of the two-stage RC feedback network, based on a Wien bridge oscillator

the feedback network can be written as:

$$H(s) = \frac{v_{out}}{i_{in}} = \left(s \cdot C + \frac{1}{R}\right)^{-1} \cdot k \cdot \frac{R^2}{2 \cdot \left(R + \frac{1}{sC}\right)} \tag{7.54}$$

$$= \frac{k \cdot \frac{R}{C}}{2 \cdot \left(s^2 + \frac{2 \cdot s}{R \cdot C} + \frac{1}{R^2 \cdot C^2}\right)} \tag{7.55}$$

where k is the transconductance of the voltage-controlled current source. To close the feedback loop, the current source on the left is changed to a voltage-controlled current source. The two current sources are assumed to be identical with a transconductance equal to k. The new transfer function must be equal to 1 to satisfy the Barkhausen criterion (Theorem 2.2):

$$H(s) = \frac{v_{out}}{v_{in}} = \frac{k^2 \cdot \frac{R}{C}}{2 \cdot \left(s^2 + \frac{2 \cdot s}{R \cdot C} + \frac{1}{R^2 \cdot C^2}\right)} \tag{7.56}$$

$$= \frac{k^2 \cdot R^2 \cdot \omega_n \cdot s}{2 \cdot \left(s^2 + \frac{\omega_n}{Q} \cdot s + \omega_n^2\right)} = 1 \tag{7.57}$$

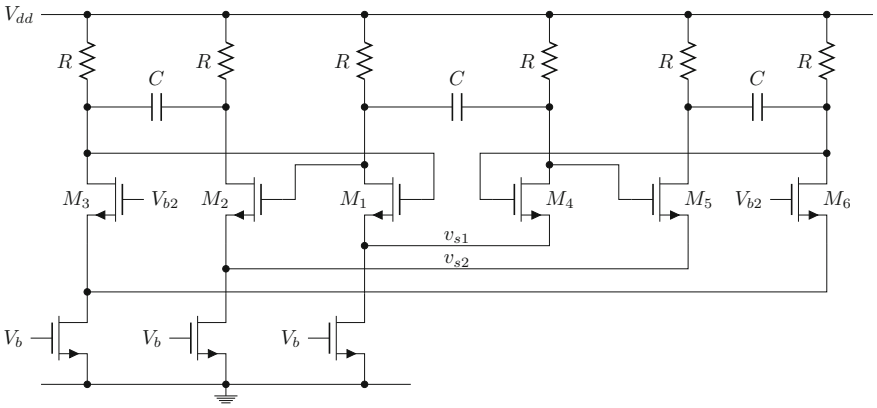

Fig. 7.17 Schematic of the differential implementation of the proposed oscillator. By connecting the 2 oscillators differentially and by sharing the capacitor in the first stage, the oscillators are forced in opposite phase. The voltages v_{s1} and v_{s2} are used to implement a lock detection circuit and a circuit to increase the lock range

$$\text{with} \quad \omega_n = \frac{1}{R \cdot C} \quad \text{and} \quad Q = \frac{1}{2} \tag{7.58}$$

When substituting $s = j \cdot \omega$ and $\omega = \omega_n$, the natural angular frequency of the feedback network, the left-hand side of (7.57) is real, which stands for a phase shift equal to zero. Furthermore, $k^2 \cdot R^2$ must be equal to 4 to obtain a loop gain equal to 1. Note that the attenuation of the RC network ($A_t = 1/4$) is somewhat higher than in the case of a Wien bridge oscillator ($A_t = 1/3$). The oscillation frequency is equal to the pole frequency of the first stage which results in a $-45°$ phase shift between input and output. Figure 7.3 shows the amplitude and phase of the transfer function; the angular frequency is normalized to ω_n and the gain $k \cdot R$ is equal to one.

For a practical implementation, the voltage-controlled current sources are changed by transistors. Furthermore, a differential topology is preferable for reasons of symmetry and a better common-mode and supply rejection ratio [219]. Apart from that, by controlling the current sources at the source of the differential pair, the current consumption can be kept constant in a changing environment. The final schematic of the differential oscillator is shown in Fig. 7.17. The two differential oscillators are connected by the first stage's capacitor which forces the two oscillators in opposite phase: only when the two oscillators are running in opposite phase, the shared capacitor has the right capacitive value to fulfill the Barkhausen criterion. In the other case, the attenuation of the feedback network increases drastically at the point where the phase shift equals zero.

An extra measure has been taken to decrease the power consumption of the oscillator. The output stage (M_3 and M_6) is mainly present to implement the correct DC biasing for the feedback signal. Furthermore, it implements the output resistor of the feedback network. This resistance, however, is mainly determined by the physical

resistor R and not by the transistor branch. The current in the output stage has been decreased by a factor of 4 compared to the other stages. The DC biasing is preserved by increasing the resistor R. An extra resistor (not drawn) is put between the two differential branches (the gates of M_1 and M_4) to obtain the correct impedance in the feedback network.

7.4.1.1 Use as a Frequency Divider

Since the use of the circuit is in low-power applications, the oscillation frequency must be as low as possible. Therefore, the 2.4 GHz RF signal is not injected at the drain of the differential transistors (the oscillator output), but at the source. In this way, the differential pair acts as a mixer with the oscillator signal.[3] If the frequency of the injected signal is around twice the tank natural frequency ω_n, the sum frequency is filtered out by the tank and only the difference, which is close to the natural frequency, is injected into the tank. The amplitude of the injected current is determined by the mixer's conversion gain K_{mix}, as shown in Fig. 7.18. Since this conversion gain is determined by many circuit parameters such as the linearity, it can best be determined by simulation. The upper bound of K_{mix} is obtained when the differential pair is switching hard. In this case the conversion gain is equal to $2/\pi$ [47]. The one-sided lock range referred to the input is then equal to [from Eq. (7.6)] [213]:

$$(\omega_i - \omega_n) = \frac{\omega_n}{2 \cdot Q} \cdot \frac{4}{\pi} \cdot \frac{A_{inj}}{A_{ds}} \tag{7.59}$$

where A_{ds} is the peak oscillator current through the differential transistors. It is clear that the amplitude of the injected signal, compared to the oscillator current, is determining the lock range. The losses in the first stage are only one third of the total losses in the feedback network. Since the gain of the two stages is equal, the input signal of the first stage is smaller than that of the second stage. To increase the lock range, it is therefore better to inject the current in the first of the two identical stages. This, of course, does not take the efficiency of the mixer into account. Simulations show that the first stage is the better one to inject the signal. In the following section, some other techniques to increase the lock range are discussed.

As explained, a trade-off exists between the lock range and the sensitivity. Furthermore, the lock range of the oscillator must be large enough to be sure that all (1.2 GHz) oscillators can be locked to the 2.4 GHz signal (which lies within an ISM frequency band). Due to the use of an RC oscillator with a low Q factor, even for a weak injected signal, the oscillator easily locks to the external signal. However, because a fully-integrated oscillator is aimed for, a frequency offset of ±20 % can be expected after production due to statistical process variations. Within one production batch, the expected frequency deviation is lower than ±5 %. During measurements

[3] It is due to the nonlinearity of the differential pair that the oscillator signal also appears at the common-mode point at double frequency.

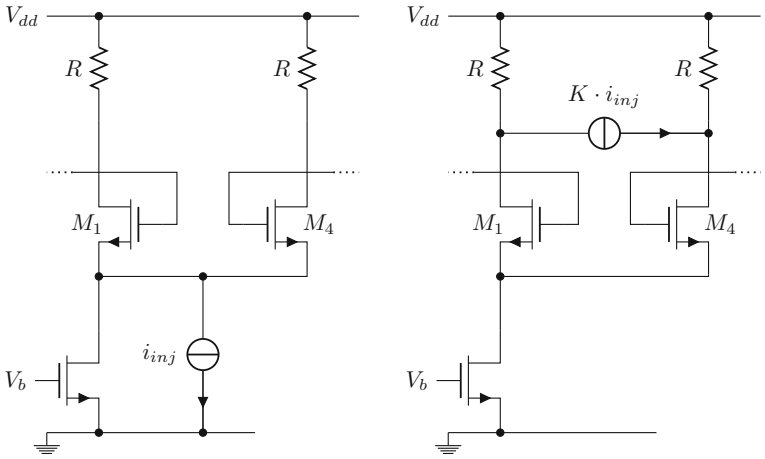

Fig. 7.18 The injection-locked oscillator can be described as a single balanced mixer. *On the left* the current with angular frequency $2 \cdot \omega_i$ is injected at the sources of the differential pair. This corresponds to the current source *on the right* with angular frequency ω_i. K_{mix} is the conversion gain of the mixer

the sensitivity to reach a $\pm 10\,\%$ lock range is determined: when using this lock range, all measured samples have been able to lock to the same input signal under all circumstances (over temperature and supply voltage). Using (7.6), the expected sensitivities for higher input levels can easily be extrapolated. Note that the lower the input signal, the more the lock range suffers from offset etc. in the input amplifiers.

7.4.2 Techniques to Increase the Lock Range

It is clear that the amplitude of the injected signal is low compared to the oscillator current, which limits the lock range. Different possibilities exist to increase the lock range of the oscillator.

7.4.2.1 Input Amplifiers

The most straightforward approach is to amplify the injected signal. A two-stage differential amplifier has been designed, with a total voltage gain of around 20 dB or 10. This already is a 10-fold increase of the lock range. The power consumption of the amplifier is $28\,\mu$W. To increase the dynamic range and decrease the noise sensitivity, the input stage is designed two times bigger than the second stage.

7.4.2.2 The Integrating Phase Detector

Another approach is the use of a phase detector. As shown in Sect. 7.2.3, when so-called pulling or frequency beating occurs, the injected signal already has some influence on the oscillator. This means that, when a signal is injected with an angular frequency just above or below the edge of the lock range, the oscillator already tries to follow the sine edges. From Fig. 7.9, it can be concluded that for an injected frequency above the lock range, the average phase shift between the injected waveform and the oscillator is negative and close to −90°. Similarly, when the injected frequency is just below the lock range, the mean phase shift will be around 90°. For frequencies further away from the lock range, the average phase shift will go to zero. Inside the lock range, the mean phase shift can be calculated from (7.2): it goes from 90° on the low side to −90° on the high side. In Fig. 7.19 this is shown for an injection-locked oscillator modeled in Matlab. In the upper graph the lock range is clearly visible. In the two graphs below, the averaged phase shift is shown between the injected signal and the oscillator output (or a 90°-shifted version). The oscillator signal and the injected signal (second graph) can be used to increase the lock range. A 90°-shifted version of the oscillator signal and the injected signal can be used as a lock detection (third graph).

A PMOS differential pair has been used to detect this phase difference as shown in Fig. 7.20. By connecting the common-mode point of the second oscillator stage v_{s2}, which is 90° shifted compared to the first stage, and the injected antenna signal

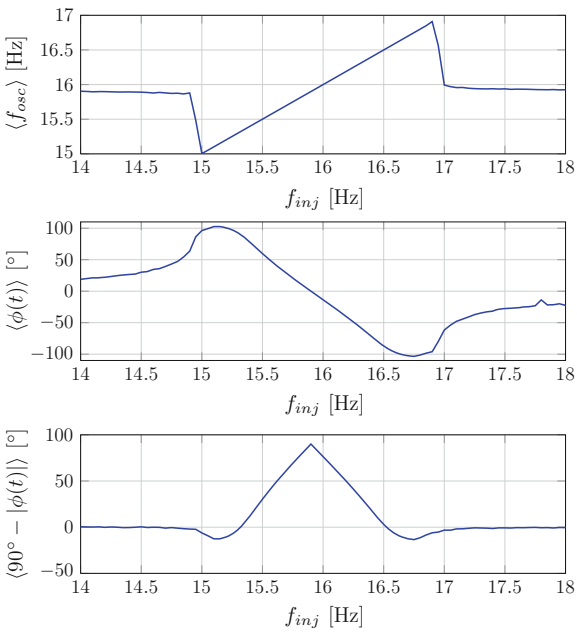

Fig. 7.19 Average output frequency and phase difference as a function of the frequency of the injected signal. The phase curves can be obtained by mixing the oscillator signal (or a 90°-shifted version) with the injected signal

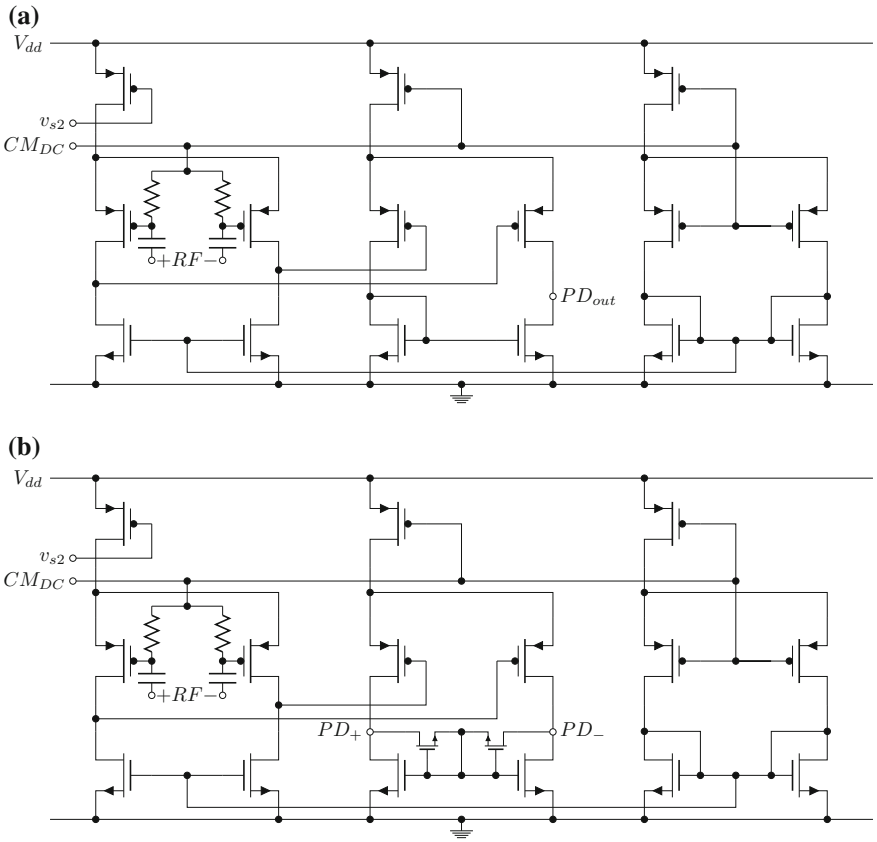

Fig. 7.20 Schematic of the integrating phase detector. The biasing of the detector is done by the differential stage *on the right*, making use of the common-mode signal coming from the oscillator biasing replica. The detector has two inputs: the antenna signal coming from the output of the first stage of the input amplifier and the common-mode source voltage of one of the two oscillator stages, v_{s1} or v_{s2}. **a** Shows a single-ended version with a digital output; **b** is a differential implementation with a lower gain and an analog output

to the differential pair, the circuit behaves as an averaging phase detector. A second differential stage is used to amplify the output, which actually is the down-mixed signal of the antenna input. This signal can be used to adapt the oscillator frequency and in this way extend the lock range [236]. Furthermore, if the common-mode input is connected to the common-mode point of the first stage v_{s1} (or the common mode of the output buffers, since this is not affected by the injected signal), the circuit can be used as a lock detector. The phase detectors, including the shared biasing circuitry of both phase detectors, consume only 6 μW. As shown in Fig. 7.20, the output can be both single-ended, for the lock detection, and differential, to use in a feedback loop. The single-ended version has been implemented with a high gain to obtain a digital output.

7.4.3 Measurement Results

The circuit has been processed in a 130 nm standard CMOS technology. The key measurement properties of the oscillator are listed in Table 7.1. A chip photomicrograph is shown in Fig. 7.22. As shown in Table 7.2, different versions of the chip have been processed. Because 1.2 GHz is a rather high frequency for an integrated RC oscillator, also a 600 MHz version has been processed. Apart from this frequency, also a difference was made in the input gain and the phase detectors. The input gain can also be controlled by adapting the externally applied biasing current. Good results have been obtained with prototype 1 and 2: a two-stage input amplifier with a gain of 10–15. With a −59.3 dBm antenna signal, which is well below the expected input signal of the energy scavenger [51], the measured lock range is 950–1,150 MHz. This wide lock range is mainly caused by the low Q factor and the low oscillation amplitude (120 mV peak-to-peak at the output of the first stage). The use of a source follower at the output of the input amplifier also increases the lock range drastically, since it is mainly the injected current which determines this range. The measured free-running frequency of 3 samples together with the minimum upper bound and maximum lower bound of the lock range are shown in Fig. 7.21. As a function of temperature, the free-running frequency decreases drastically. This is caused by the increasing impedance of the resistors, which is desired to compensate for the decreasing gain with increasing temperature. However, for an input signal of 1,050 MHz, all samples have been able to lock over the entire temperature range. The increasing lock range as a function of the supply voltage is mainly caused by the increased gain at the input stage. The externally applied biasing current has been kept constant during these measurements. The minimum measured power consumption at 1 V is 127 μW, without taking the output buffers into account.

By monitoring the output of the phase detectors, it has been possible to detect a lock condition. The differential output of the second phase detector is around 20 mV (−20 mV), for an input RF signal of ±200 MHz above (below) the lock range. However, in this first version, no feedback loop has been implemented.

The results are compared to other state of the art timing solutions in Table 7.4. From this table it is clear that an increased accuracy goes at the expense of an increased

Table 7.1 Overview of the key measurement properties (8 samples)

Technology	130 nm CMOS
Area (core)	520 μm × 340 μm (90 μm × 75 μm)
Power consumption at 1.0 V	127 μW
Temperature range	−20 to 100 °C
Voltage range	0.7–1.6 V
Frequency range	950–1,150 MHz
Sensitivity	−59.3 dBm

Table 7.2 Overview of the implemented prototype versions

Number	f_{osc} (MHz)	Input amp	Lock detector	Phase detector
0	1,200	1-stage	Single-ended	Differential
1	1,200	2-stage	Single-ended	Differential
2	1,200	2-stage	Differential	Single-ended
3	600	1-stage	Single-ended	Differential
4	600	2-stage	Single-ended	Differential
5	600	2-stage	Differential	Single-ended

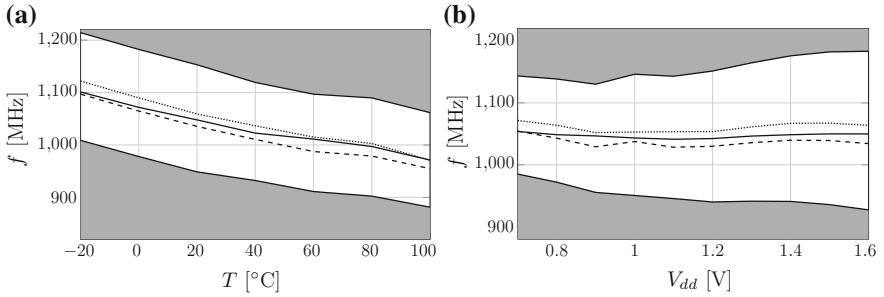

Fig. 7.21 Measured free-running frequency of 3 different samples. Also the minimum upper bound and maximum lower bound of the lock range of all 8 samples are shown as a function of **a** the temperature and **b** the supply voltage

power consumption. Furthermore, the available solutions that can also sustain an unstable supply voltage are rather limited.

7.4.3.1 Use with an UWB Transmitter

After a 32-fold frequency division, the clock has been connected to an UWB transmitter. Even with the transmitted signal which interferes with the carrier, no influence on the lock range and the lock behavior of the oscillator has been observed. This is caused by the low-pass filtering of the injected signal by the injection-locked loop (Sect. 7.3.2). This makes the locking principle a feasible solution to overcome the synchronization problem in WSNs and impulse-based UWB links.

7.4.4 Conclusion on the 130-nm Injection-Locked Oscillator

In this first prototype, different aspects of the use of injection locking for node synchronization have been demonstrated. First of all, it is clear that the low Q factor

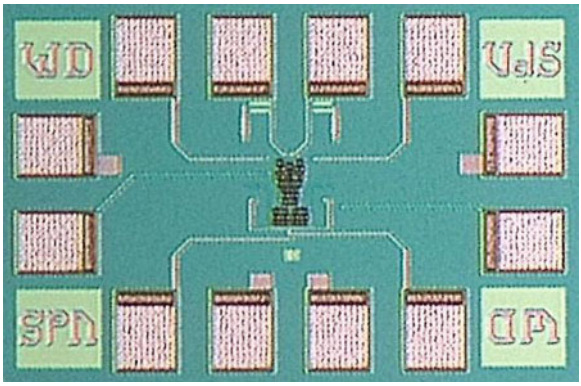

Fig. 7.22 Photomicrograph of the injection-locked oscillator

of the RC oscillator makes it possible to have a huge lock range. The differential two-stage oscillator topology makes it possible to implement a lock detection and/or a phase detector to increase the lock range. The drawback of the low Q factor is the increased noise in the injection-locked oscillator. However, as shown in (7.53), the output spectrum within the lock range is mainly determined by the spectrum of the injected signal. Furthermore, because all nodes lock to the same injected signal, a correlation exists between the low-frequency noise in the different sensor nodes. This correlation results in a performance increase of the communication link between the different nodes. Due to the low-pass filtering of the injected signal, the circuit is robust against perturbations or even short interrupts in the received signal. This is the main reason why this solution is preferred over amplifying the received signal and feeding it to a frequency divider. The main drawback is the power consumption of the high-frequency RC oscillator. Even with 2-fold frequency division, the high frequency (1 GHz) puts a minimum value to the power consumption of the oscillator.

7.5 The 40-nm Injection-Locked Receiver

The 40 nm implementation of the injection-locked oscillator contains 2 major innovations over the injection-locked solution from the previous section. First of all, instead of locking to the carrier frequency, the oscillator locks to the envelope of an AM-modulated clock signal. This improvement saves a lot of power since no high-frequency oscillator or frequency divider are needed. In Fig. 7.23 a block diagram of the system is shown: only the input amplifier and the AM-demodulator are working at the carrier frequency. The second innovation is the addition of an ultra-low-power receiver which can be used for network coordination. This receiver uses the phase difference between the oscillator and the injected signal. By applying phase steps to the clock signal, a bit stream can be received, indicating whether the

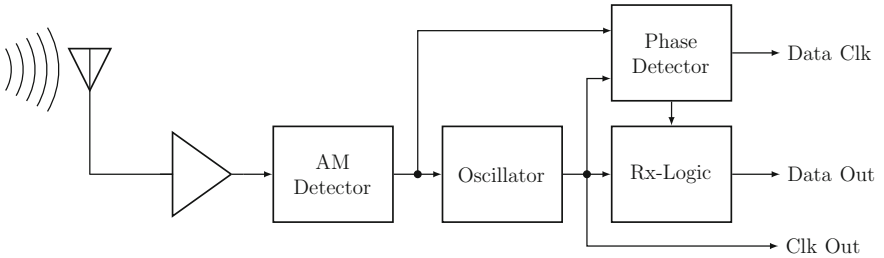

Fig. 7.23 Block diagram of the clock and receiver circuitry. Only the input amplifier and the AM demodulator are working at the (high) carrier frequency

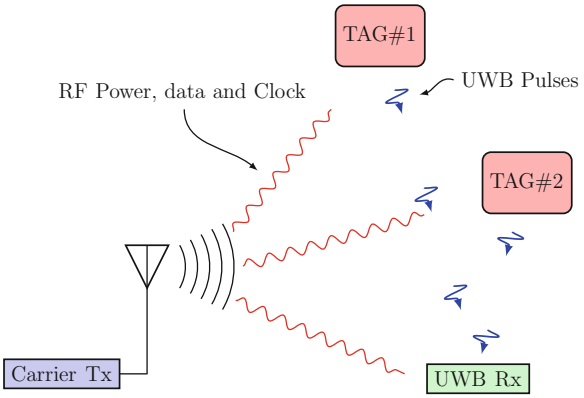

Fig. 7.24 System overview of the wireless sensor network (*WSN*) with RF clock distribution and coordination receiver. The specifications of the clock carrier in terms of temperature and supply voltage stability are unimportant as long as the different network components can lock to the wirelessly distributed clock signal. The implemented downlink makes network coordination possible and avoids data collisions

RFID tag is expected to respond or not. Other benefits of the previous topology are retained: the clock frequency is exactly constant and equal at both the transmitter and the receiver side; in case of a sudden carrier loss the clock works several cycles autonomously; the carrier of the clock signal can be shared with an RF power signal. The main drawback of the presented topology is the lack of selectivity and the large input noise bandwidth, which results in a drastically decreased input sensitivity. A modified version of the overall system setup is shown in Fig. 7.24.

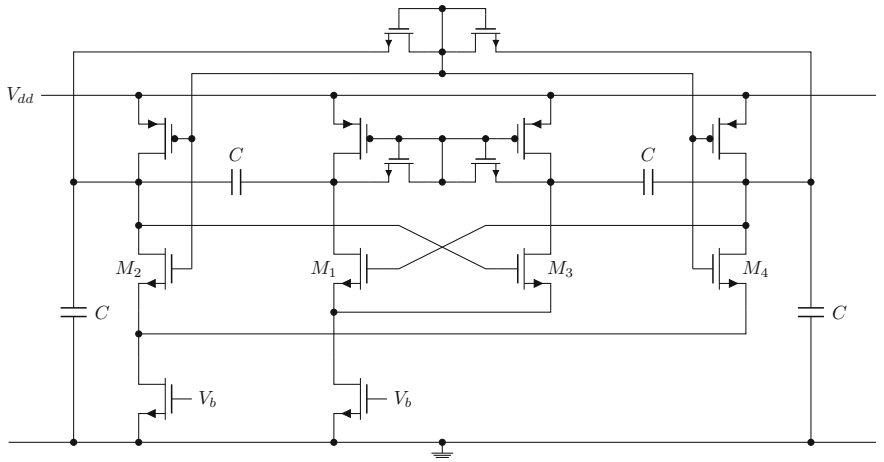

Fig. 7.25 Schematic of the differential implementation of the proposed oscillator. By connecting the 2 oscillators in series, both transistor branches are oscillating differentially

7.5.1 The Clock Circuit

The used oscillator is a differential RC Wien bridge oscillator. The working principle of this oscillator has elaborately been discussed in Chap. 5. Similar to the implementation in Chap. 5, two inverting amplifiers and two feedback networks are put in series. This results in the differential topology of Fig. 7.25. The power consumption of this 30 MHz oscillator is around 16 μW.

7.5.1.1 The Input Amplifier

To increase the sensitivity of the circuit to the carrier and to obtain a usable signal amplitude at the input of the AM detectors, a four-stage differential input amplifier is used. A block diagram of the input structure is shown in Fig. 7.23. The amplifier contains four stages of which the schematic is shown in Fig. 7.26. Each stage has its own common-mode feedback. The input is AC-coupled and the third stage contains a DC-suppression capacitor to avoid offset problems. For noise reasons, the first stage is sized with a factor of 4 and it has two DC biasing resistors to set the DC level of the two antenna inputs. The total power consumption of the amplifier is 40–48 μW to obtain a gain of 6, 30, 150 or 720 (the output can be taken at the output of each amplifier stage), as shown in the bode plot on Fig. 7.27. In order to avoid saturation of the input amplifiers, the AM-detector and/or the receiver circuit (see next section), an automatic gain control can be useful. The gain of the input amplifier in this prototype design can be controlled by selecting the appropriate amplifier stage and/or by adapting the biasing current. As will be seen, however, the gain of the

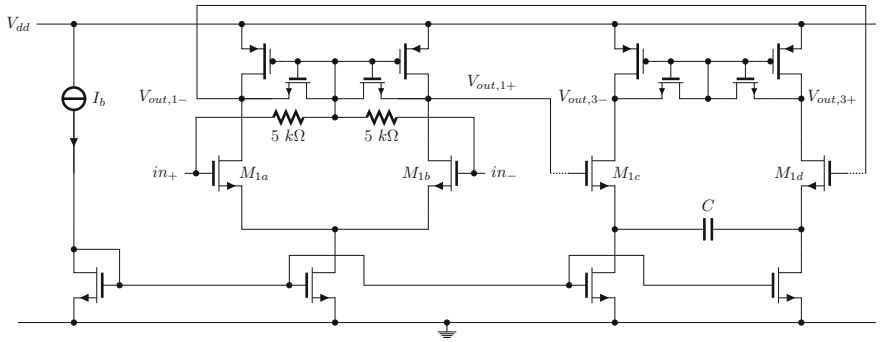

Fig. 7.26 Schematic of the first and third stage of the four-stage input amplifier. Each stage has its own common-mode feedback, implemented by the two NMOS transistors on *top*. The first stage also has two biasing resistors to set the DC level of the antenna inputs. The input is AC-coupled and the third stage contains a DC-suppression capacitor

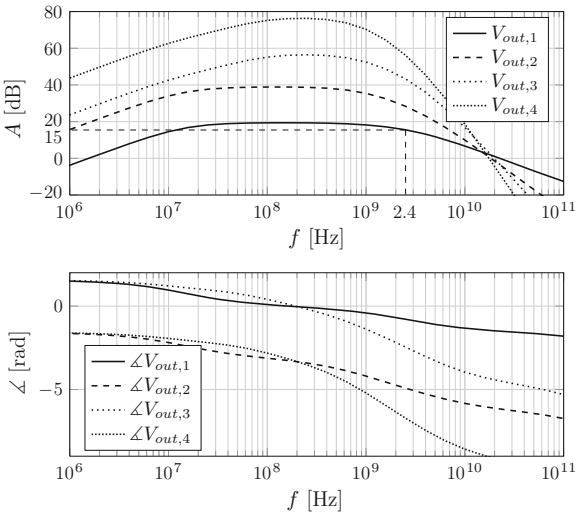

Fig. 7.27 Bode plot of the 4-stage front-end amplifier stages. The gain of the first stage at 2.4 GHz is around 15 dB or 6. The total gain is between 6 and 720, depending on the number of stages

baseband signal can also be controlled, which turns out to be a much more reliable control mechanism.

7.5.1.2 The AM-Detector

The oscillator is locked on the clock signal which is AM-modulated on the RF carrier. The schematic of the AM-detector is shown in Fig. 7.28. The biasing voltage V_B

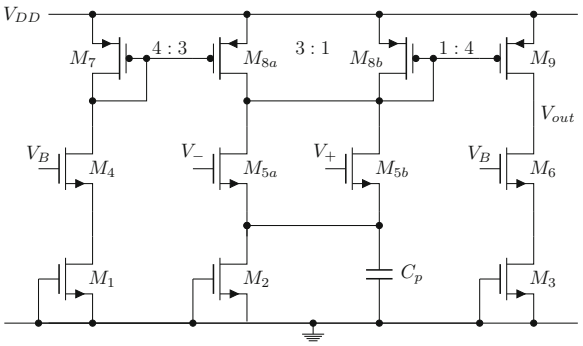

Fig. 7.28 AM-detector with an NMOS input pair. In practice, two AM-detectors, NMOS and PMOS, are used to generate a differential signal which can be injected differentially into the oscillator

is coming from the amplifier and is also used to set the DC output voltage of a high-pass filter between the amplifiers and the detectors. In practice, two AM-detectors (or envelope detectors) are used to obtain a differential signal: one designed with an NMOS input pair and a mirrored version using a PMOS input pair. The output signals of these detectors are amplified and AC-coupled to the gate of transistor M_2 and M_4 of the oscillator (Fig. 7.17). To obtain a stable DC biasing, the detectors are replica biased, using a replica of the input amplifiers. The total power consumption of the two AM-detectors is below 3 μW.

As shown in [201], the conversion gain of an envelope detector strongly depends on its input amplitude. Starting from Fig. 7.28, an approximation of the output current can be calculated as a function of the input amplitude. As a result of the low-Vth NMOS transistors in cutoff (M_1 to M_3), the input transistors (M_{5a} and M_{5b}) are biased in weak inversion. The current through these transistors is then written as:

$$I_{ds,wi} = I_{D0} \cdot \frac{W}{L} \cdot e^{\frac{V_{gs}-V_{th}}{n \cdot k \cdot T/q}} \tag{4.44}$$

The envelope detector relies on the nonlinear component of the output current. Before calculating this, it is assumed that the capacitor C_p causes a zero at the source of both input transistors with a frequency well below the envelope frequency (around 30 MHz).[4] Using a Taylor expansion of (4.44), the nonlinear component of the current through each one of the input transistors for an input voltage $V_i = V_s \cdot \sin(\omega_i \cdot t)$ can be approximated by the second-order term:

$$i_o = \frac{V_i^2}{2} \cdot \frac{\partial^2 I_{ds,wi}}{\partial V_i^2} \tag{7.60}$$

[4] Without this assumption, the nonlinear component of the current is drastically damped by the source impedance.

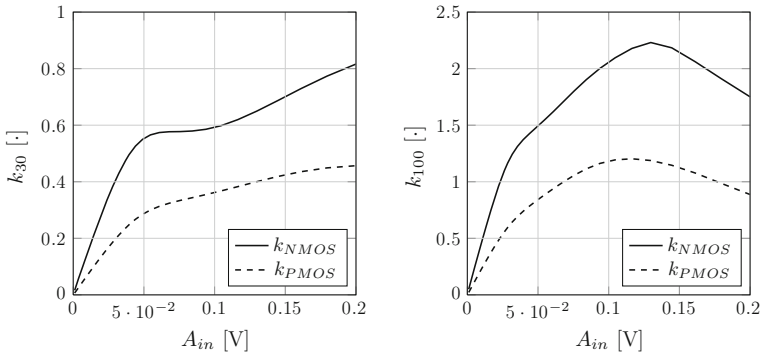

Fig. 7.29 Conversion gain of the envelope detectors for different input levels. *On the left*, the conversion gain is shown as a function of the input amplitude with 30 % modulation depth. Note that this is the simulated output amplitude divided by the carrier amplitude and not the amplitude of the envelope. *On the right*, the same graph is shown for a signal with 100 % modulation depth

$$= \frac{g_m}{2 \cdot n \cdot V_t} \cdot V_s^2 \cdot \sin^2(\omega_i \cdot t) \tag{7.61}$$

where $V_t = kT/q$ is called the thermal voltage. The high-frequency component at $2\omega_i$ is filtered out by the limited bandwidth of the circuit, and the low-frequency output is equal to:

$$i_o \approx \frac{g_m}{4 \cdot n \cdot V_t} \cdot V_s^2 \tag{7.62}$$

As can be seen, the transconductance of the envelope to the output is then equal to:

$$g_{env} \approx \frac{g_m}{4 \cdot n \cdot V_t} \cdot V_s \tag{7.63}$$

The output current of the input transistors is added (a factor of 2) and mirrored to the output branch (a factor of 4). To obtain the output voltage, it needs to be multiplied by the output impedance. This, however, can only be determined more accurately by simulations (r_0 of the used short-channel transistors is rather low). A simulation of the conversion gain of both phase detectors (with a PMOS and an NMOS input pair) is shown in Fig. 7.29. The linear increase of the conversion gain for small amplitudes is clearly visible. For higher amplitudes, the conversion gain increases more slowly because the biasing point of the transistors is moving towards strong inversion. Finally, the conversion gain decreases, because the output amplitude is limited by the supply rails.

In a next step, the output of both AM detectors is sent to a differential amplifier before injecting it into the oscillator. This amplifier is shown in Fig. 7.30. The gain of the amplifier can be controlled by V_{ctrl} to prevent the oscillator from being overtaken by the injected signal, which would result in a non-working receiver. A second two-

stage amplifier is used to amplify the AM signal towards the receiver, which needs a digital signal at the input. The Bode plot of both amplifiers and the small-signal gain of the first amplifier as a function of the control signal are shown in Fig. 7.31. Note that for large signals, the control transistor 'clips' the output signal instead of only controlling the small-signal gain. This is a useful feature when the input voltage saturates, since this clipping level is mainly independent from the input amplitude. Finally, a detailed overview of the AM front-end and receiver chain is shown in Fig. 7.32. All building blocks discussed above are schematically drawn, including their impact on the input spectrum.

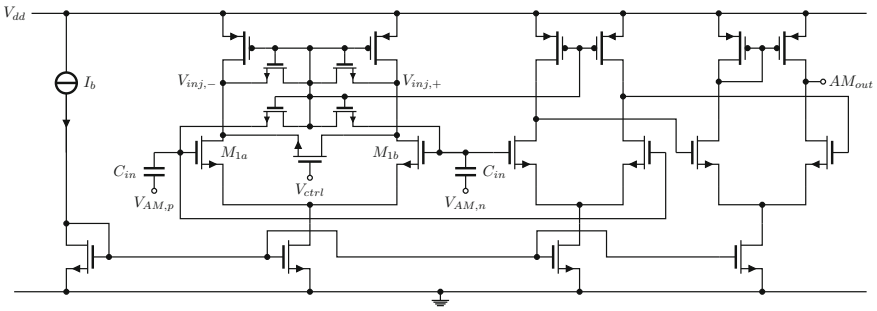

Fig. 7.30 The output of both AM detectors is combined in a differential amplifier before injecting it into the oscillator. The gain of the amplifier can be controlled by adapting V_{ctrl}. The AM signal is also amplified by a two-stage amplifier to obtain a digital signal at the input of the phase detector

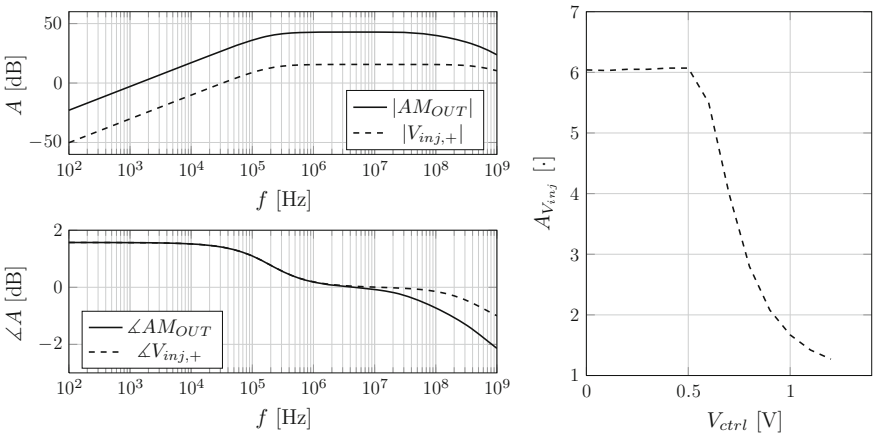

Fig. 7.31 Bode plot of the two baseband amplifiers including the high-pass filter at the input. The first amplifier, which amplifies the baseband signal towards the oscillator, has a controllable gain. This is shown in the graph *on the right* (simulated for a 1 V supply voltage, at 30 MHz)

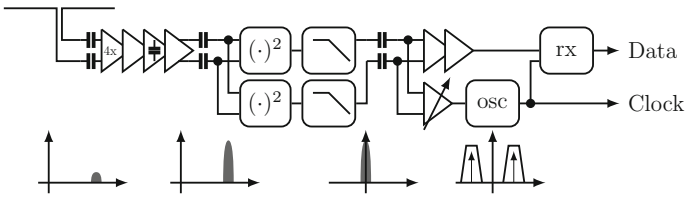

Fig. 7.32 Detailed overview of the receiver chain. The operations performed on the input spectrum are schematically drawn *at the bottom*. The combination of two phase detectors detects the negative envelope as well as the positive envelope of the input waveform, which results in a signal gain of 2

7.5.1.3 Sensitivity Analysis of the AM-Receiver

To get an insight in the maximum achievable sensitivity of the receiver chain, a brief analysis is done on the input amplifier in combination with the AM detectors. As will be seen, several approximations are made. A more detailed analysis of a typical AM receiver chain (filter, input amplifier, envelope detector) can be found in [88, 201]. When looking only at the amplifier and a standard envelope detector, it can be shown that the total noise factor F_{tot} is equal to [200]:

$$F_{tot} = 2 \cdot F_{amp} + \frac{N_{LF} \cdot k_{DC}^2}{N_{src} \cdot A_v^2 \cdot k^2} + \frac{N_{o,ED}}{N_{src} \cdot A_v^2 \cdot k^2} \tag{7.64}$$

where F_{amp} is the noise factor of the front-end amplifier, N_{LF} is the low-frequency (below the envelope detector bandwidth) output noise density of the front-end amplifier, $N_{o,ED}$ is the noise at the output of the envelope detector and N_{src} is the source noise density (equal to $4kTR_s$). These parameters need to be simulated to obtain an approximate value of the total noise factor. A detector bandwidth B_{det} of 30 MHz is assumed, since this is the frequency of the clock envelope. To obtain N_{LF} and $N_{o,ED}$, the noise spectrum is calculated and integrated. This value is divided by $B_{noise} \approx 2$ GHz to obtain a *brickwall* noise density. B_{noise} is the noise bandwidth of the amplifier, which can be estimated from Fig. 7.27 and is large due to the lack of an input filter. As the gain of both phase detectors is assumed to be identical and since the noise on the amplifier output signal is expected to be uncorrelated, a 3 dB SNR increase can be expected by using two envelope detectors instead of one. To take this into account, the average detector gain is used and F_{tot} is divided by 2. Using F_{tot}, the input-referred noise power can then be written as:

$$P_{n,in} = -174 + 10 \cdot \log(B_{noise}) + NF_{tot} \tag{7.65}$$

where NF_{tot} is equal to $10 \cdot \log(F_{tot})$ and the power is expressed in dBm. To obtain an estimate of the minimum signal input power, P_m, it is assumed that a minimum SNR of 12 dB at the output of the envelope detectors is needed to obtain a proper data

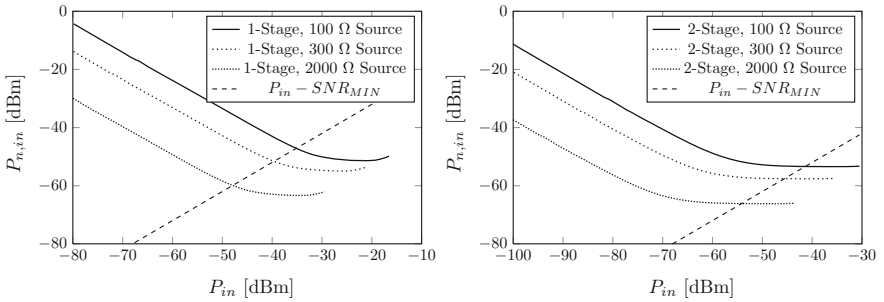

Fig. 7.33 The hockey stick curves show the input referred noise of the AM receiver chain for different input resistances and a 30 % modulation depth. The crossing of these curves with the $P_{in} - SNR_{min}$ curve determines the minimum detectable input signal level. *On the left* the input gain is equal to 6 (1 stage), *on the right* an input gain of 30 is assumed (2 stages)

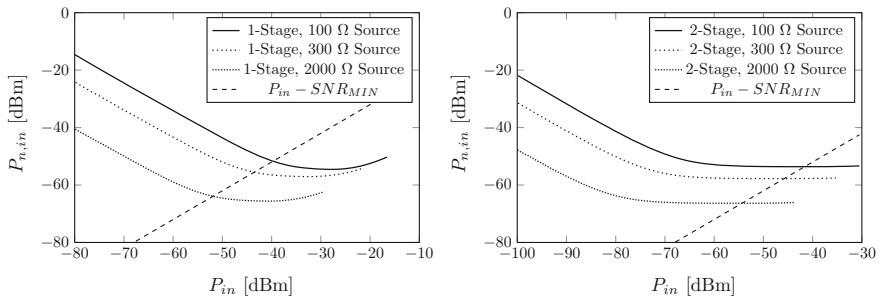

Fig. 7.34 The hockey stick curves show the input referred noise of the AM receiver chain for different input resistances and a 100 % modulation depth. The crossing of these curves with the $P_{in} - SNR_{min}$ curve determines the minimum detectable input signal level. *On the left* the input gain is equal to 6 (1 stage), *on the right* an input gain of 30 is assumed (2 stages)

reception (similar to [201]). $P_{n,in}$ and $P_{in} - SNR_{min}$ are drawn in Figs. 7.33 and 7.34 for different values of the source resistance, the modulation depth and the input gain. For each configuration, the crossing with the $P_{in} - SNR_{min}$ curve results in the minimum detectable input signal level.

From this figures, different conclusions can be drawn. As opposed to the implementations discussed in [201], the noise is dominated by the noise figure of the input amplifier instead of the input sensitivity of the AM detectors (the AM detectors cause the curves to go up on the left). This is mainly caused by the huge input noise bandwidth. In the first place, this can be seen from the crossing points, which are in the horizontal area, but also from the fact that from a certain gain, the gain of the amplifier does not have a big impact on the sensitivity (taking the 150 or 720-fold amplifier has no added benefit). Due to the high signal level and the sensitivity of the envelope detectors, the impact of the modulation depth is low in the case of an input gain of 30. The increase of the curves for high input levels is caused by the saturation

of the detectors, which has a negative impact on the conversion gain. Since this saturation results in a reduction of the output noise and only the 30 MHz component of the signal is of interest, this increase can be neglected (the noise reduction by the saturation effects is not taken into account in the calculation of F_{tot}). It is seen that for a matched input impedance, a signal level of −38.8 to −43.5 dBm (depending on the modulation depth and the input gain) can be detected for a 100 Ω input impedance. The 300 Ω resistance is added since this is the resistance of a folded dipole antenna.

The sensitivity analysis in this section is only an approximation, used for common AM receivers. The situation here is different since the output signal of the detectors is injected in an oscillator. As seen previously, this results in a significant reduction of the noise components outside the lock range (the oscillator acts as a bandpass filter). Therefore, only the noise in a small band around the 30 MHz carrier is of interest in this design. Furthermore, the data detection compares well to that of a BPSK receiver, which requires a much lower SNR to obtain the same bit error rate. Both effects, however, are not taken into account in the above calculation. To control the noise bandwidth at the output of the AM detectors, the lock range itself can be controlled by controlling the gain of the baseband amplifiers discussed in the previous section. The reduced sensitivity of this topology compared to the 130 nm implementation is mainly caused by the huge noise bandwidth of the signal injected in the AM detectors. In the previous design, this noise bandwidth is limited by the limited lock range of the oscillator.

7.5.2 The Receiver Circuit

By locking the oscillator to the injected signal, the synchronization problem between the RFID tag's transmitter and the receiver is mainly solved. Adding a continuously working receiver to each network node, in order to add some coordination in the sensor network, is difficult due to the limited power budget. However, a decent lock detection and a mechanism to avoid data collisions also reduces data losses in the network and thereby also the power consumption. Both functions can easily be implemented by the injection-locked receiver, a novel receiver topology which only adds a negligible cost to the power budget.[5]

7.5.2.1 The Injection-Locked Receiver

As mentioned earlier, the phase difference ϕ_i between the injected signal and the oscillator is always between ±90°. However, by applying an abrupt phase step to the injected signal, the oscillator will instantaneously lose its lock condition. After a few cycles, the oscillator will be in lock again. These sudden phase steps can be detected by a simple phase detector such as a D-flipflop. The time between two phase

[5] Recently a similar architecture using two injection-locked oscillators was patented [320].

shifts indicates whether a one or a zero is received. A block diagram of the receiver is shown in Fig. 7.35. The amplitude of the injected signal (lock range) as well as the applied phase shift do affect the number of cycles in which the lock condition recovers from the applied phase shift. This has an influence on the maximum data rate of the receiver: the stronger the injected signal, the faster the oscillator reached stable lock and the higher the data rate can be [see (7.33)]. From Fig. 7.7, the lock time can be estimated as a function of the lock range:

$$t_L \cdot \omega_L \lesssim 8 \tag{7.66}$$

As seen from the measurements of the 130 nm injection-locked oscillator (see Sect. 7.4.3), a lock range of around ±10 % of the oscillation frequency is assumed to make sure the oscillator locks to the injected signal in all circumstances. The lock range in this case depends on the strength of the received signal as well as the modulation depth. The estimated number of periods to recover to oscillator lock is then calculated to be:

$$\frac{t_L}{T} \lesssim \frac{80}{2 \cdot \pi} \approx 12.7 \tag{7.67}$$

The output signals of a simulated oscillator and receiver are shown in Fig. 7.36. The oscillator has a lock range of ±10 % and $\phi_\infty = 28.5°$. As expected, it takes around 10 cycles to recover from an applied phase step. Also the evolution of $\phi_i(t)$ is similar to what is predicted in Fig. 7.7: $\phi_i(t)$ evolves faster to ϕ_∞ at phase angles where the curve of the lock time is more horizontal. Also ϕ_∞ is a crucial parameter in the lock process since the output of the phase detector switches at $\phi_i(t) = 0$.

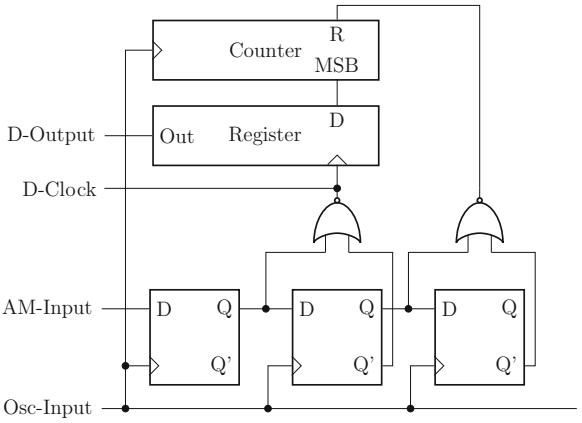

Fig. 7.35 The receiver consists of a simple shift register of which the first flipflop is used as a phase detector. When a phase shift is applied to the input, the data register will clock. Depending on the most significant bit of the counter, which counts the clock cycles between two phase shifts, a zero or a one is received. In the subsequent clock cycle, the counter is reset

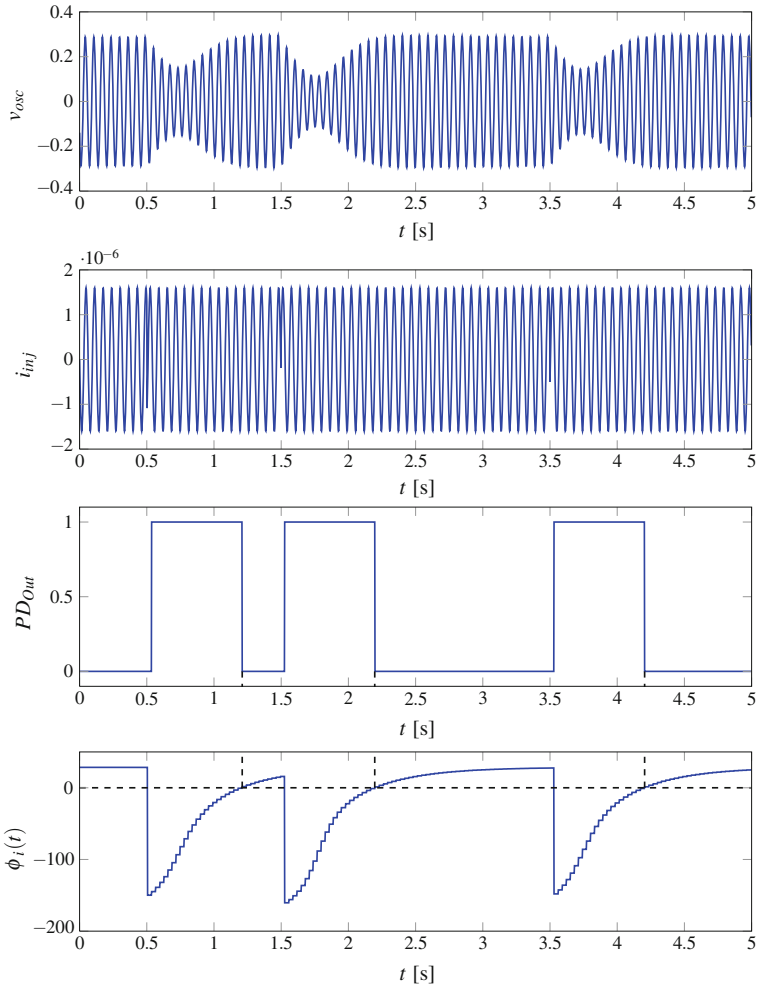

Fig. 7.36 The simulated waveforms of an injection-locked receiver. Three times a 180° phase shift is applied to the injected signal. The *bottom graph* shows the evolution of the phase difference. It takes around 10 periods until the output of the phase detector recovers from the phase shift. Note that the oscillator only has a weak nonlinearity in its amplifier, which results in a slow amplitude regulation

When the input signal is too strong, the oscillator will never lose its lock and the receiver will stop working since the injected signal completely dominates the oscillator output.[6] For flexibility reasons in this first prototype the reset value of the counter is programmable. This allows to test the receiver for different input

[6] This effect strongly depends on different system parameters such as the detector output bandwidth, the exact moment and sharpness of the applied phase step, the oscillator amplitude, etc.

frequencies, signal strengths and data rates. During measurements a data rate of 1.8 Mbit/s was obtained (the counter resets to a start value of 16). The additional power consumption of the receiver logic is below 1.5 μW (compared to a total power consumption of 72 μW). Note, however, that the working principle strongly affects the frequency stability of the oscillator. This has to be taken into account when other tag circuitry (such as an UWB transmitter) is used simultaneously with the receiver. However, when used as a coordination receiver, this does not pose any problem.

Note that the receiver has an increased noise sensitivity since 16 correct phase detections are needed to obtain 1 data bit. Although most of the time the oscillator is locked to the injected signal (which results in an increased success-rate), the noise has a great impact during the re-locking of the oscillator. This noise sensitivity in the receiver logic can therefore greatly be reduced by switching off the phase detector for 10–14 cycles after a phase step is detected. This can be done by the addition of a few extra digital gates.

7.5.2.2 Use as an AM-FM Receiver

The same circuitry can also be used as an FM receiver. By modulating the frequency of the AM signal continuously (instead of by applying hard phase steps), the angle between the injected signal and the oscillator signal also changes. In this way, the output of the phase detector can be switched in a controlled manner. The main drawback, however, is the oscillator frequency which is not precisely known after production. This results in an uncertainty about the moment the phase detector will switch from 1 to 0 and vice versa.

A last option is to change the modulation depth of the transmitted signal. To receive this, however, the phase detector must slightly be adapted to switch at a nonzero phase angle. This can also be obtained by delaying one of the input signals. By changing the amplitude of the injected signal, the phase angle changes and the receiver logic can be triggered. The main problem, again, is the impossibility to predict this behavior at the transmitter side. Therefore, the proposed technique using phase steps is considered to be the most robust solution for communication and synchronization in this application.

7.5.3 Measurement and Simulation Results

The circuit has been processed in a 40 nm standard CMOS technology. After reviewing the measurements of the RF sensitivity, however, several inconsistencies where detected in the obtained results. Since some values cannot be verified, these results are omitted and replaced by simulated values. The key measurement and simulation properties of the oscillator and the receiver circuit are listed in Table 7.3. A chip photomicrograph is shown in Fig. 7.37. Compared to previous designs such as the 130 nm implementation, the power consumption is drastically reduced due to the

Table 7.3 Overview of the key measurement and simulation properties (5 samples)

Technology	40 nm CMOS
Area (core)	550 µm × 300 µm (65 µm × 26 µm)
Power consumption at 1.0 V	72 µW
Temperature range	−20 to 100 °C
Voltage range	0.7 to 1.5 V
Frequency range	23–36 MHz
Carrier frequency	Max 2.6 GHz
Max. data rate	1.8 Mbit/s
Sensitivity	−43 dBm

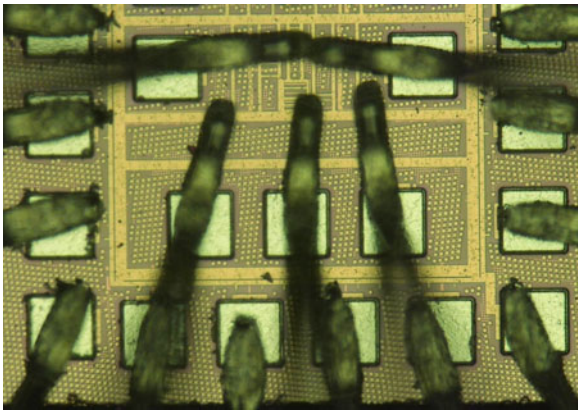

Fig. 7.37 Photomicrograph of the 40 nm injection-locked oscillator and receiver

use of AM-detectors instead of the locking to the carrier frequency. Another power advantage, comes from the technology node in which the circuit has been processed. The lock range of the oscillator is high due to the low Q factor and can easily be enlarged by increasing the gain of the low-frequency AM signal. In turn, the oscillator itself can oscillate at a higher amplitude, which enables a better frequency stability and output noise performance.

7.5.3.1 Results on the Injection-Locked Oscillator

Although the different blocks in the injection-locked oscillator are affected by the changing temperature and supply voltage, the injection-locked oscillator has proven to be a robust design. The receiver chain, however, has several critical points. The first point is the output of the front-end amplifier, which saturates at an output amplitude around 600 mV at 1 V (450 mV at $V_{dd} = 0.7$ V). When this output saturates, the

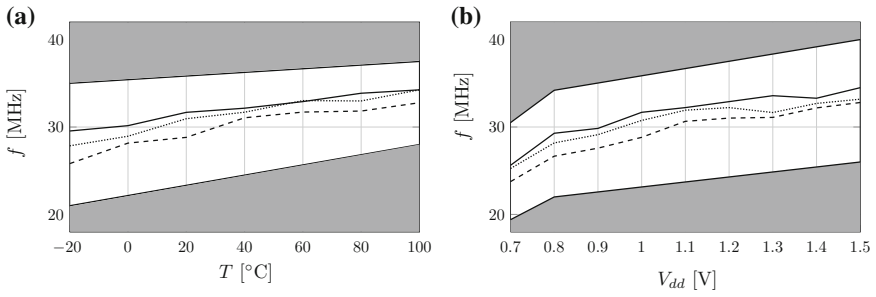

Fig. 7.38 Measured free-running frequency of 3 different samples of the 40 nm implementation. Also the estimated lock range is shown as a function of **a** temperature and **b** supply voltage

envelope of the AM signal can be removed. A second critical point is the noise sensitivity and the sensitivity of the envelope detectors, which puts a lower limit to the input signal level. It has, however, been observed that it is mostly the noise which determines the lower limit of the input sensitivity. The third critical point, which is important for the functionality of the receiver chain, are the outputs of the baseband amplifier which at high amplitudes possibly overtake the oscillator circuit. This will be discussed into more detail in the next section.

Four parameters can be modified while operating the circuit: the power of the received carrier, the modulation depth, the input gain and the gain of the baseband amplifier, which can be controlled by adapting V_{ctrl}. The power of the carrier plays a crucial role in the saturation of the input amplifier. The best way to avoid this saturation is by using a modulation depth of 100 % (on-off keying), which can impossibly be masked by the input amplifier. This, however, mostly results in an oversteering of the oscillator, which needs to be avoided by adapting V_{ctrl} properly. Two differential input signals (with a matched 50 Ω impedance each) are assumed in the following calculations. A −39 dBm signal with a 100 % modulation depth results in a 30 mV signal at the output of the amplifiers. The combined conversion gain (k_{100}) for this signal level is around 1.2 and a 210 mV differential signal is sent through a high-pass filter towards the oscillator. This signal results in a lock range of around 23–36 MHz at room temperature and at a 1 V supply voltage. This lock range will vary over temperature as well as over the supply voltage, as can be seen in Fig. 7.38. The gain of the input stage decreases slightly over the considered temperature range, which results in a decreasing lock range with increasing temperature. The gain increases with increasing supply voltage, as can be seen in Fig. 7.38 on the right.

7.5.3.2 Results on the Injection-Locked Receiver

The receiver can saturate as a result of an injected signal which then overrules the proper functioning of the oscillator itself. This effect is expected to happen with an injected signal amplitude of around 250–300 mV. In Fig. 7.39, this is calculated for

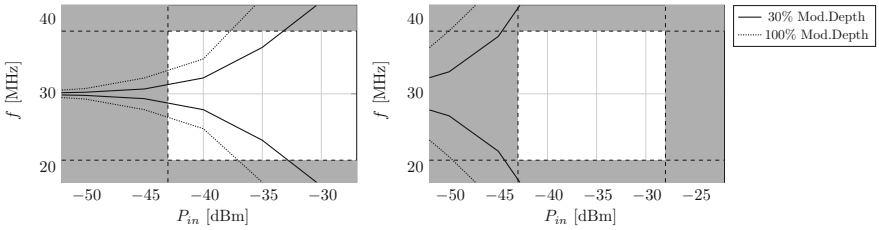

Fig. 7.39 Operating range of the injection-locked receiver and the upper and lower limit of the lock range without controlling the baseband gain. *On the left* an input gain of 6 is used, *on the right* the input gain is equal to 30

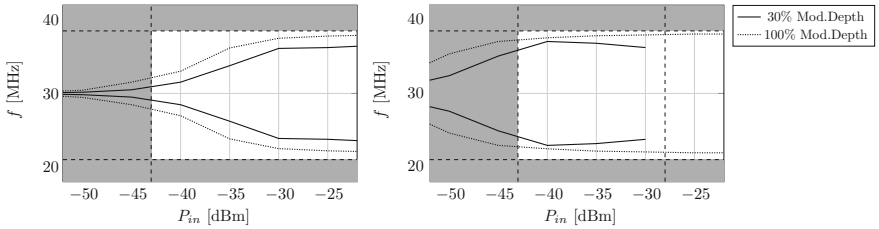

Fig. 7.40 Operating range of the injection-locked receiver and the upper and lower limit of the lock range with baseband gain control. V_{ctrl} was set to 0.75 V (or $V_{dd}-0.25$ V). *On the left* an input gain of 6 is used, *on the right* the input gain is equal to 30

different input signal levels. The graph shows the calculated minimum and maximum of the lock range for two different input modulation depths. The upper and lower border of the receiver operating region are determined by the amplitude of the injected signal (which indeed corresponds to a certain lock range). The border on the left is caused by the noise in the input amplifier. On the right, the baseband signal vanishes as a result of a saturating input amplifier. This can be solved by using a 100 % modulation depth. Fig. 7.40 contains the same information when the control voltage is used to adapt the baseband gain. The voltage is typically set around 0.75 V or $V_{dd} - 0.25$ V. This results in a limited amplitude of the baseband signal, which indeed results in a receiver working at higher input levels as long as the input amplifier does not saturate. As an alternative, clipping (transistor) diodes can be used to limit the signal. These graphs are calculated using simulation results of the different building blocks.

The receiver principle was proven by measurements. As simulated, it can reach a data rate up to 1.8 Mbit/s (1 bit every 16 cycles), using a modulation depth of both 30 % and 100 %. For each bit, 180° of phase shift is applied to the baseband signal. At low signal levels, however, the receiver chain is vulnerable to noise, which is also a function of $\Delta\omega_n$, the difference between the natural oscillator frequency and the frequency of the injected signal. As expected, the robustness increases drastically

when moving towards higher signal levels in combination with baseband gain control and/or an increased modulation depth.

7.5.3.3 Comparison to the State of the Art

Compared to other state of the art timing solutions (Table 7.4), the circuit is a unique combination of power and accuracy and is the only circuit which includes an ultra-low-power coordination receiver. In most other designs, such as [178], an increased accuracy goes at the cost of a higher power consumption. Furthermore, in literature, most timing solutions do not face the problem of an unstable supply voltage, as we experience in the targeted autonomous WSN nodes. By using the injection-locked receiver, a lock condition can easily be detected, but also network coordination has been implemented. A comparison to other state of the art (wake-up) receivers is shown in Table 7.5. Although the power consumption of the proposed receiver is somewhat higher than the two first implementations, this solution also solves the synchronization problem between the different network nodes. The bit error rate (BER) is not measured extensively, but during measurements a success rate of $>95\,\%$ was observed for receiving a correct 16-bit tag-ID.[7] In this design the unique tag-ID can be programmed externally in a (volatile) shift register. The different tags can be addressed independently through the AM-PSK downlink, and collisions of different data bursts can be avoided. This lowers the global power consumption drastically, and has a huge benefit in terms of network and communication efficiency.

A severe drawback of the current implementations is the lack of selectivity and sensitivity. Although the coordination receiver prevents the wireless tag from transmitting useless data bursts, the tag can be activated by signals in 'any' transmission band. Moreover, the lack of selectivity can result in a saturation of the input receiver by an unwanted signal. However, when increasing the selectivity using an input filter, also the sensitivity will be increased by the reduction of the noise bandwidth of the amplifier. This, most likely, also goes at the cost of an increased power consumption and/or a decreased data rate. The implementation in [200] uses a BAW-filter in combination with an uncertain-IF topology to obtain the reported values. In [113], which has a high sensitivity and selectivity, an external SAW-filter is used. Also the two-tone modulation technique results in a high tolerance towards in-band interferers. Although in our application it can be assumed that the signal level of the RF power signal transcends any other interferers, at least a bandpass filter at the receiver input is needed to remove unwanted signals.

[7] The injection-locked receiver was mainly designed to receive short data bursts. When receiving a continuous data stream, the operation of the receiver can be affected by unwanted detection of phase steps being the result of frequency drift. This drift of the free-running frequency can be caused by a decreasing supply voltage or a changing temperature.

Table 7.4 Comparison of the injection-locked clock generators to the state of the art

Ref.	Tech. (μm)	Oscillator	f (MHz)	T sens. (ppm/°C)	V sens. (ppm/V)	P (μW)	V-range (V)	Rel. V-range (%)[a]	Trimming/ calibration
40 nm	0.04	Harmonic, RC	23–36	Lock	Lock	72	0.7–1.5	73	No, locked
130 nm	0.13	Harmonic, RC	950–1,150	Lock	Lock	127	0.7–1.6	78	No, locked
[56]	0.13	Pulsed harmonic	47.3	92	74	46	0.6–1.6	91	No
[192]	0.5	Relaxation, RC	12.8	625	5.3e3	>400	2.5–5.5	75	Yes
[178]	0.35	Harmonic, LC	12	12	38	31 mW	4.5–5.5	20	Yes

[a] $\Delta V_{rel} = 2 \cdot (V_{\max} - V_{\min})/(V_{\max} + V_{\min}) \cdot 100\,\%$

Table 7.5 Comparison of the receiver to the state of the art

	[199]	[28]	[113]	This work
Technology	90 nm CMOS	130 nm CMOS	90 nm CMOS	40 nm CMOS
Power	52 μW	37.5 μW	120 μW[a]	72 μW
Frequency	2 GHz	45 MHz	915 MHz	2.4 GHz
Data rate	100 kbit/s	200 kbit/s	10 kbit/s	1.8 Mbit/s
Sensitivity	−72 dBm	−62.7 dBm	−83 dBm	−43 dBm
BER	10^{-3}	–	10^{-3}	$<5 \times 10^{-3}$

[a]Power consumption of the external IF clock generator not included

7.6 Conclusion

In this chapter, two fully-integrated injection-locked oscillator topologies have been presented. By locking the oscillator to a wirelessly received RF signal, the different sensor nodes in the network can be synchronized exactly. The main difference between both implementations is the reduction of the power consumption by using the envelope of the injected signal instead of locking onto the carrier frequency itself. This results in a unique combination of low power and high accuracy. Apart from this, also an injection-locked coordination receiver has been developed. The 40 nm oscillator and receiver implementation is simulated to lock to a −43 dBm, 2.4 GHz RF signal. This signal strength is in the same order of magnitude as what is needed for an RF scavenging signal. The simulated lock range for a −39 dBm signal is 23 MHz to 36 MHz. The complete circuit, including the 1.8 Mbit/s coordination receiver, has a total power consumption of 72 μW and is designed to work from −20 to 100 °C and from 0.7 to 1.5 V. The circuit proves to be a very promising low-power solution for addressing, synchronization and coordination issues in wireless sensor networks.

Chapter 8
Oscillator-Based Sensor Interfaces

Nowadays sensors and feedback systems are used everywhere. One of the founding fathers of control theory is Cornelius Drebbel, a Dutch engravist, scientist and engineer. In the 1620s he described a 'circulating oven', which in fact is a thermostatic oven with automatic temperature control. In his description he mentions two important inventions, a 'judicium', what we nowadays call a thermometer, and a 'regimen', which is considered to be a control mechanism. His oven was used as an automatic breeder for chicken eggs. The term 'thermometer' appears the first time around 1624 in a French scientist's work. Afterwards, in a Latin translation of this work by Caspar Ens, the device is even called 'Instrumentum Drebilianum'. Although this is still under discussion, Drebbel is considered to be the inventor of the first human-made thermometer system [128].

8.1 Introduction

Apart from the oscillator circuitry, also sensor interfaces are suffering greatly from the unstable supply voltage and temperature variations. In this chapter it is shown that, by using a time ratio rather than an absolute time value, it is possible to implement an oscillator-based sensor interface independent from environmental parameters. Contrary to the previous oscillator implementations, it is no longer necessary to keep the frequency itself independent from the environment. By matching two oscillators or time delays, an input value can be sampled independently of external parameters. If the influence of temperature and voltage is identical for both circuits, the frequency drift is canceled out.

Two sensor interface topologies are presented: a PLL structure, which makes use of two matched oscillators, and a PWM-based structure, which relies on the matching between the stages in a ring oscillator. Both techniques can also be referred to as *closed-loop* and *open-loop* structures, respectively. In the next section, the PLL structure is presented. A more elaborate discussion on this topic can be

V. De Smedt et al., *Temperature- and Supply Voltage-Independent Time References for Wireless Sensor Networks*, Analog Circuits and Signal Processing 128,
DOI 10.1007/978-3-319-09003-0_8

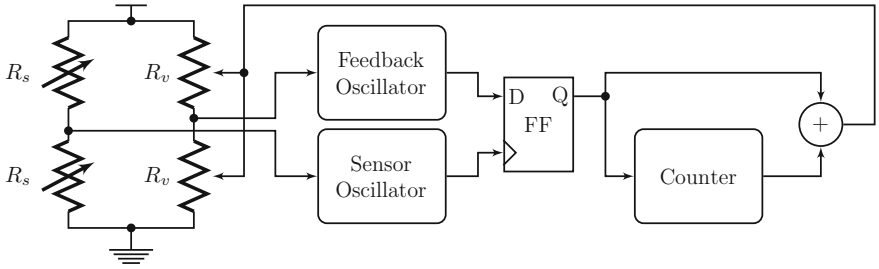

Fig. 8.1 Block diagram of a PLL-based sensor interface. The resistors R_s represent the sensor input, which is connected to an oscillator. Due to the phase detector and the digitally controlled feedback resistors R_v, both oscillator frequencies are matched

found in [43].[1] Afterwards, in Sect. 8.3, the PWM-based sensor interface is presented. The interface is based on a coupled sawtooth oscillator structure. Therefore, in Sect. 8.4, a noise analysis of this oscillator is performed to better understand the different design decisions and constraints. In Sect. 8.5, the two CMOS implementations in 130 and 40 nm are presented and compared. The measurement results of the sensor interface are presented in Sect. 8.5.3. Finally, in Sect. 8.6, conclusions are drawn.

8.2 PLL-Based Sensor Interfaces

A first method to obtain a sensor value independent of the supply voltage and the temperature is by integrating the sensor in one of the oscillators of a Phase-Locked Loop (PLL). A block diagram of such a PLL is shown in Fig. 8.1. When the sensor value (represented by the resistors R_s) changes, the frequency of the oscillator changes. However, due to the feedback mechanism of the PLL, the frequencies of both oscillators are re-aligned. This can either be done by tuning the second oscillator towards the frequency of the sensor oscillator or by compensating the influence of the sensor in the sensor oscillator. Typically, the feedback signal is implemented digitally, to obtain a digital version of the sensor signal. If both oscillators are matched properly, external parameters have an influence which is equal for both oscillators and have little or no influence on the output signal.

8.2.1 Implementation of the PLL

The architecture of the PLL-based sensor interface was first proposed in [279]. In this work a system study has been performed on the Bang-Bang PLL (BBPLL), a PLL using a (binary) quantized phase detector . The feasibility of the PLL has been

[1] This work has been done in collaboration with Hans Danneels and later also with Jelle Van Rethy.

demonstrated, using simulations in a 130 nm CMOS technology. A block diagram of this structure is shown in Fig. 8.1. It has been shown that, next to the integral feedback path (the counter), also a proportional path is needed in the feedback loop to obtain a stable PLL. Furthermore, the concept of course- and fine-tuning was introduced. First the counter takes large steps to quickly reach a course sensor value. When the loop is locked, the counter is switched to fine-tuning and an accurate sensor value can be obtained. Compared to a PLL using only fine-tuning, a speed increase up to a factor of 10 is reached for acquiring the first measured output sample. Such short startup time is important on a wireless tag, since the circuit is only active during a short burst period.

8.2.1.1 Second-Order PLL Implementation

In [263] and [264] a first implementation of a BBPLL-based sensor interface has been demonstrated. The implementation makes use of a ring oscillator using differential Maneatis delay cells [171]. This delay cell has important benefits in terms of dynamic supply noise and substrate noise rejection, due to its symmetrical load and biasing. Again, a proportional and an integral feedback path are implemented, which explains the name *second-order PLL*. The proportional path consists of the 1-bit phase detector output, which is directly connected to the oscillator load. The integral path, i.e. the output of the 8-bit counter, is fed back through a 5-bit R-2R digital-to-analog converter (DAC). The resolution of 8 bit is obtained by a PWM switching scheme of the 5-bit output. An important benefit of using a resistive sensor in combination with a matched output of the R-2R DAC, is the high power supply rejection ratio [264]. An output resolution of 8.9 effective number of bits has been obtained in this implementation, including nonlinearity.

8.2.1.2 First-Order PLL Implementation

In [45], a first-order BBPLL has been demonstrated. This means that the feedback loop only contains a 1-bit proportional path and that a PWM signal is obtained at the output. Both oscillators in this case are simple ring oscillators with capacitive loading. This results in an extremely low minimum supply voltage of 0.3 V, which corresponds to a power consumption of only 270 nW. Instead of using a resistive sensor, the interface is used to read out a capacitive pressure sensor. The 1-bit PWM output signal is fed back using a switched capacitor in the feedback oscillator, which causes both oscillators to lock. In [43] different other implementations of the BBPLL sensor interface structure have been discussed.

8.2.1.3 Performance of the BBPLL

An elaborate theoretical performance analysis on BBPLL-based sensor interfaces has been presented in [266]. It is shown that the performance of the digital output

is limited due to phase noise in the oscillator rather than quantization noise. Using oversampling, the output (noise) performance of the PLL can be increased up to resolutions of 18+ bits. The theoretical model derived in [266] has been applied to different configurations for different noise levels at the input, different oversampling ratios and different word lengths of the feedback counter. Also the impact of the stability factor (which has to do with the ratio of the proportional and the integral feedback path) on the output performance has been investigated.

In Table 8.5, where the performance of the developed PWM-based sensor interface is evaluated, also the results of several closed-loop PLL-based sensor interfaces can be found.

8.3 The PWM-Based Sensor Interface

The second method to obtain an output signal independent of external parameters, is by using a time ratio within the oscillator itself. This can be done, for instance, by building a ring oscillator of which the stage delay is modulated. When a differential sensor is used, each half of the stage delays is increased and decreased simultaneously. By using an output latch, a Pulse-Width-Modulated (PWM) signal can be extracted of which the duty cycle is a measure for the sensor value. A block diagram of this oscillator system is shown in Fig. 8.2. When an oscillator with a high control linearity is used, the output duty cycle is proportional to the sensor value. To obtain this, the coupled sawtooth oscillator [94] is used.

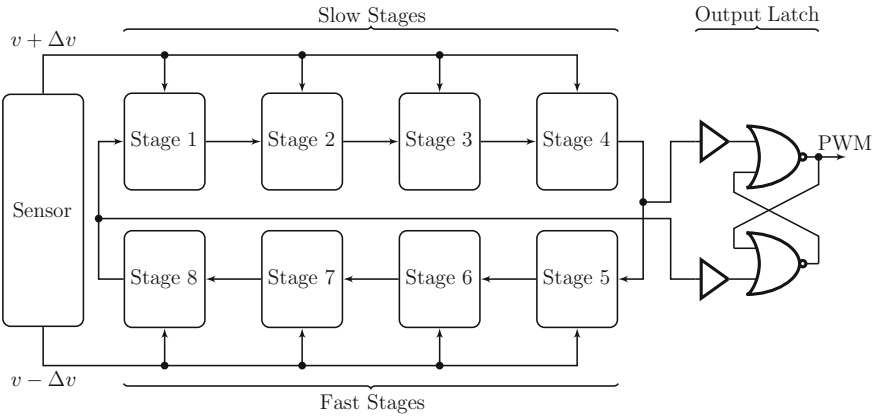

Fig. 8.2 Block diagram of the PWM-based sensor interface. Half of the oscillator stages are slowed down by the sensor signal, the other half is sped up. The output latch converts the oscillator signals into a PWM signal of which the duty cycle is proportional to the sensor value

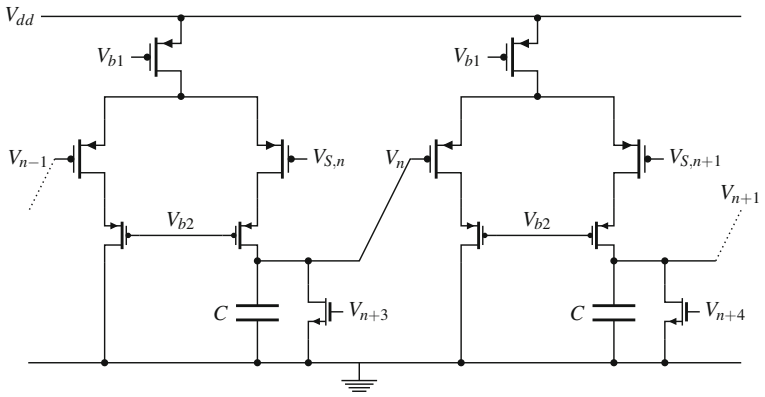

Fig. 8.3 Schematic of two oscillator stages and their interconnection. When a rising edge is applied to the input, the capacitor charges linearly and activates the next stage. The oscillator stage is reset by the output signal of stage $n + 3$. In this way, all internal control signals are generated by the oscillator itself

8.3.1 The Coupled Sawtooth Oscillator

The coupled sawtooth oscillator is a ring oscillator topology with a good phase noise performance compared to other relaxation oscillators [94]. Another benefit is the high control linearity, which is the main reason to use this oscillator in measuring applications. The oscillator in our design consists out of 8 differential stages. The schematic and interconnection of these differential stages is shown in Fig. 8.3. The delay of one stage is determined by the current through the current source I_b, the capacitor value C and the reference voltage V_S. This delay is given by:

$$T_D = \frac{V_S \cdot C}{I_b} \tag{8.1}$$

This formula is, however, only valid when the differential pair switches infinitely fast or when the switching of the differential pair is point-symmetric around its balance point (i.e. differential input equal to zero). The meaning of this is shown in Fig. 8.4. The dotted lines show the switching behavior of a differential pair with infinite gain. In this case the output current switches instantaneously from one branch to the other, linearly charging the capacitor. For a point-symmetric pair, switching smoothly over a certain input voltage span, the resulting delay stays exactly the same. The point-symmetry of the used differential pair can be proven by showing that the charging current only depends on the differential input voltage and not on the common-mode input voltage. Using the ideal MOSFET current Eq. (4.4.3), one can calculate the current through one branch of an ideal, symmetric CMOS differential pair:

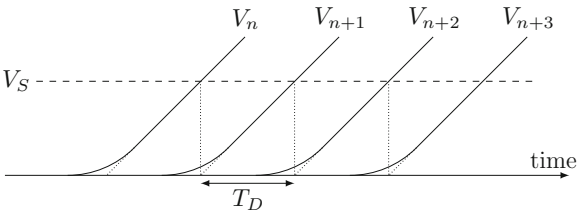

Fig. 8.4 Sketch of the output waveforms of subsequent oscillator stages. When using a CMOS differential pair, the switching delay when applying a linearly increasing input is exactly the same as in the case of an amplifier with an infinite gain. This is due to the point-symmetry of the differential pair

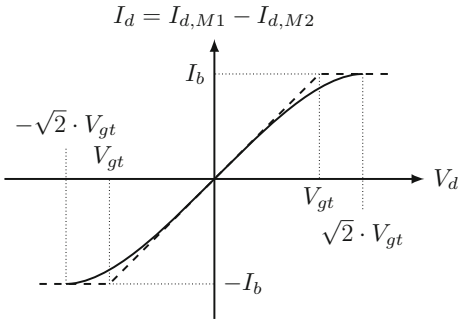

Fig. 8.5 Transfer characteristic of a differential oscillator stage. The characteristic is point-symmetric around $V_d = 0$. The linearized characteristic is shown as a *dashed line*

$$I_1 = \frac{1}{2} \cdot \left(I_b \pm V_d \cdot \sqrt{-k^2 \cdot \frac{W^2}{L^2} \cdot V_d^2 + 2 \cdot k \cdot \frac{W}{L} \cdot I_b} \right) \tag{8.2}$$

where I_b is the biasing current, $k = \frac{\mu_n \cdot C_{ox}}{2}$ and $V_d = V_+ - V_-$, the differential input voltage. For an increasing voltage V_{n-1} at the input, the negative sign is valid over the switching interval (output current from 0 to I_b). A plot of this transfer characteristic is shown in Fig. 8.5. Note that the behavior is perfectly symmetric around $V_d = 0$. This proves that the differential pair is point-symmetric and the average current during the switching period is equal to $I_b/2$ as long as a linearly increasing input voltage is applied at the input. When the switching operation is completed, the current charging the capacitor is equal to I_b. The time interval over which the switching operation is performed must always be smaller than the stage delay. If not, the successive switching operations overlap and the assumption of point-symmetry is no longer valid. This, in turn, has an impact on the control linearity of the stage delay. As will be seen in the next section, the slow switching has important benefits for improving the noise performance of the circuit.

The differential pair is, however, not ideal due to the asymmetric load and the limited output resistance of the current source. Therefore, to increase the output

resistance and to keep the charging current as constant as possible, cascode transistors are added. This, however, limits the low-voltage operation of the oscillator circuit.

8.3.2 Use in Combination with a Sensor

The coupled sawtooth oscillator is a highly-linear oscillator topology. This, in combination with the ratioed output signal, results in a high temperature and supply voltage independence. The sensor value itself, however, can also be affected by these external variations. Since the temperature effects are part of the sensor design, only the supply voltage dependency is discussed for two commonly used resistive sensor configurations.

8.3.2.1 Using a Wheatstone Bridge

A typical resistive sensor is used in the form of a Wheatstone bridge. A schematic of such a sensor is shown in Fig. 8.6. Two configurations are shown: one with a current source on top, the other with a voltage source. In case of the current source, when the applied current is equal or proportional to I_b, the biasing current of the oscillator, it is easy to see that the oscillation frequency becomes independent of this current. The output voltages of the Wheatstone bridge are given by:

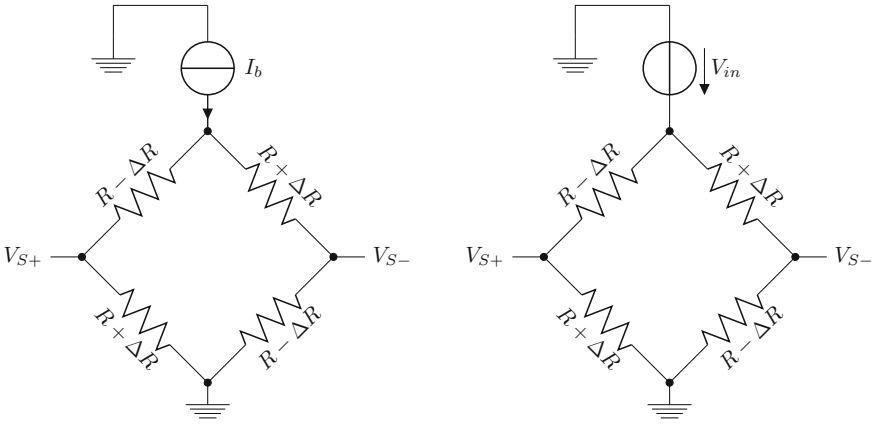

Fig. 8.6 Two configurations of a Wheatstone bridge: one with a current source on *top*, the other connected to an input voltage source

$$V_{S+} = V_{in} \cdot \frac{R + \Delta R}{2 \cdot R} \tag{8.3}$$

$$V_{S-} = V_{in} \cdot \frac{R - \Delta R}{2 \cdot R} \tag{8.4}$$

When inserting these voltages into (8.1), the stage delay of respectively a slow and a fast stage becomes:

$$T_{S+} = \frac{V_{in} \cdot (R + \Delta R) \cdot C}{2 \cdot R \cdot I_b} \tag{8.5}$$

$$T_{S-} = \frac{V_{in} \cdot (R - \Delta R) \cdot C}{2 \cdot R \cdot I_b} \tag{8.6}$$

Which results in a duty cycle of:

$$DC = \frac{T_{stage1-4}}{T_{Osc}} = \frac{R + \Delta R}{2 \cdot R} \tag{8.7}$$

This expression is completely independent of the voltage (or current) applied to the Wheatstone bridge which is a consequence of the linearity of the sensor interface. In the presented design, the external sensor resistors are biased by a replica of the oscillator stages' current source.

8.3.2.2 Use with a Single-Ended Sensor

When the Interface is used in combination with a single-ended sensor, a similar calculation can be made. The two input signals are then equal to:

$$V_{S+} = V_{in} \cdot \frac{R + \Delta R}{2 \cdot R} \tag{8.8}$$

$$V_{S-} = V_{Cte} \tag{8.9}$$

where V_{Cte} is an arbitrary voltage, preferably equal to the zero-input sensor voltage. When converting this into a duty cycle, it is observed that the sensitivity of the interface is divided by two and the frequency becomes dependent on the sensor value:

$$DC = \frac{R + \Delta R}{2 \cdot R + \Delta R} \tag{8.10}$$

Furthermore, it is crucial that the voltage V_{Cte} is proportional to V_{in} to make the output independent of the voltage or current applied to the sensor branch. Measurements show an increased nonlinearity in the case of a single-ended input signal. Furthermore, also the noise performance and the sample frequency are affected by the use of a single-ended sensor (see Sect. 8.4).

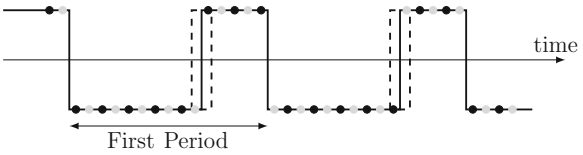

Fig. 8.7 The sampling of the oscillator output signal when the duty cycle is equal to 1/3. If only the *black samples* are taken into account, the samples need to be averaged over several periods. However, when the sampling speed is higher (*all samples*), only the first period is enough to obtain the right duty cycle. This shows the trade-off between the sampling speed and the bandwidth

8.3.3 Transmission of the Output Signal

The sensor interface is designed to create a transmittable signal from an analog sensor input. In order to transmit the PWM signal wirelessly, it needs to be sampled. Since the sensor interface translates all the amplitude information from the sensor into time information, the PWM signal has a timing resolution which is much higher than the oscillator frequency. However, since the sampled signal can be averaged over several oscillator periods, the sampling frequency can be lower than the Nyquist frequency of the PWM signal. Instead, it determines the bandwidth (or Nyquist rate) of the output signal. The upper limit of the output bandwidth is of course determined by the oscillator speed. This is shown in Fig. 8.7. Even if the output is sampled at a rate far below the oscillator speed, on the long term, the averaged duty cycle of the sampled signal is equal to the duty cycle of the sensor interface. Roughly speaking, it can be stated that for a certain modulation depth and a certain sampling accuracy, the ratio of the sampling speed and the resulting bandwidth is constant. Even if a supply voltage or temperature change is applied during the period over which the output signal is sampled, the influence on the output value lowers when the number of averaged PWM periods increases. In this way, the influence of external parameters can be lowered, be it at the cost of bandwidth. It should be noted that this reasoning is only valid when the sample frequency is uncorrelated with or floating compared to the oscillator frequency.

To give an example of the required sampling speed, it is assumed that a 50 MHz sampling clock is used. When the variation of the duty cycle is around $\pm 16\,\%$, the oscillation period of the interface is 500 ns and the required accuracy is around 8 bits, then a resolution of at least 80 ns/256 is required. This results in a needed sampling accuracy of 0.31 ns. When sampling at 50 MHz, around 64 periods of the sensor interface are needed to obtain an accurate sampled value. Although the 50 MHz oscillator does not have any accuracy requirements, it does consume some extra energy. A factor 100 (instead of 64) is used to take the extra power consumption of the sampling oscillator into account. From the measured data of the 40 nm implementation it can be calculated that this corresponds to a 10 μW 50 MHz sampling clock, which is reasonable in the used technology. The results of this estimation are used when comparing the interface to the state of the art (Sect. 8.5.3).

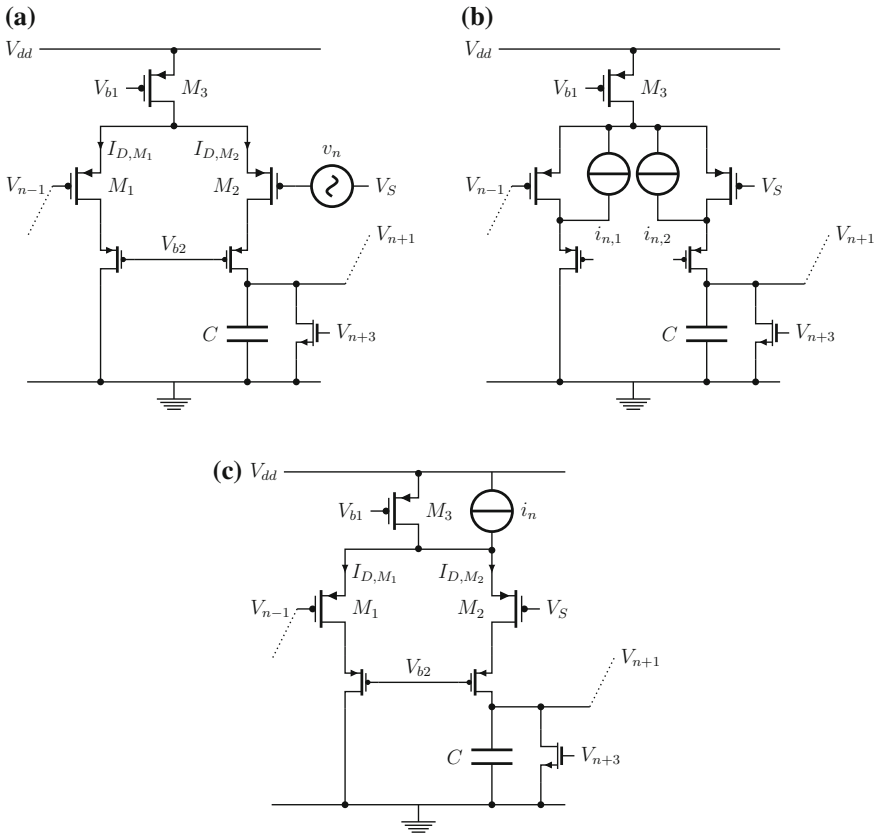

Fig. 8.8 Simplified schematic of the different noise contributions: **a** noise in the reference voltage V_S; **b** noise in the differential pair; **c** noise in the current source

8.4 Jitter in the Coupled Sawtooth Oscillator

As in every circuit, different noise sources are present. These sources can have an impact on for instance the exact switching moment, which causes jitter in the output waveform. Since the output sensor value is determined by the edges of the oscillator, this jitter also has an impact on the output noise of the converted sensor signal. The different noise sources are identified as (see Fig. 8.8):

- Voltage noise in series with the reference voltage V_S (sensor noise)
- Noise in the differential pair
- Current noise in parallel with the bias current I_b

In a first step, the resulting jitter of the different noise sources will be discussed. Afterwards, the impact on the output sensor signal will be calculated. Important to note is that the focus in this noise analysis is on uncorrelated (white) noise. The first

reason to do so is the fact that, when designed properly, the main part of the injected noise is white noise. Furthermore, since the current source in every stage copies its current from one common biasing circuit, a correlation exists between the noise on V_S and I_b in the different stages. As a result, the low-frequency noise coming from these sources has no, or very little, impact on the output noise of the sensor interface. Indeed, after each oscillation period the duty cycle of the output signal is measured, i.e. *the on-period of the output signal is compared to the oscillation period itself*. Due to this operation, the common low-frequency noise component is canceled out. This, however, does not hold for the noise generated by the current sources (M_3) themselves. In both technologies a sufficiently large current source is assumed to diminish this low-frequency noise. Furthermore, as will be explained in Sect. 8.5.2.1, a current switching technique is included in the 40 nm implementation, which also reduces the low-frequency noise in the current sources. Therefore, and for the sake of better understanding, only white noise is taken into account to calculate the cycle-to-cycle jitter (Definition 3.2). The conclusions from this discussion will be used when designing both implementations of the sensor interface.

8.4.1 Jitter due to Sensor Noise

The delay of each oscillator stage in the coupled sawtooth oscillator is determined by the reference voltage, which, in this case, is the sensor output signal. This noise source is shown in Fig. 8.8a. As a result, the sensor noise is directly visible in the oscillator's output signal. Note that, although this calculation is necessary to investigate the noise propagation in the circuit, this noise is not caused by the design of the interface itself. To slightly simplify the noise calculation, a linearized transfer characteristic of the differential pair is used (see Fig. 8.5):

$$\begin{cases} I_d = -I_b & V_d \leq -V_{gt} \\ I_d = g_m \cdot V_d & -V_{gt} \leq V_d \leq V_{gt} \\ I_d = I_b & V_d \geq V_{gt} \end{cases} \tag{8.11}$$

where $V_{gt} = V_{gs} - V_{th}$ and g_m is the transconductance of the differential pair (at $V_D = 0$), equal to I_b / V_{gt}.

8.4.1.1 Relationship Between Voltage Noise and Jitter

During the switching operation, it is the transconductance g_m which determines the propagation of the input noise to the output current (i.e. the charging current of the capacitor):

$$i_{d,n} = v_n \cdot g_m \tag{8.12}$$

This noisy current causes an uncertainty on the capacitor voltage ΔV_n, which results in a time error ΔT_n at the output of the oscillator stage. The relation between both depends on the output slope of the oscillator stage:

$$Slope = \frac{I_b}{C} = \frac{V_S}{T_{Osc}/n} \tag{8.13}$$

where I_b is the charging current and an n-stage oscillator is assumed. Next, also the so-called *first crossing approximation* is used: it is assumed that the delay of a stage lasts until the moment it crosses the (noisy) reference level of the next stage [92]. This means that the time error, caused by an oscillator stage, is related to the voltage error by:

$$\Delta T_n = \frac{\Delta V_n}{Slope} = \frac{\Delta V_n \cdot C}{I_b} \tag{8.14}$$

or, when calculating the variance of the resulting jitter:

$$\sigma^2_{T_n} = \frac{\sigma^2_{V_n} \cdot C^2}{I_b^2} \tag{8.15}$$

8.4.1.2 Calculating the Voltage Noise ΔV_n

Using the linearized differential-pair model, the time over which the differential pair is switching can easily be calculated. This time is equal to the time during which the input signal (which is the output signal of the previous stage) lies within the $\pm V_{gt}$ input interval. Using the expression for the output slope of the previous stage, the switching time is calculated to be :

$$T_{switch} = \frac{2 \cdot V_{gt}}{I_b/C} = \frac{2 \cdot C}{g_m} \tag{8.16}$$

The voltage uncertainty at the output of an oscillator stage due to a noise signal v_n at the reference input is equal to a filtered noise voltage:

$$\Delta V_n = \frac{1}{C} \int_{T_{Switch}} \frac{i_{d,n}(t)}{2} dt \tag{8.17}$$

$$= \frac{1}{T_{Switch}} \int_{T_{Switch}} v_n(t) dt \tag{8.18}$$

From this, the variance of the input voltage can also be calculated, based on its frequency spectrum. Similarly to the calculation of the cycle-to-cycle jitter in C.1.1 and Sect. 3.6, the output noise voltage of an oscillator stage can be written as a

moving average:

$$\Delta V_n(t) = \frac{1}{C} \int_{t-T_{Switch}/2}^{t+T_{Switch}/2} \frac{i_{d,n}(t)}{2} dt \tag{8.19}$$

which is equal to the convolution:

$$\Delta V_n(t) = \frac{1}{C} \int_{-\infty}^{\infty} \frac{i_{d,n}(p)}{2} \cdot \Pi\left(\frac{t-p}{T_{Switch}}\right) dp \tag{8.20}$$

where $\Pi(x)$ is the rectangular function. In the frequency domain, this equation can be written as:

$$S_{V_n}(f) = \frac{1}{4 \cdot C^2} \cdot S_{i_{d,n}}(f) \cdot \left[T_{Switch} \cdot \text{sinc}(\pi \cdot T_{Switch} \cdot f)\right]^2 \tag{8.21}$$

$$= \frac{g_m^2}{4 \cdot C^2} \cdot S_{v_n}(f) \cdot \left[T_{Switch} \cdot \text{sinc}(\pi \cdot T_{Switch} \cdot f)\right]^2 \tag{8.22}$$

where $S_{V_n}(f)$ is the PSD of the output (noise) voltage V_n and $S_{v_n}(f)$ is the PSD of the input noise source v_n. If $S_{v_n}(f)$ is a white and single-sided spectrum with an unlimited bandwidth and low-frequency value S_{v_n}, the variance of the output voltage is calculated as:

$$\sigma_{V_n}^2 = \frac{S_{v_n} \cdot g_m^2}{4 \cdot C^2} \int_0^{\infty} \left[T_{Switch} \cdot \text{sinc}(\pi \cdot T_{Switch} \cdot f)\right]^2 df \tag{8.23}$$

$$= \frac{S_{v_n} \cdot g_m^2}{8 \cdot C^2} \cdot T_{Switch} \tag{8.24}$$

Using (8.16) to substitute for g_m, this reduces to:

$$\sigma_{V_n}^2 = \frac{S_{v_n}}{2 \cdot T_{Switch}} \tag{8.25}$$

It is clear that, due to the averaging of the noise over the switching interval, the resulting jitter on the clock edge at the output of each stage is lower than in the case of an infinitely fast switching oscillator stage. The effective bandwidth over which the input noise of the reference voltage contributes to the output noise, is equal to $1/(2 \cdot T_{Switch})$, which is a motivation to make the switching interval as large as possible (i.e. as long as it does not interfere between the subsequent oscillator stages).

Since the switching interval of the subsequent stages is non-overlapping, and only the white noise at the input is considered here, the time variance of the different stages

can be added. Using the relation between the time and the voltage uncertainty (8.15), the timing jitter is written as:

$$\sigma_{T_n}^2 = \frac{1}{n^2} \cdot \frac{S_{v_n} \cdot T_{Osc}^2}{2 \cdot T_{Switch} \cdot V_S^2} \tag{8.26}$$

The variance of the oscillator period is then equal to:

$$\sigma_{T_{Osc}}^2 = n \cdot \sigma_{T_n}^2 = \frac{1}{n} \cdot \frac{S_{v_n} \cdot T_{Osc}^2}{2 \cdot T_{Switch} \cdot V_S^2} \tag{8.27}$$

Since the best results can be obtained when T_{Switch} is equal to one stage delay, it is often assumed to be T_{Osc}/n. In this optimal case, the number of stages has no impact on the jitter:

$$\left(\frac{\sigma_{T_{Osc}}}{T_{Osc}}\right) = \frac{\sqrt{\frac{S_{v_n}}{2} \cdot f_{Osc}}}{V_S} \tag{8.28}$$

However, it is hardly possible to design the switching interval of the differential pair towards this ideal situation. Therefore, expression (8.27) is mostly used.

8.4.2 Jitter from the Differential Pair

Also the differential pair causes jitter in the output signal. This is modeled by a noise current source between the source and the drain of each transistor in the differential pair (Fig. 8.8b). Again, the noise current is integrated as long as the differential pair is switching. When the switching operation is completed, $i_{n,1}$ is equal to zero and the current from $i_{n,2}$ is completely absorbed by the right-hand-side transistor which acts as a cascode. The linearized characteristic of the differential pair is used to calculate the impact of the noise sources. The current noise sources of both differential transistors are equal to (3.7)–(3.9), when only considering the channel noise:

$$S_{i_{n,1}} = 8/3 \cdot k \cdot T \cdot g_{m,1}(V_d) \tag{8.29}$$

$$S_{i_{n,2}} = 8/3 \cdot k \cdot T \cdot g_{m,2}(V_d) \tag{8.30}$$

where $g_{m,1}$ and $g_{m,2}$ are the transconductance of M_1 and M_2 respectively.[2] The contribution of both noise currents can be calculated to be:

[2] In [92] another noise model is used, in which $S_{i_n} = 4 \cdot k \cdot T \cdot g_m$. The resulting formulas can easily be adapted depending on the noise model and/or technology.

$$S_{i_n}(V_d) = S_{i_{n,1}} \cdot \left(\frac{g_{m,2}(V_d)}{g_{m,1}(V_d) + g_{m,2}(V_d)} \right)^2 + S_{i_{n,2}} \cdot \left(\frac{g_{m,1}(V_d)}{g_{m,1}(V_d) + g_{m,2}(V_d)} \right)^2 \tag{8.31}$$

$$= 8/3 \cdot k \cdot T \cdot \frac{g_{m,1}(V_d) \cdot g_{m,2}(V_d)}{g_{m,1}(V_d) + g_{m,2}(V_d)} \tag{8.32}$$

$$= 8/3 \cdot k \cdot T \cdot \frac{1}{2} \cdot g_m(V_d) \tag{8.33}$$

where $g_m(V_d)$ is the resulting transconductance of the differential pair (this can be understood when noting that the ratio of the transconductances is the expression for 2 resistors in parallel). The resulting transconductance is assumed to be constant over V_d, which makes:

$$S_{i_n}(V_d) = 8/3 \cdot k \cdot T \cdot \frac{1}{2} \cdot g_m \tag{8.34}$$

Note that the current i_n flowing into the capacitor is equal to half of the noise current in the differential transistors:

$$i_n = 0.5 \cdot i_{d,n} = 0.5 \cdot g_m \cdot v_{d,n} \tag{8.35}$$

which shows that the noise of the differential pair can be expressed as an input voltage noise source. Therefore, the same expression for the variance of the output voltage is valid as in the previous case of the reference voltage noise:

$$\sigma^2_{V_n} = \frac{S_{v_n} \cdot g_m^2}{8 \cdot C^2} \cdot T_{Switch} \tag{8.36}$$

$$= \frac{S_{i_n}}{2 \cdot C^2} \cdot T_{Switch} \tag{8.37}$$

$$= \frac{2 \cdot k \cdot T \cdot g_m}{3 \cdot C^2} \cdot T_{Switch} \tag{8.38}$$

$$= \frac{4 \cdot k \cdot T}{3 \cdot C} \tag{8.39}$$

where the last step makes use of (8.16). Similar to (8.27) the expression for the variance of the period of an n-stage oscillator of which all differential stages produce uncorrelated white noise, is equal to:

$$\sigma^2_{T_{Osc}} = n \cdot \sigma^2_{T_n} = \frac{1}{n} \cdot \frac{8 \cdot k \cdot T \cdot T^2_{Osc}}{3 \cdot g_m \cdot T_{Switch} \cdot V_S^2} \tag{8.40}$$

$$= \frac{1}{n} \cdot \frac{\frac{4 \cdot k \cdot T}{3 \cdot C} \cdot T^2_{Osc}}{V_S^2} \tag{8.41}$$

where (8.41), again, can be further simplified for an optimal switching interval, uses (8.16) and V_S is the sensor voltage.

8.4.3 Jitter due to the Current Source

When a noise source is present in parallel with the current source on top of each oscillator stage, this will also have an impact on the timing of the stage's output signal (Fig. 8.8c). This noise source can be analyzed in a similar way as in the case where the noise is coming from the reference voltage. At the moment, it is, however, assumed that the switching of each stage happens immediately. Again, the first crossing approximation is used. When the capacitor voltage crosses the reference voltage of the next stage for the first time, the next stage switches irreversibly and charges its capacitor. The integrated noise results in this case in:

$$\sigma_{V_n}^2 = \frac{S_{i_n}}{2 \cdot C^2} \cdot T_{Charge} \tag{8.42}$$

Important to note is the difference with the previous case, where the noise was integrated over the switching interval instead of the charging interval. The variance of the time error is calculated to be:

$$\sigma_{T_n}^2 = \frac{\sigma_{V_n}^2}{(I_d/C)^2} \tag{8.43}$$

$$= \frac{S_{i_n}}{2} \cdot \frac{T_{Charge}}{I_b^2} \tag{8.44}$$

$$= \frac{S_{i_n}}{2 \cdot n} \cdot \frac{T_{Osc}}{I_b^2} \tag{8.45}$$

Since only white noise is considered, the noise added in the subsequent oscillator stages is independent. The noise on the oscillator period results in:

$$\sigma_{T_{Osc}}^2 = n \cdot \sigma_{T_n}^2 = \frac{S_{i_n}}{2} \cdot \frac{T_{Osc}}{I_b^2} \tag{8.46}$$

However, the slow switching of the subsequent stages also has an impact on the resulting output noise. First of all, the noise of the ith stage propagates to the $i+1$th stage during the switching operation. Secondly, also the noise of the $i+1$th stage is visible at its output. In [92] an elaborate and more exact calculation is conducted to obtain the resulting timing jitter of the oscillator stage. For an oscillator in which the switching interval is maximum and equal to the stage delay, this results in the following expression:

$$\sigma^2_{T_{Osc}} = \frac{S_{i_n}}{3} \cdot \frac{T_{Osc}}{I_b^2} \tag{8.47}$$

As can be seen, the impact of the slow switching is only minor compared to its impact in the previous cases (factor 3 instead of factor 2). Since the switching interval is difficult accurately at design time, (8.46) can best be used.

8.4.4 Noise Propagation to the Sensor Interface Output

The duty cycle of the sensor output is a measure for the sensor value. As a result, it is not only the jitter on the entire oscillation period which is visible in the output signal, but also the jitter on half the oscillation period. The jitter on both these measures is correlated which makes the calculation of the output jitter a more complex problem. This is shown in Fig. 8.9. The period of respectively the high and low phase of the output signal can be written as the sum of its ideal value and a random jitter component:

$$T_h = T_{h,0} + \Delta T_{h,n} \tag{8.48}$$

$$T_l = T_{l,0} + \Delta T_{l,n} \tag{8.49}$$

The oscillation period, as shown in Fig. 8.9, is the sum of both values. From the previous discussion an estimate value of the standard deviation σ_h and σ_l of both half-periods is known. The question is now how these values propagate to the sensor output value:

$$V_{out} = \frac{T_h}{T_h + T_l} = \frac{T_{h,0} + \Delta T_{h,n}}{T_{h,0} + \Delta T_{h,n} + T_{l,0} + \Delta T_{l,n}} = f(T_h, T_l) \tag{8.50}$$

In [85] this topic has elaborately been investigated. Formulas have been derived for the standard deviation of the product of two stochastic variables as well as for ratios. It is, however, necessary to have some information about the distribution of these variables to obtain the correct results. For example, a normal distribution, which is commonly assumed for the sake of simplicity, does not have any zeros. This results in convergence problems when calculating the distribution and standard deviation of

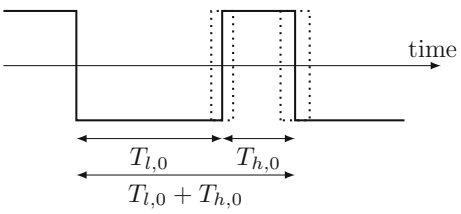

Fig. 8.9 The jitter on the complete oscillator period ($T_{l,0} + T_{h,0}$) as well as the jitter on half the oscillation period ($T_{l,0}$ or $T_{h,0}$) are present in the interface's output signal

the inverse of a normally distributed stochastic variable. Therefore, a linear approach is taken. For a generic function $f(T_h, T_l)$ of two stochastic variables with standard deviation σ_h and σ_l, the variance can be approximated to be:

$$\sigma_V^2 = E\left[(V_{out} - E(V_{out}))^2\right] \tag{8.51}$$

$$= E\left[\left(f(T_h, T_l) - E(f(T_h, T_l))\right)^2\right] \tag{8.52}$$

$$\approx E\Bigg[\Bigg(f(T_{h,0}, T_{l,0}) + \frac{\partial f(T_{h,0}, T_{l,0})}{\partial T_h} \cdot \Delta T_{h,n} + \frac{\partial f(T_{h,0}, T_{l,0})}{\partial T_l} \cdot \Delta T_{l,n} - E(f(T_h, T_l))\Bigg)^2\Bigg] \tag{8.53}$$

$$= E\left[\left(\frac{\partial f(T_{h,0}, T_{l,0})}{\partial T_h} \cdot \Delta T_{h,n} + \frac{\partial f(T_{h,0}, T_{l,0})}{\partial T_l} \cdot \Delta T_{l,n}\right)^2\right] \tag{8.54}$$

$$= E\Bigg[\left(\frac{\partial f(T_{h,0}, T_{l,0})}{\partial T_h}\right)^2 \cdot \Delta T_{h,n}^2 + \left(\frac{\partial f(T_{h,0}, T_{l,0})}{\partial T_l}\right)^2 \cdot \Delta T_{l,n}^2 + 2 \cdot \frac{\partial f(T_{h,0}, T_{l,0})}{\partial T_h} \cdot \frac{\partial f(T_{h,0}, T_{l,0})}{\partial T_h} \cdot \Delta T_{h,n} \cdot \Delta T_{l,n}\Bigg] \tag{8.55}$$

$$= \left(\frac{\partial f(T_{h,0}, T_{l,0})}{\partial T_h}\right)^2 \cdot E(\Delta T_{h,n}^2) + \left(\frac{\partial f(T_{h,0}, T_{l,0})}{\partial T_l}\right)^2 \cdot E(\Delta T_{l,n}^2) + 2 \cdot \frac{\partial f(T_{h,0}, T_{l,0})}{\partial T_h} \cdot \frac{\partial f(T_{h,0}, T_{l,0})}{\partial T_h} \cdot E(\Delta T_{h,n} \cdot \Delta T_{l,n}) \tag{8.56}$$

$$= \left(\frac{\partial f(T_{h,0}, T_{l,0})}{\partial T_h}\right)^2 \cdot \sigma_h^2 + \left(\frac{\partial f(T_{h,0}, T_{l,0})}{\partial T_l}\right)^2 \cdot \sigma_l^2 + 2 \cdot \frac{\partial f(T_{h,0}, T_{l,0})}{\partial T_h} \cdot \frac{\partial f(T_{h,0}, T_{l,0})}{\partial T_h} \cdot \sigma(T_h, T_l) \tag{8.57}$$

Since only white noise is considered and there is no overlap between the two half periods T_h and T_l, the covariance between both values is equal to zero. Therefore:

$$\sigma_V^2 \approx \left(\frac{\partial f(T_{h,0}, T_{l,0})}{\partial T_h}\right)^2 \cdot \sigma_h^2 + \left(\frac{\partial f(T_{h,0}, T_{l,0})}{\partial T_l}\right)^2 \cdot \sigma_l^2 \tag{8.58}$$

Applying this to the sensor interface for which:

$$f(T_h, T_l) = \frac{T_h}{T_h + T_l} \tag{8.59}$$

results in:

$$\sigma_V^2 \approx \left(\frac{T_l}{(T_h + T_l)^2}\right)^2 \cdot \sigma_h^2 + \left(\frac{-T_h}{(T_h + T_l)^2}\right)^2 \cdot \sigma_l^2 \tag{8.60}$$

which makes it possible to calculate the jitter in the output signal.

8.4.4.1 Impact of the Sensor Value

In a next step, it is interesting to investigate the impact of the sensor input on the noise of the output signal. From the previous discussion it appears that, except for the noise from the current source, the noise sources are not affected by the sensor input. Since the charging current in each stage is not modulated, the output slope of each stage also stays constant. Only the stage delay, which is decreased and increased, puts a limit on the switching period of the oscillator stages. The more the sensor input can vary, the shorter the switching period must be in order to prevent the switching operation from overlapping between the subsequent stages. Although the modulation depth needs to be taken into account at design time, it is constant for a certain design. The standard deviation of T_h and T_l therefore only weakly depends on the sensor input value. The noise propagation, on the other hand, is affected by the sensor value. For an ideal control linearity, and using a perfectly differential sensor, it can be assumed that:

$$\Delta T_h = -\Delta T_l \tag{8.61}$$

This also means that the oscillator frequency is independent of the sensor input. Using (8.60), Fig. 8.10 shows the output noise for a constant input noise source as a function of the sensor input value. When the sensor is single-ended, ΔT_l is equal to zero. The noise propagation in this case is slightly different. The fact that the noise

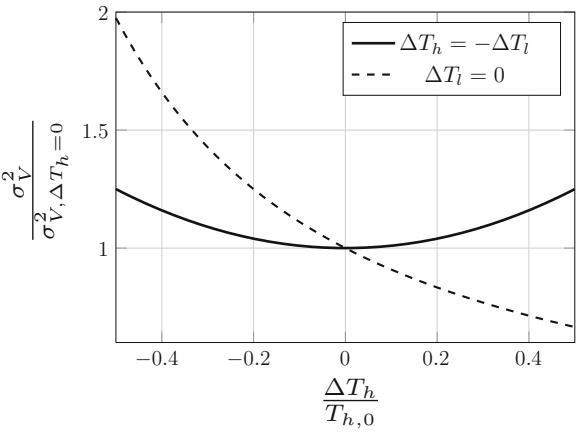

Fig. 8.10 Normalized jitter (compared to the noise for a zero-input signal) of the output duty cycle as a function of the varying sensor input. The *solid line* uses a differential sensor; the *dashed line* is for a single-ended sensor. The noise sources themselves are constant; the variation is caused by the input–output transfer characteristic of the noise

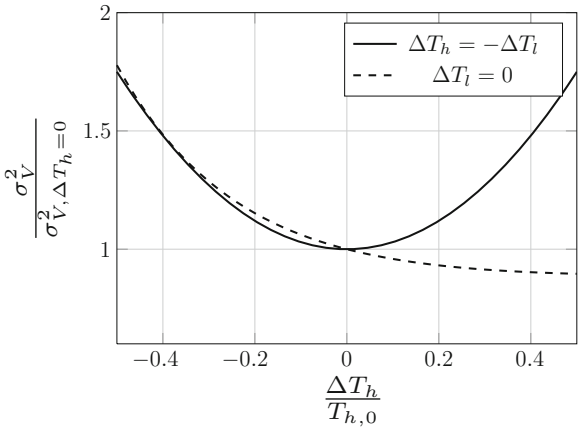

Fig. 8.11 The normalized jitter (compared to the noise for a zero-input signal) of the output duty cycle as a function of the varying sensor input for the noise generated by the current source. The variance of the noise increases linearly with the stage delay. The *solid line* uses a differential sensor; the *dashed line* is for a single-ended sensor

lowers for high values of ΔT_h is because the oscillation period becomes longer. In turn for the better noise performance this, however, makes the sensor interface to become slower. A separate graph is shown for the noise generated in the current source, Fig. 8.11. The variance of the jitter on T_l and T_h caused by the current source increases linearly with the stage delay.

8.4.4.2 Colored Noise Propagation

When colored noise is injected in the oscillator, the variance can no longer be used as a noise measure (Sect. 3.6.3). Due to the correlation between the subsequent errors on the output value, this measure will diverge and it will be strongly dependent on the measuring interval. In Appendix C.2.1 different methods are presented to detrend the measured values to obtain a convergent noise measure (which eventually can also be linked to a frequency spectrum). For $1/f$ noise, this can be done using the Allan variance (or a second-order structure function). Similar to (8.60) a formula can be derived to calculate the colored noise propagation in the system, using the Allan variance (Appendix C, [5]):

$$\begin{aligned}\sigma_{A,f,\tau} &= \frac{1}{2}\cdot E\left[\left[f(T_h(t+\tau),T_l(t+\tau)) - f(T_h(t),T_l(t))\right]^2\right] \\ &= \frac{1}{2}\cdot E\left[\left(\frac{\partial f(T_{h,0},T_{l,0})}{\partial T_h}\right)^2\cdot(\Delta T_{h,n,t+\tau} - \Delta T_{h,n,t})^2\right. \\ &\quad \left.+\left(\frac{\partial f(T_{h,0},T_{l,0})}{\partial T_l}\right)^2\cdot(\Delta T_{l,n,t+\tau} - \Delta T_{l,n,t})^2\right.\end{aligned} \tag{8.62}$$

$$+\frac{\partial f(T_{h,0},T_{l,0})}{\partial T_h}\cdot\frac{\partial f(T_{h,0},T_{l,0})}{\partial T_l}$$
$$\cdot(\Delta T_{h,n,t+\tau}-\Delta T_{h,n,t})\cdot(\Delta T_{l,n,t+\tau}-\Delta T_{l,n,t})\Big] \tag{8.63}$$
$$=\left(\frac{\partial f(T_{h,0},T_{l,0})}{\partial T_h}\right)^2\cdot\sigma_{A,h}^2+\left(\frac{\partial f(T_{h,0},T_{l,0})}{\partial T_l}\right)^2\cdot\sigma_{A,l}^2$$
$$+\frac{\partial f(T_{h,0},T_{l,0})}{\partial T_h}\cdot\frac{\partial f(T_{h,0},T_{l,0})}{\partial T_l}\cdot\sigma_{A,h,l} \tag{8.64}$$

where $\sigma_{A,h}$ and $\sigma_{A,h}$ are the Allan variance of T_h and T_l respectively and $\sigma_{A,h,l}$ is called the Allan covariance [87]. Part of the colored noise sources are different in all oscillator stages; others are common, for instance part of the noise added by the current source. The fact that the periods T_h and T_l are non-overlapping does not mean that the Allan covariance $\sigma_{A,h,l}$ equals zero as was previously the case when assuming only white noise! Indeed, since the colored noise is correlated over time due to the high low-frequency content, ΔT_l and ΔT_h are also correlated. Without proof, it can therefore be seen that this correlation of the low-frequency noise decreases the output noise of the sensor interface.

For higher-order colored noise injections, similar conclusions can be drawn using a higher-order structure function (Sect. C.2.3). These structure functions detrend the correlation between the subsequent samples to obtain a convergent noise measure. As shown in Appendix C.2.3, the Allan variance and the variance of the structure functions can be linked to the noise spectrum.

8.4.5 A/D-Converter FoM

Similar to the FoMs used for oscillator circuits (Sect. 4.3), another FoM exist to characterize the performance of an A/D converter. The formula takes the Signal to Noise and Distortion Ratio (SNDR) in dB of the output signal into account by calculating the effective number of bits (ENOB):

$$ENOB=\frac{SNDR-1.76}{6.02} \tag{8.65}$$

To obtain a FoM, this value is compared to the sampling frequency and the power consumption [280]:

$$FoM_{AD}=\frac{P}{f_s\cdot 2^{ENOB}} \tag{8.66}$$

This FoM will be used in the remainder of this chapter to characterize and compare the designed sensor interfaces.

8.4.5.1 Impact on the Design of the Sensor Interface

From the previous analysis, different conclusions can be drawn concerning the design of the sensor interface. First of all, it has been shown that the switching time T_{Switch} needs to be as large as possible to diminish the noise coming from the differential pair and the sensor voltage. Increasing this time interval, decreases the effective noise bandwidth (8.25) and therefore reduces the noise in the interface output signal. The problem of increasing T_{Switch}, however, is the fact that the switching intervals of subsequent oscillator stages must not overlap when a high control linearity is required, as is the case in a highly-linear sensor interface. This clearly shows the trade-off between the linearity and the output noise of the sensor interface.

Secondly, the input signal has an impact on the noise of the current source and, more importantly, also on the noise propagation to the output. It was shown that, for a differential sensor, the noise propagation reaches a minimum around the sensor's equilibrium point. When a single-ended sensor is used, the output jitter is also affected by the changing oscillator period; when the oscillator slows down, the jitter decreases.

Relating to the colored noise sources it was shown that the correlation of the low-frequency noise between the different stages results in a decrease of the noise propagation to the output. The uncorrelated colored noise sources (such as the current source M_3), however, need special attention since they directly appear at the output. The current source therefore preferably is a large transistor. Current switching techniques can be used to reduce the $1/f$ noise generated by these transistors, see Sect. 8.5.2.1.

8.5 Implementation of the Sensor Interface

The PWM-based sensor interface, has been implemented in a 130 nm CMOS technology as well as in a 40 nm CMOS technology. Although in the end only the version in 40 nm CMOS has been processed, it is interesting to compare both implementations in terms of power efficiency, linearity and noise performance based on simulation results. Both implementations have a sampling frequency around 2 MHz and consist of an eight-stage ring oscillator. The control voltages, controlling the delay of each stage, are coming from a differential resistive sensor, biased by a replica of the oscillator stage. The (noise) current through this sensor is therefore also correlated to that in the oscillator stages.

8.5.1 Implementation in 130 nm CMOS

The interface has first been designed in a 130 nm standard CMOS technology. In this technology standard-V_{th} as well as low- and high-V_{th} transistors are available which makes low- or high-voltage design often more easy. The problem is that this design

Table 8.1 The most important design parameters of the PWM-based sensor interface in 130 nm CMOS

MOSFET	W/L
M_1	9.5 µm/1 µm
M_2, $M_2\prime$	8.0 µm/0.2 µm
M_3, $M_3\prime$	1.2 µm/0.13 µm
M_4	2 µm/0.12 µm
Parameter	Value
I_{D,M_1}	8–10 µA
C	2 pF
V_S	300 mV

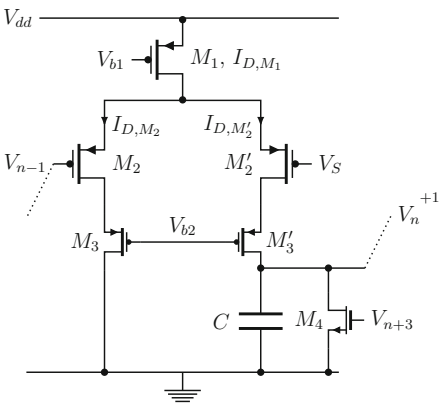

Fig. 8.12 The most important design parameters of the PWM-based sensor interface in 130 nm CMOS

has to work over very different supply voltages: the simulated range is from 0.8 to 1.6 V, which strongly reduces the design possibilities. As shown in Sect. 8.3.2, the control linearity of the delay stages is crucial to maintain the supply independence. Moreover, linearity in this case means that the (extrapolated) linear voltage-delay relation needs to go through zero at every supply voltage and for every temperature. This can be obtained by increasing the output resistance of the differential pair. As can be seen in Table 8.1 and Fig. 8.12, the size of the current source is rather large to decrease the voltage drop V_{ds} over this transistor. This creates the voltage headroom needed to use a cascoded differential pair, resulting in a high output resistance over a wide range of supply voltages. The output resistance of the current source is less important in this case since, when switched completely, the cascoded differential transistors act as 2 cascode transistors.

The sensor DC voltage V_S is around 300 mV, which leaves a headroom of around 200 mV for each transistor. When the voltage over the capacitor increases further, eventually the output impedance drops until the charging stops. An important design constraint is that the switching operation of the next delay stage must be completed before the charging current starts to drop. The output waveform of 4 stages are plotted in Fig. 8.13. The point-symmetry due to the linear charging curve is clearly

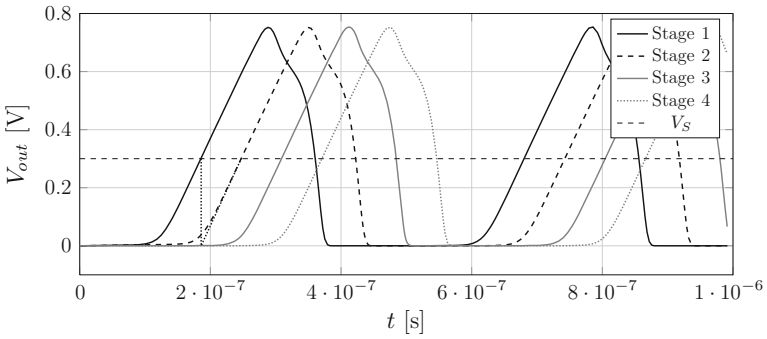

Fig. 8.13 Output waveform of 4 oscillator stages. The linear charging curve as well as the slow switching and the point-symmetry of the switching operation are clearly visible

visible. It is clear that the switching operation is designed to be as large as possible, but is completed at the moment the next stage starts to switch. In this graph, which is a simulation at $V_{dd} = 1\,\text{V}$, it shows that the voltage of the charging curve increases largely above 300 mV, which guarantees a linear curve until the next stage is completely switched. These margins on the switching time as well as the voltage headroom decrease rapidly when the sensor voltage is modulated. On the borders between the fast and the slow stages, the limits are reached soon, which causes a nonlinear behavior for lower supply voltages (as will be seen later).

The 8-stage oscillator has an oscillation frequency around 2.2 MHz which hardly depends on the sensor input value. It does, however, slightly depend on the supply voltage and temperature. As will be shown in the next paragraph, these frequency changes have a low impact on the sensor output value.

8.5.1.1 Simulation Results

To prove the high linearity, the interface has been simulated over a $\pm 15\,\text{k}\Omega$ resistor deviation which corresponds to a $\pm 25\,\%$ change of the sensor output voltage. The resistor is fed by a replica of the oscillator stages which acts as a (cascoded) current source. On Fig. 8.14a and 8.14b the linearity error relative to the output range is shown as a function of the supply voltage and of the temperature respectively. An accuracy of 9 bit can easily be obtained for this wide input range at all temperatures and supply voltages. Figure 8.15a and 8.15b show the relative error compared to the reference supply voltage (1.2 V) and temperature (30 °C). The maximum error is 1.2 % which is extremely low for the applied environmental changes. The presented design therefore proves the extreme robustness of this topology. In specific applications, where smaller temperature and supply changes are expected, the results can even further be improved.

To calculate the Signal to Noise Ratio (SNR) and the Signal to Noise and Distortion Ratio (SNDR), transient circuit simulations have been performed including noise.

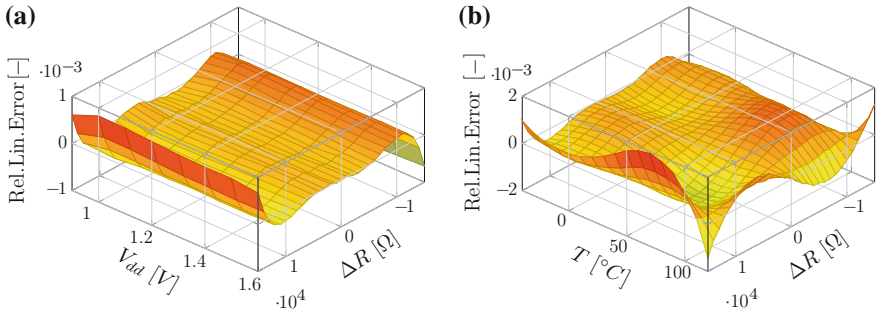

Fig. 8.14 Linearity error of the output duty cycle as a function of the input voltage. In **a** the supply voltage V_{dd} is varied from 0.9 to 1.6 V; in **b** the temperature is varied from −40 to 120 °C

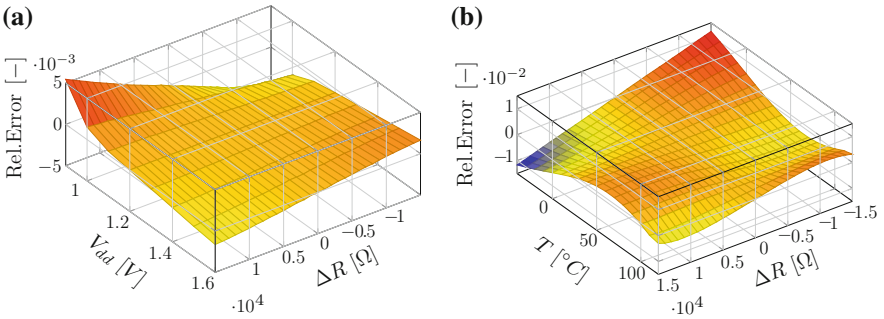

Fig. 8.15 Simulated error on the output duty cycle as a function of the input resistance. In **a** V_{dd} is varied and the error is relative to the output value at 1.2 V. In **b** the temperature is varied (−40 to 120 °C), the error values are relative to the output value at 30 °C. The maximum error appears at low temperatures for high input values and is equal to 1.2 %

A 100 kHz input signal with different amplitudes is applied at the input resistors. The spectrum of the output PWM signal for an input signal with an amplitude of 25 % is shown in Fig. 8.16. The 100 kHz input signal is clearly visible and the noise bandwidth (from which the SNR and SNDR are calculated) is equal to 1 MHz. Due to the symmetrical structure of the interface, the output signal contains only odd harmonics. In Fig. 8.17 the resulting SNR and SNDR are shown for different input amplitudes. From the SNDR also the effective number of bits (ENOB) is calculated. For amplitudes lower than around 15 %, the SNDR is mainly dominated by the noise of the oscillator circuit. At higher amplitudes, the SNDR is determined by the distortion of the output signal. Therefore, the ENOB reaches a maximum of 10.2 bits at an amplitude between 10 and 25 % of the equilibrium sensor resistance (dc input voltage).

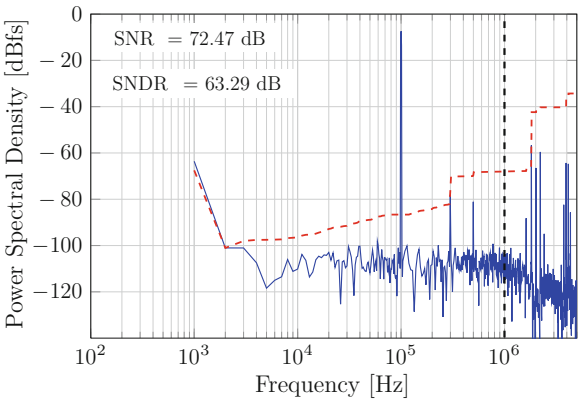

Fig. 8.16 Output spectrum of the sensor interface in 130 nm. The noise bandwidth is equal to 1 MHz, the 100 kHz, 25 % amplitude input signal is clearly visible

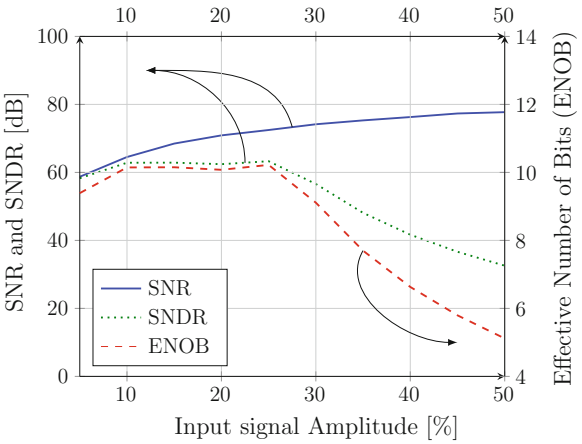

Fig. 8.17 The SNR and SNDR as a function of the input amplitude. From the SNDR also the ENOB can be calculated. A maximum is reached for an input amplitude between 10 % and 25 % of $V_{S,DC}$

8.5.2 Implementation in 40 nm CMOS

The implementation in a 40 nm technology is, as expected, very similar to the 130 nm implementation. The used technology has a nominal supply voltage of 0.9 V, which slightly reduces the headroom compared to the 130 nm technology. According to the design manual, it is, however, possible to use the technology at a nominal supply voltage of 1.2 V without significant transistor aging effects. Another difference with the 130 nm technology is the transistor threshold voltage V_{th}. Instead of an expected reduction of V_{th}, an increase of around 20 % has been observed during the simulations

(from around 350 mV to around 430 mV). Furthermore, the difference between the nominal-V_{th} and the low-V_{th} transistors is small (30 mV), which makes the technology at first sight more difficult for use in low-voltage applications. During the simulations, however, this constraint seemed to be relaxed because the border between the different operation regions is fuzzy. While performing a DC simulation, it is often not clear what the impact is of the operating region. AC simulations show that high frequency operation (3 GHz and higher) in this deep-submicron technology is perfectly possible when the simulator indicates an operating point in the sub-threshold region. This is much higher than expected and is therefore an indication that the meaning of V_{th} and the other parameters in the transistor current equation is not what it used to be. This makes the design less straightforward. Furthermore, contrary to the transistor bandwidth, the linearity of the designed circuits (and the expected quadratic behavior of the differential pair) suffer greatly from the sub-threshold operating point.

As can be seen in Fig. 8.18, the circuit topology is exactly the same as in the previous design case. The transistor sizes and other design parameters, which do differ from the previous case, are shown in Table 8.2. From the previous discussion it appears that, due to the increased high-frequency performance, the technology

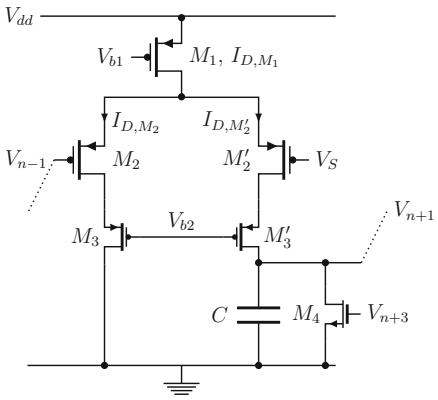

Fig. 8.18 The most important design parameters of the PWM-based sensor interface in 40 nm CMOS

Table 8.2 The most important design parameters of the PWM-based sensor interface in 40 nm CMOS

MOSFET	W/L
M_1	$2 \times 1.09\mu/0.86\mu$
M_2, $M_2\prime$	$3 \times 1.5\mu/0.04\mu$
M_3, $M_3\prime$	$0.73\mu/0.16\mu$
M_4	$4 \times 1\mu/0.30\mu$
Parameter	Value
I_{D,M_1}	$2 - 4\,\mu$A
C	752 fF
V_S	300 mV

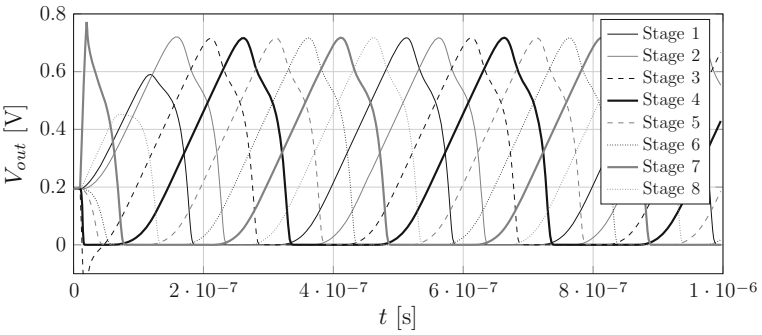

Fig. 8.19 Simulated output waveform of the 40 nm oscillator at a supply voltage of 1.2 V. When the output of stage 7 ($n + 3$) is active, the current of stage 4 (n) can be switched off

allows ultra-low power design for applications in the lower frequency range. As mentioned above, due to the high V_{th} and the fuzzy border between the operation regions, an increased nonlinearity is observed.

8.5.2.1 Current Switching

One of the drawbacks in the coupled sawtooth oscillator is the current dumping. At every moment, only a few stages are active. This means that a lot of current is flowing in the unused stages and a lot of energy is needlessly wasted or 'dumped'. An easy way to solve this is by switching off the current sources of the inactive stages. Similar to the discharge signals (which are coming from the other oscillator stages), the necessary control signals are available within the oscillator itself. In this case, the oscillator counts 8 stages, of which 4 can easily be switched off. Note that this technique is difficult to implement when only a small number of stages is used in the oscillator.

When taking a look at the output waveform of the oscillator (Fig. 8.19), it is observed that the current of stage n can be switched off when the output of stage $n + 3$ is high. This is (as expected) the same signal as was used for the reset of the nth stage. Note also that it is important to *switch off* the current instead of switching it *on* when an output is high. This would lead to an oscillator that would never start. The estimated power reduction in the oscillator stages is almost 50 %. The switching operation can be implemented by a simple digital circuit, shown in Fig. 8.20. The trip point of the inverter is designed to be around 300 mV, to increase the power savings using low-V_{th} transistors. Simulations show no impact on the waveform of the oscillator. It is, however, advisable to connect a decoupling capacitor to V_{b1} to avoid any spikes (noise) due to the on- and off-switching.

As shown in [92], current switching also has a positive effect on the noise in the oscillator [283]. By switching off the current through the current source and the differential pair, the noise sources are also switched off during the time interval in

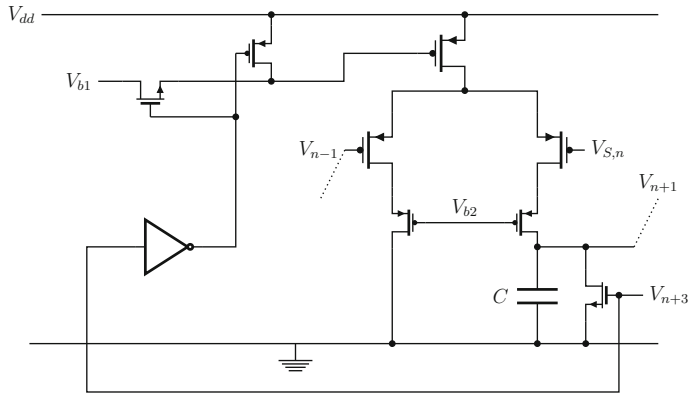

Fig. 8.20 Schematic of the current switch circuit. The current source is switched off when the stage is reset. When the oscillator is not oscillating, all current sources are switched on, which enables the startup of the oscillator

which the capacitor is discharged. This results in a reduction of the $1/f$ noise of the oscillator. The main part of the $1/f$ noise, however, is coming from the mirrored biasing current source and is correlated between the different oscillator stages. The noise reduction therefore only has a limited impact on the output noise of the interface. Hence, the output noise is mainly dominated by the cycle-to-cycle jitter caused by the white noise (see also Sect. 8.4) .

8.5.2.2 Simulation Results

Similar to the simulations in 130 nm, a $\pm 25\,\%$ variation of the sensor voltage is applied. In this case, since the biasing current is lower compared to the 130 nm design, this corresponds to a resistor change of $\pm 37.5\,\mathrm{k\Omega}$. Again, the sensor resistors are fed by a replica of the oscillator stage, acting as a cascoded current source. First, the linearity of the sensor interface is analyzed over different temperatures and supply voltages. Unless mentioned differently, the supply voltage is equal to 1.2 V and the temperature is equal to room temperature. This is shown in Fig. 8.21. Compared to the simulations of the 130 nm implementation, the results are rather noisy. Since the settings of the simulator are equal in both cases, this is probably caused by differences in the device models. The trends, however, are clearly visible.

Next, in Fig. 8.22, the relative error is shown compared to the output at the reference voltage of 1 V and the reference temperature of 70 °C. This reference temperature is chosen in such a way that the maximum deviation is more or less symmetric around the reference value. When compared to the 130 nm implementation, the nonlinearity is increased with a factor of 8–10. This is because of the increased transistor nonlinearity. Furthermore, the current through the sensor resistors is not constant due to the finite output resistance of the current sources. The

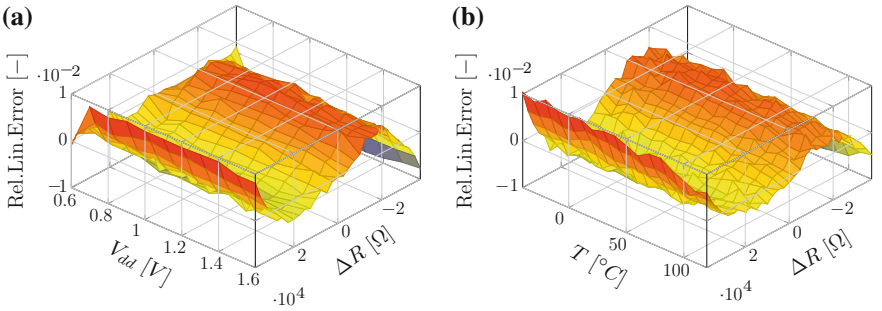

Fig. 8.21 Linearity error of the output duty cycle as a function of the input sensor resistance. In figure **a**, the supply voltage V_{dd} is varied from 0.6 to 1.6 V. In figure **b** the temperature is varied from −40 to 120 °C

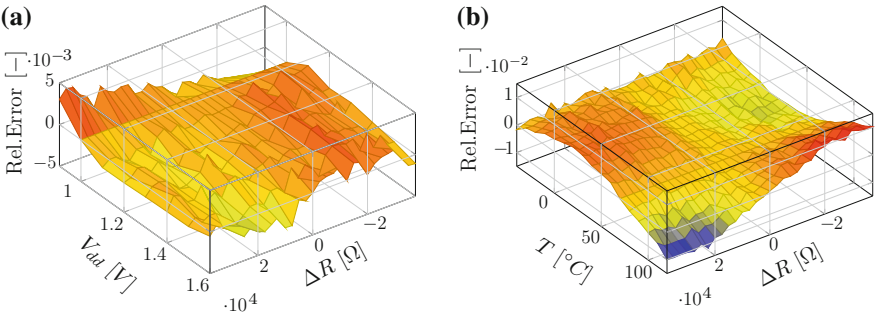

Fig. 8.22 Error of the output duty cycle as a function of the input sensor resistance. In **a** V_{dd} is varied and the error is relative to the output value at 1 V. At all supply voltages (0.9 to 1.6 V) the error stays *below* 0.5 %. In **b** the temperature is varied (−40 to 120 °C), the error values are relative to the output value at 70 °C. The maximum error appears at high temperatures for high input values and is around 1.1 %

error as a function of temperature and/or supply voltage, on the other hand, is very comparable to the 130 nm implementation.

In a next step, instead of modulating the value of a resistor, a voltage is applied to the sensor inputs of the oscillator. Again, a maximum deviation of ±25 % is applied, which in this case corresponds to a differential voltage of ±150 mV (±75 mV variation at each input). When the temperature is varied, the supply voltage is equal to 1.2 V. This results in very similar graphs. Figure 8.23 shows the linearity as a function of the input voltage over different temperatures and supply voltages. The linearity error decreases with a factor of 2 over temperature and supply voltage variations compared to the simulations with a biased sensor resistor at the input.

In Fig. 8.24 the error is shown for the different input values as a function of the supply voltage and the temperature. The error over the different supply voltages stays, similar to the case where the sensor resistance is varied, below 0.5 %.

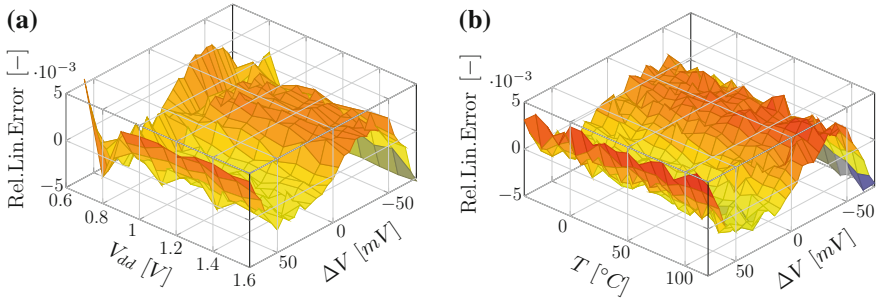

Fig. 8.23 Linearity error of the output duty cycle as a function of the input sensor voltage. In figure **a** the supply voltage V_{dd} is varied from 0.6 to 1.6 V. In **b** the temperature is varied from −40 to 120 °C

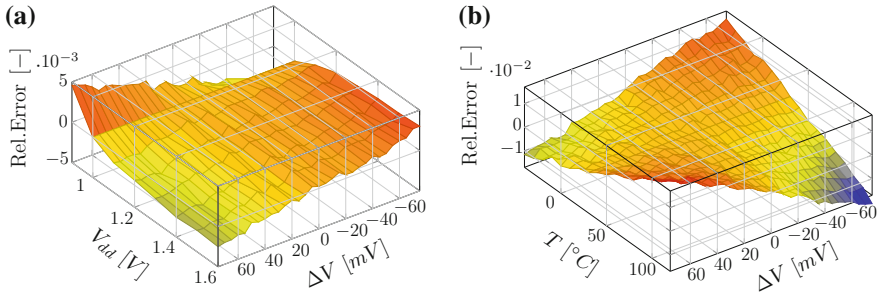

Fig. 8.24 Error on the output duty cycle as a function of the input sensor voltage. In **a** V_{dd} is varied and the error is relative to the output value at 1 V. At all supply voltages (0.9 to 1.6 V) the error stays *below* 0.5 %. In **b** the temperature is varied (−40 to 120 °C) and the error values are relative to the output value at 30 °C. The maximum error appears at high temperatures for high input values and is around 1.5 %

The error over different temperatures slightly increases to 1.5 %. Note, however, that trend of the error over temperature is different from the previous case. In a last step also the dynamic behavior of the sensor interface has been simulated including transient noise. A 100 kHz sine wave with different amplitudes is injected in the sensor interface and the output spectrum is measured. From this, the SNR, SNDR and ENOB can be calculated. In Fig. 8.25 the results are shown as a function of the input amplitude. The optimum is, due to the increased nonlinearity, shifted to the left compared to the 130 nm design case. For a real implementation, the noise is expected to be more dominant, which shifts the optimum somewhat to the right.

A comparison between both sensor interface implementations is shown in Table 8.3. Note that this table only contains simulation results. Although the power consumption of the 40 nm implementation is lower than that of the 130 nm implementation, it is the increased nonlinearity which limits the effective number of bits. However, by increasing the power consumption of the 40 nm implementation, the accuracy can be increased due to the noise reduction for low input swings. The

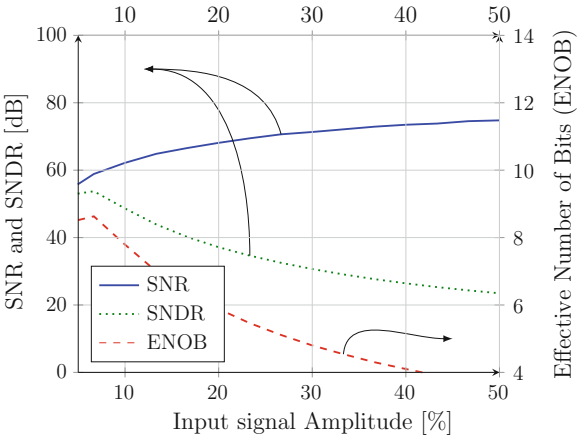

Fig. 8.25 The SNR and SNDR as a function of the input amplitude. From the SNDR also the ENOB can be calculated. The maximum in this case is reached at lower input amplitudes due to the increased nonlinearity

Table 8.3 Comparison of the key simulated properties of the two designs

Technology	130 nm CMOS	40 nm CMOS
Power at 1.2 V (no CS)	96 µW	41 µW
Power at 1.2 V (CS)	(not implemented)	22 µW
Temperature range (error)	−40 to 120 °C (1.2 %)	−40 to 120 °C (1.5 %)
Voltage range (error)	0.8–1.5 V (0.5 %)	0.7–1.5 V (0.5 %)
Speed	>2 MHz	>2 MHz
Nonlinearity (±25 %)	<0.2 %	<0.5 %
Max ENOB	10.2	8.63
Best FoM (V_{dd}) (no CS)	37.1 f J/conv. (1.2 V)	44.0 f J/conv. (1 V)

power efficiency as well as the error as a result of the changing supply voltage and/or temperature are similar in both implementations.

8.5.3 Measurement Results

The interface circuit has been processed in a 40 nm standard CMOS technology. The key measured properties of the circuit are listed in Table 8.4 and a chip photomicrograph is shown in Fig. 8.27. The circuit is laid out in a point-symmetric way in order to reduce the effect of mismatch. The impact of process variations is addressed using replica biasing. The maximum measured offset over 5 samples referred to the input is around 6 mV. This means that an offset calibration is preferable. The nonlinearity has been measured in two ways. First the static nonlinearity, which is shown in Fig. 8.26. The observed behavior closely approaches the simulated behavior in Fig. 8.23.

Table 8.4 Overview of the key properties (5 samples)

Technology	40 nm CMOS
Area (core)	550 µm × 300 µm (95 µm × 95 µm)
Power consumption at 1.0 V	18 µW
Temperature range	−20 to 100 °C
Voltage range	0.8 to 1.5 V
Speed	>2 MHz
Nonlinearity (±180 mV)	<0.7 %
Nonlinearity (±140 mV)	<0.3 %
Max ENOB	7.6

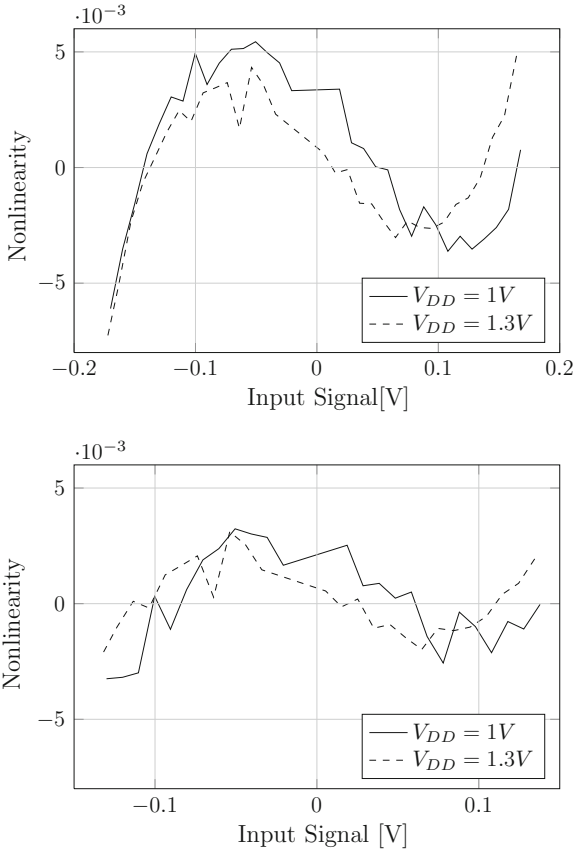

Fig. 8.26 The static nonlinearity of the sensor interface. In the *upper graph*, the nonlinearity is shown for a differential ±180 mV input signal. The *graph below* shows the nonlinearity for a smaller input range of ±140 mV. The nonlinearity slightly decreases when the supply voltage increases

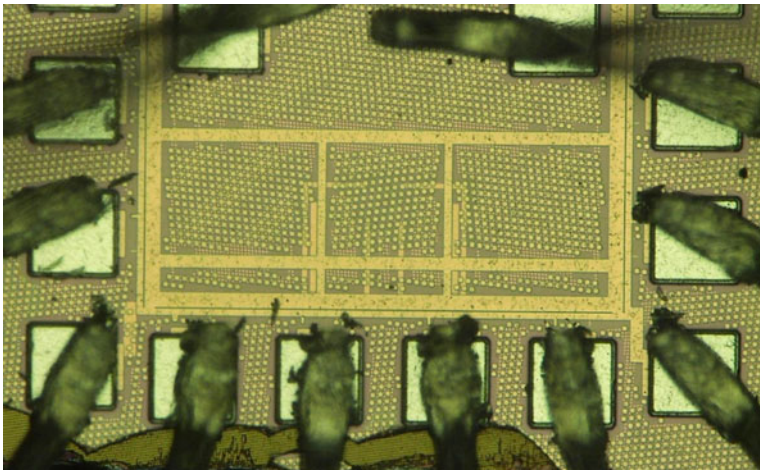

Fig. 8.27 Photomicrograph of the sensor interface in 40 nm CMOS

During the measurements it has been noticed that the linearity improved when the DC component of the input signal was increased by 15–20 % to 360 mV. This is caused by the fact that the switching of the subsequent stages slightly overlaps for higher input amplitudes. This, however, results in a speed decrease when the biasing current is kept constant. The nonlinearity for a ± 190 mV (26 %) differential input signal stays slightly below 0.7 %, while, for a differential input signal of ± 140 mV (20 %), the nonlinearity quickly drops below 0.3 %. This corresponds to an 8-bit accuracy. The dynamic performance of the sensor interface, i.e. the SNR and the SNDR, are measured by measuring the output spectrum when applying a 100 kHz input signal. This spectrum is shown in Fig. 8.28 for a 100 mV input amplitude. As can be seen, although the circuit is differential, a strong second-order component is present in the output signal. This is caused by the mismatch or frequency offset between the 2 oscillator halves. For a 100 mV-amplitude differential input signal, this results in 7.6 effective bits at a 1 V supply voltage. The maximum FoM in this configuration is reached for a bandwidth of 700 kHz. The slight decrease of the effective bits can be explained as a result of the increased nonlinearity due to mismatch.

Apart from this, also some temperature and supply voltage measurements have been performed. The maximum temperature error is 79 ppm/°C over a -20 to 100 °C temperature sweep. The slight increase of the temperature performance is likely caused by the increased DC input (linearity). The output deviation over a 0.8–1.5 V supply voltage span is below 1.42 %/V. For both parameters, the error profile is similar to the previously simulated behavior. In Table 8.5 the circuit is compared to other state of the art sensor interfaces. Although the original focus of the design was to withstand temperature and supply voltage variations, the linearity of the circuit results in a FoM in the same order of magnitude as the other state of the art interfaces. Because the PWM signal still needs to be sampled before transmission, in Sect. 8.3.3 a rough estimation is made to obtain the FoM for a 50 MHz sampled output

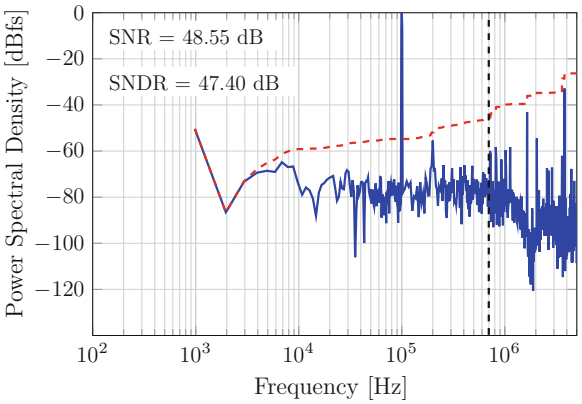

Fig. 8.28 Measured output spectrum of the sensor interface for a 1 V supply voltage and a 100 mV differential signal. The SNDR determines the effective number of bits since it takes the noise as well as the distortion into account. The maximum FoM is reached for a 700 kHz bandwidth

signal. This is shown in the lower half of the table. The circuit in [319] has a unique temperature independence and an ultra-high resolution. This, however, comes at the cost of a higher FoM, which cannot be accepted in this low-power application. The other circuits, such as [99], have a comparable FoM to our design, but have a higher power consumption or did not optimize for temperature and voltage independence, which makes them less suitable for use in wireless sensor networks. The proposed topology makes a unique trade-off between power efficiency, accuracy and stability over supply voltage and temperature changes.

Table 8.5 Comparison to the state of the art in sensor interfaces

Ref.	Tech. (µm)	Power (µW)	Speed (MHz)	ENOB	T sens. (ppm/°C)	V sens. (%/V)	V-range (V)	FoM[a] (J/b-conv.)
This work	0.04	18	2.1 (1.4)	7.6	79	1.42	0.8–1.5	66.2 f
[58], ES '12	0.13	96	2.2	10.2	86	0.71	0.9–1.6	37.1 f
[44], ES '11	0.13	2.3 m	42	10	–	–	–	55.2 f
This work, sampled[b]	0.04	28	0.021	7.6	79	1.42	0.8–1.5	6.6 p
[263], ASSCC '12	0.13	124.5	0.01	8.9	–	3.3	0.85–1.15	13.03 p
[45], ESSCIRC '11	0.13	270 n	1 k	6.1	–	–	0.3	2.1 p
[247], ASSCC '07	0.18	504	262 k	6.8	–	–	1.0–1.8	17.3 p
[19], TCAS I '07	0.5	7	10 Hz	8	–	–	2.7–3.3	1.37 n
[319], JSSC '12	0.7	1.35 m	5.88 Hz	20	0.7	–	5	219 p
[99], CICC '12	0.13	11.3	1 k	11.2	–	–	0.5	4.8 p

[a] $FoM = Power/(Speed \cdot 2^{ENOB})$,
[b] Estimate

8.6 Conclusion

In this chapter the design of an ultra-low-power sensor interface has been discussed. The proposed topology, which is a differentially modulated ring oscillator, is very robust against supply voltage and temperature variations. Furthermore, also the effects of scaling towards a deep-submicron technology have been investigated. Although there is a slight increase in nonlinearity, a significant power reduction is obtained in an advanced technology. As a result, the FoM stays in the same order of magnitude. The 40 nm implementation has been fabricated and measured. The main problem seems to be the mismatch between the oscillator stages. The design, however, has resulted in a FoM comparable to other state of the art implementations.

Part III
Wireless Sensor Nodes

The last part of this Ph.D. work describes the development of a wireless integrated RFID tag. It will be seen in Chap. 9 that the main building blocks of this tag have previously been developed in Part II. While discussing the architecture of the RFID tag, it will be shown that the architecture of the building blocks results in a greatly increased flexibility of the tag.

Finally, in the last chapter, Chap. 10, an elaborate comparison will be made between all oscillator implementations discussed in this Ph.D. work and the state of the art. Furthermore, the drawbacks of the different architectures will be compared, which finally results in suggestions for possible future work.

Chapter 9
Design of a Low-Power Wireless RFID Tag

9.1 Introduction

The first chapter of this thesis has depicted the different challenges of building a wireless sensor network. This has resulted in a wish list of specifications for the circuitry on a wireless tag. One of the main problems is the powering of the tag. Here, it is assumed that RF scavenging is used as energy source. An elaborate discussion on this is found in [51]. Due to the extremely low power output of such RF scavengers and the lack of sustainable energy reservoirs, an unstable supply voltage is unavoidable. Moreover, the available power budget is extremely limited. Therefore, the most important specifications of the tag circuitry are the supply-voltage and the temperature (PVT) independence. As shown in Chap. 4, this poses a huge challenge for the timing circuitry. Nevertheless, when using relative timing accuracy instead of absolute accuracy, the use of a time value has proven to be useful to obtain a PVT-independent sensor interface, as demonstrated in Chap. 8.

When talking about the network layer of a wireless sensor network, other challenges arise. In an environment with hundreds of tags, network coordination is necessary to avoid data loss due to collisions [156]. Furthermore, unnecessary transmission of data bursts results in a waste of energy at the transmitter side.

The tag to be presented in this chapter makes use of the building blocks described in part II of this work. This results in a highly-flexible RFID tag with an on-board coordination receiver and sensor interface. As a result of the technology change compared to the work in [51] (130 to 40 nm CMOS), no RF energy scavenger has been implemented on the tag. Therefore an external energy source must be attached (for instance a scavenger or a small battery).

This chapter is organized as follows. In the next section the tag architecture will be discussed. Afterwards, the different building blocks will briefly be discussed, referring to the corresponding chapters. In Sect. 9.2.4 the focus will be on the digital logic. Next, in Sect. 9.3, the measurement results will be discussed and compared to the results of the standalone building blocks. Finally, in Sect. 9.4, conclusions will be drawn.

V. De Smedt et al., *Temperature- and Supply Voltage-Independent Time References for Wireless Sensor Networks*, Analog Circuits and Signal Processing 128,
DOI 10.1007/978-3-319-09003-0_9

9.2 Architecture of the Wireless Tag

A system overview and block diagram of the proposed tag architecture is shown in Fig. 9.1. The wireless tag contains both an Ultra-Wideband (UWB) transmitter and a 2.4 GHz small-band receiver to receive network commands (see Chap. 7). Apart from this, also a digital controller block and a sensor interface (see Chap. 8) are incorporated. A downlink is implemented using an ultra-low-power pulsed-UWB transmitter. The digital logic is switched on by the receiver logic when the correct 8-bit RFID address of the tag is received. Afterwards, the digital logic controls the power supply of the transmitter and the sensor interface.

The digital logic (see Fig. 9.2) consists of a Finite State Machine (FSM) and different counters to control the length of the preamble, the device data and the sensor data in the transmitted burst. All transmitted data are scrambled with the output of a 6-bit LFSR, which allows code lengths up to 63 chips. The output signal is sent to the UWB transmitter. The tag address, the scrambling polynomial and initial data of the LFSR and the data and packet length are programmed through a 55-bit shift register. This allows to adapt the content, actions and energy consumption of the tag during one burst depending on the application.

Another important improvement compared to the state of the art is the ability of all circuitry to work over a wide and varying supply voltage range, from 0.8 to1.5 V. The

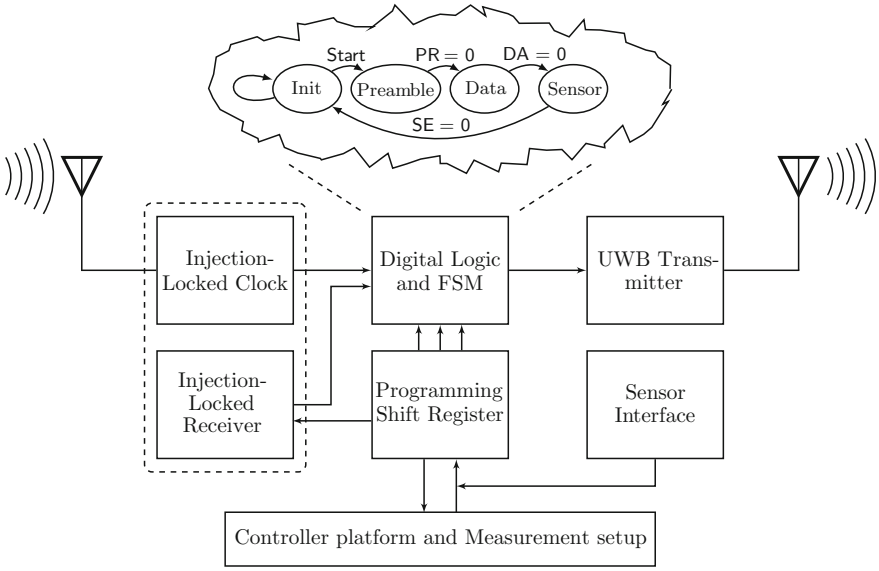

Fig. 9.1 Block diagram of the wireless RFID tag. The power supply and clock input of different building blocks are controlled by the digital control logic. The state diagram of the finite state machine (*FSM*) is shown *at the top*. The length and content of the different states can be programmed by means of the shift register

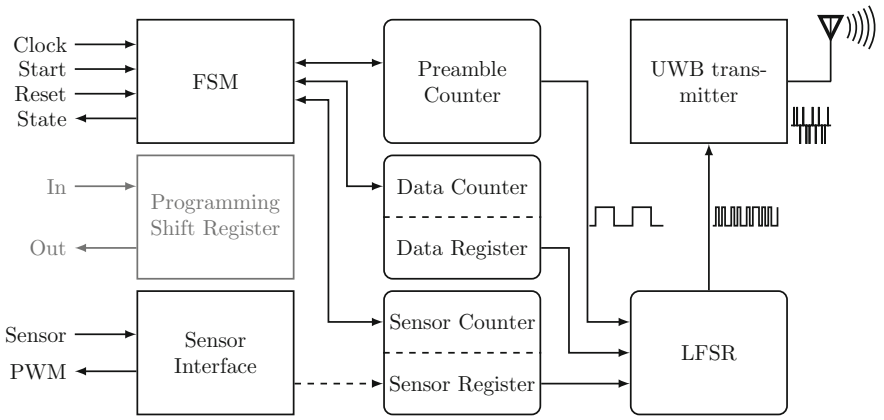

Fig. 9.2 Overview of the digital logic on the WSN tag. The FSM relies on different counters to make the right state transitions. The transmitted data, including the preamble, are scrambled using an LFSR before they are sent to the UWB transmitter. The shift register is used to control the length of the different states, the data and the LFSR scrambling code

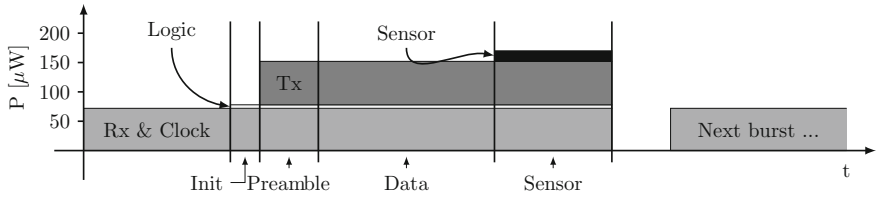

Fig. 9.3 Profile of the energy consumption during one burst. In the initial phase, only the clock circuit and the receiver are switched on. When a correct tag-ID is received, the digital logic and the transmitter are switched on. Next, the preamble, data and finally also the sensor data are subsequently transmitted. Afterwards, the tag is switched off

RFID tag can therefore be used in almost any application where energy scavenging is used, going from RF scavenging to a solar cell, or even be used with a small battery.

A profile of the power consumption during one data burst is shown in Fig. 9.3. At the beginning, only the oscillator is activated, consuming 72 μW. When the correct address is received, the digital logic (4 μW) and the ultra-wideband transmitter (75 μW) are switched on. Finally, in the sensor state, also the sensor interface is activated (18 μW). The complete RFID consumes only 169 μW.

9.2.1 The Clock and Receiver Circuit

The clock and receiver circuit has already elaborately been discussed in Chap. 7. The use of the presented topology, shown in Figs. 7.23 and 7.34, results in different power savings. By using the AM-modulated RF signal, the local oscillator can be injection-

locked to a central clock to overcome the influence of supply voltage and temperature variations on the accuracy of the local timing circuits. As a result, the length of the preamble can drastically be shrunk, which results in a major power reduction at both the transmitter and the receiver side of the UWB downlink. The injection-locked receiver is part of the oscillator circuit. By modulating the time between subsequent phase shifts applied to the injected AM signal, data are transferred. As explained, the applied phase shifts can be detected by a simple D-flipflop since the phase difference between the injected signal and the injection-locked oscillator always lies within a $\pm 90°$ interval. For a 30 MHz injected clock frequency, using a 4-bit counter, this results in an ultra-low-power 1.8 Mbit/s receiver. Compared to a simple oscillator, the receiver circuit overhead is extremely limited.

The most important power savings of the injection-locked clock and PSK uplink, are in the network aspect. First of all, since all clocks are perfectly synchronized, the preamble can be shortened drastically. When the first pulse is received, the moment the next pulses will arrive is exactly known. A second benefit is the reduction of data collisions, which on its turn reduces the unnecessary power consumption of the transmitter as well as the receiver. Also, the number of transmitted data bursts which are not received, can be reduced drastically.

9.2.2 The UWB Transmitter

The pulsed Ultra-Wideband (UWB) transmitter consists of a pulse generator and a differential H-bridge to transfer the pulse to the antenna, see Fig. 9.4. As can be seen, the pulse width is a function of the supply voltage: the higher the supply voltage, the higher the transmitted power. This can easily be solved using a voltage regulator. Obviously, the pulse width has an impact on the frequency spectrum. Therefore, in

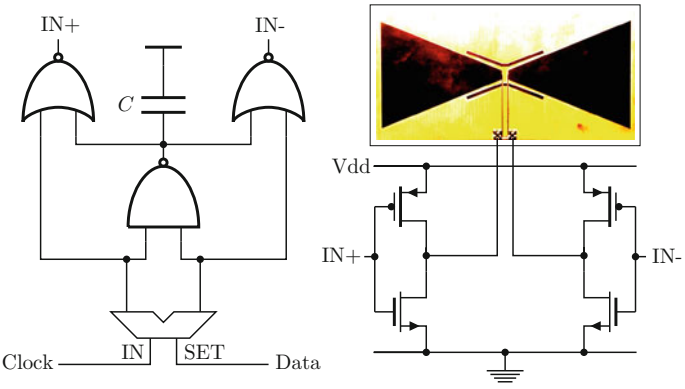

Fig. 9.4 Block diagram of the pulse generator and output stage with antenna. The capacitor C is used to set the correct pulse width

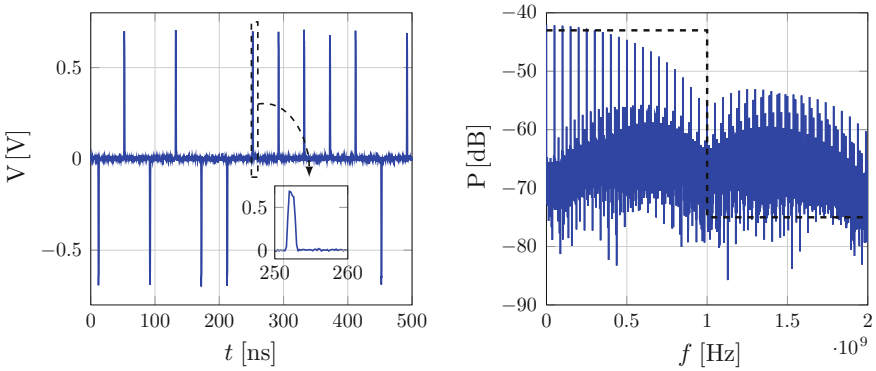

Fig. 9.5 Output waveform (*left*) and spectrum (*right*) of the UWB transmitter with a 250 Ω load resistor. When using an appropriate antenna, the output spectrum is filtered and fits nicely within the FCC mask (*dashed line*). The design of the antenna is discussed in [209]

literature, numerous other techniques exist to control the exact pulse shape [105, 182, 286].

The pulse generator on the presented wireless tag generates pulses in the lower UWB frequency band (0–1 GHz). As can be seen in Fig. 9.5, the generated pulses have a spectrum quite close to the FCC mask regulation [79, 228]. When using an appropriate antenna, the pulses are filtered and the FCC mask is met. The design of such an antenna is discussed in [209].

The main benefit of the lower-band UWB transmitter is the very simple topology, which results in a low power consumption. Another important benefit is the possibility to do accurate localization using the short pulses in the time domain [272, 321]. In [272] it is shown that a windowed sine wave can be used as a pulse template to correlate the received pulses. This correlation is needed to recover the pulses from underneath the noise floor. To do so, however, the pulse frequency needs to be extremely accurate, i.e. in the order of 100 ppm of a complete data burst. A (slow) pulse train (using two identical butterfly antennas as shown in Fig. 9.4) received over a 50 cm link is shown in Fig. 9.6. At higher distances the received pulses will disappear under the noise floor. It is clear that, apart from the timing issues, the complexity of a pulsed-UWB link indeed shifts from the transmitter to the receiver side. The feasibility of such an ultra-low-power UWB receiver has been shown in [271].

9.2.3 The Sensor Interface

As explained in Chap. 8, the sensor interface generates a PWM signal of which the duty cycle is a measure for the sensor signal value at the input. Instead of using an absolute time value, the duty cycle depends on the *ratio* of the modulated stage

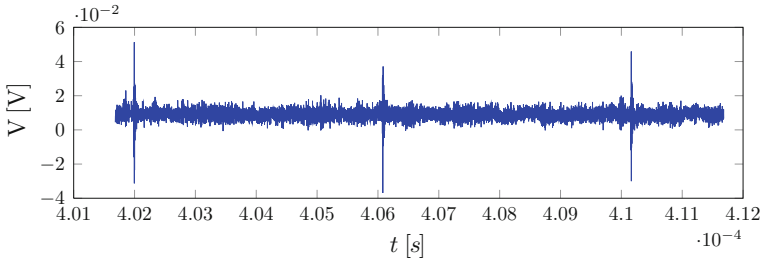

Fig. 9.6 Received slow pulse train over a 50 cm wireless link. At higher distances, the received pulses disappear under the noise floor

delays of a ring oscillator. As previously shown, this leads to a highly-accurate and temperature- and supply voltage-independent sensor readout. To minimize the power consumption of the circuit, the network shown in Fig. 8.20 automatically switches off the current sources of the stages in reset, which results in a 40 % power reduction. As explained in Sect. 8.3.3, the output signal can be sampled at an arbitrary clock rate. Therefore, depending on the application and the required sensor resolution, the sampling speed as well as the number of transmitted samples of the interface output signal can be adapted. Here, a differential input voltage is used. Note that, when using for instance a resistive divider as a sensor, the sensor also needs to be switched off during the sleep period (to implement this externally, the state bits of the FSM are available at the output).

9.2.4 The Digital Logic

The digital controller logic is the only part of the tag which has not been discussed in the previous chapters. Although this building block has a negligible power consumption compared to the analog circuitry, also here different measures have been taken to reduce the power consumption. Static logic is used to limit the static power consumption. Simulations show that, even for frequencies below 1 MHz, minimum sized logic has the lowest power consumption. Furthermore, it is the digital logic which also controls the power consumption of the other circuitry.

The digital logic mainly consists of programmable ripple counters. All these counters are built using the same static flipflop, shown in Fig. 9.7. To avoid high currents during a data change, the feedback loops are cut by the clock signal. Ripple-through of data is avoided by buffering the clock in every flipflop and by propagating the clock signal in the opposite direction as the data signal. These flipflops are used to implement different building blocks, going from ripple counters to an LFSR. To demonstrate the programming hardware of these devices, a block diagram of the counter is shown in Fig. 9.8. The programming logic is implemented using a demultiplexer of which the outputs are connected to the SET and RESET input of the flipflops. In Fig. 9.9 the LFSR circuit is shown. The initial values as well as the used polynomial can be programmed through the shift register. Code lengths from 1

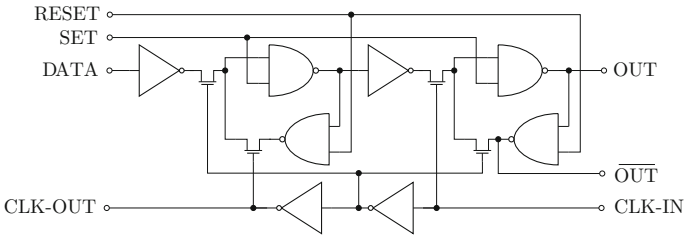

Fig. 9.7 The digital logic mainly consists of counters and shift registers. All of them are built using this basic flipflop

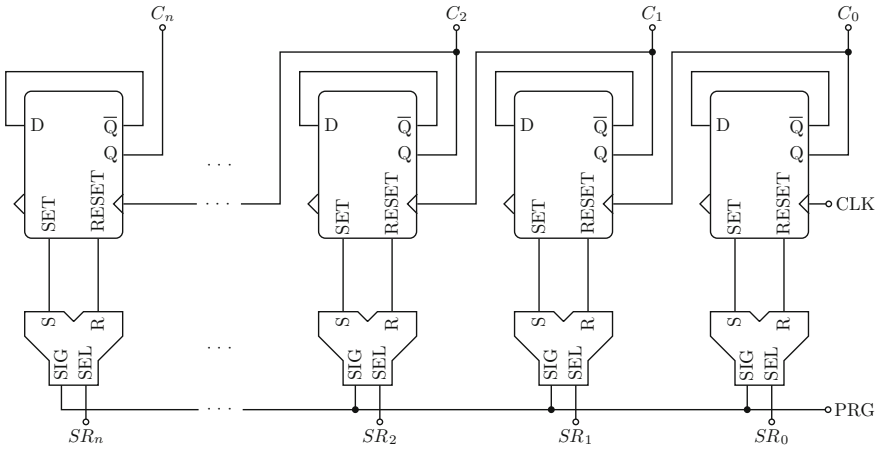

Fig. 9.8 Block diagram of an n-bit programmable counter. The counter is set to the values in the shift register at the moment when PRG is set

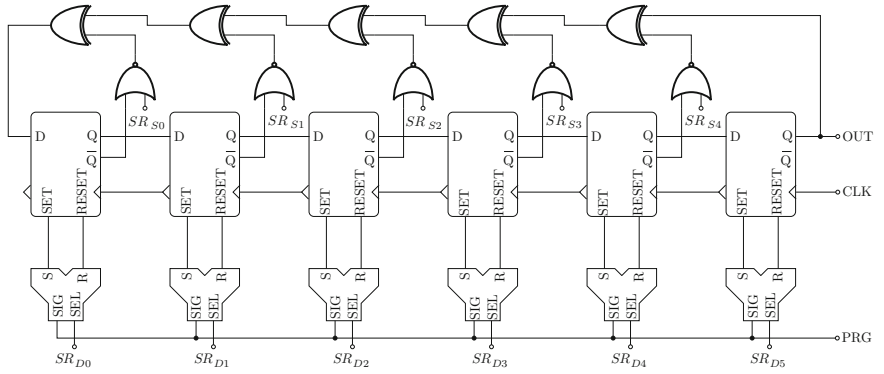

Fig. 9.9 Block diagram of 6-bit LFSR. The initial values as well as the used polynomial can be programmed through the shift register. Code lengths ranging from 1 to 63 bits can be generated using this hardware

to 63 bits can be generated with this hardware. One of the counters is also used as a programmable clock divider. This slow clock signal is used as a data clock: one period exactly corresponds to the length of the LFSR scrambling code. The length of the required period is programmed, and the clock is automatically reset at the rising edge of the MSB in the (down-counting) clock counter.

The Finite State Machine (FSM) consists of a 2-bit state counter, which is automatically reset to the initial state when the power is switched on. During the initial state, all counters and the LFSR are programmed. Afterwards, during the other states, the output logic of the FSM gates the clock signals of the different counters. To save energy, the transmitter and the sensor interface are only switched on during the corresponding states. After the last state, the complete tag is automatically switched off. Depending on the available energy and the source of energy scavenging, it can take several minutes before the oscillator is switched on again, awaiting the reception of a next valid tag-ID.

9.3 Measurement Results

The wireless RFID tag has been implemented in a 40 nm general purpose standard CMOS technology. It has been measured using a PIC-controller platform to automatically program the desired settings in the shift register and control all biasing settings digitally. A photograph of this setup is shown in Fig. 9.10.[1] A chip photograph and a bonded sample are shown in Fig. 9.11. Although all building blocks on the tag are functional, supply coupling from the transmitter to the AM-demodulators affects the

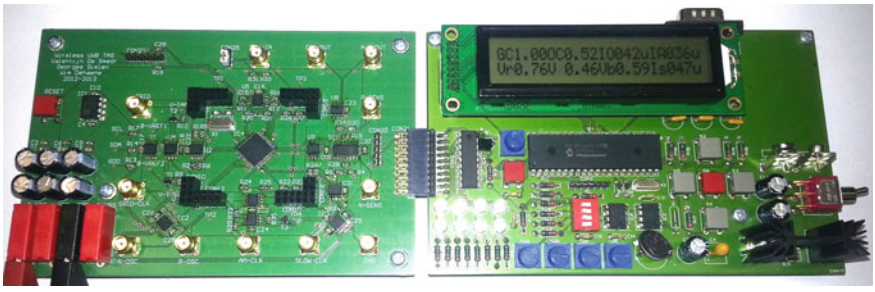

Fig. 9.10 Photograph of the automated multi-purpose measurement setup. The pcb *on the right* is a general-purpose PIC-controller platform with several human interface devices and a serial link to a PC or other measuring hardware. The board *on the left* contains all chip-specific hardware, going from DACs, to analog and digital buffers and digital potentiometers to steer the sensor interface. Both boards contain a controller, connected through an I^2C link. The data shown on the display is steered by the *left controller board* to easily detect any communication errors between both controllers

[1] A similar measurement setup has been used for the previous designs in an attempt to be able to easily reproduce any measurement data.

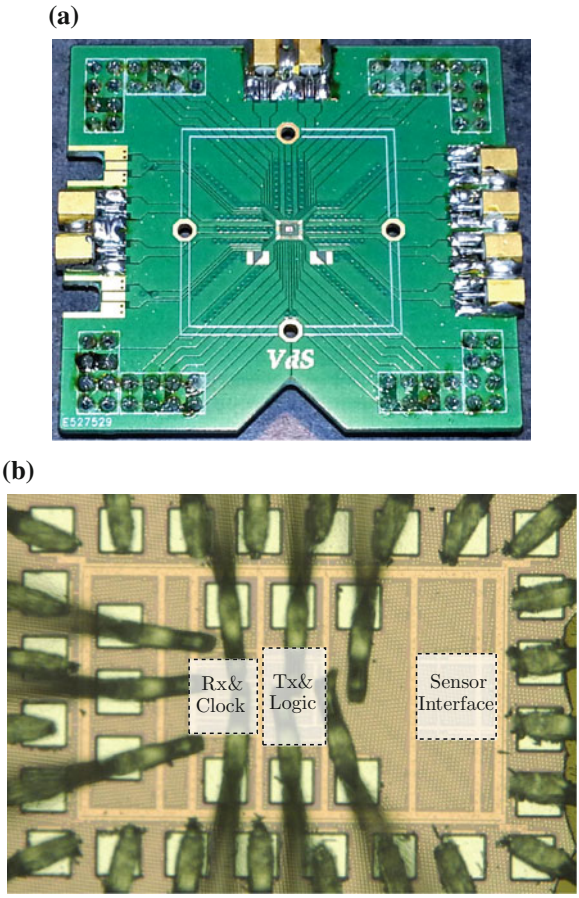

Fig. 9.11 Photograph of a bonded sample. **a** For the high-frequency signals mmcx connectors are used. **b** Photomicrograph of the wireless RFID tag

sensitivity of the injection-locked receiver. This can result in carrier loss during the data burst in the case of a weak RF signal. To prove that this artifact can be solved using a better supply decoupling, extra measurements have been performed using 2 interconnected dies: one die where the clock and receiver circuitry is used, a second die where all other tag circuitry is used. This is shown in Fig. 9.12.

During the measurements of the interconnected dies, the programmed RFID was synchronized, addressed and activated. The output signal of this first die activates the circuitry on the second die. Next, a burst of data was transmitted and the sampled sensor interface output data were clocked in the shift register for broadcasting during the subsequent data burst. The maximum length of the preamble, the (programmable) device data and the sensor data is 128 bit each, which results in a 384-bit packet length, or a burst of 384–24,192 pulses, depending on the LFSR scrambling code

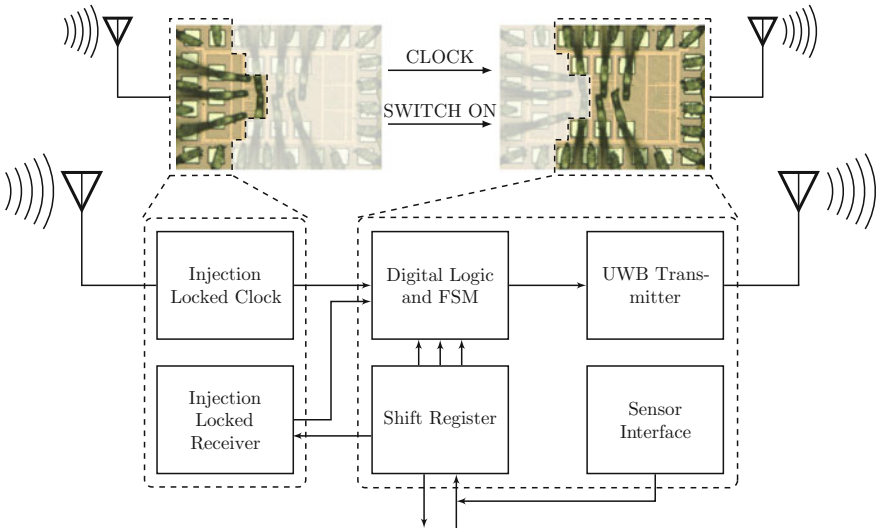

Fig. 9.12 The single-ended structure of the AM-detectors results in a high sensitivity to supply noise. Therefore, to improve the input sensitivity of the resulting tags, two connected dies have been used at measurement time. The supply coupling and sensitivity problem can be reduced by an improved detector topology, increased supply decoupling or the use of guard rings around the different blocks

used. During the main part of the measurements, a mains-powered power supply has been used. Measurements using a precharged capacitor as a small energy reservoir, return similar results (in the 2-die measurement setup, 2 separate capacitors have been used). For the wireless activation of the tag, a two small copper wire dipole antennas were used.

Since integrating a 2.4 GHz antenna is difficult as a result of the wavelength, in a fixed setup the antennas can also be etched on a printed circuit board (pcb).

Table 9.1 contains a comparison of the tag measurement results to other state of the art WSN implementations. The key improvements of this design are the versatility and programmability towards almost any sensor application and the ability to withstand voltage (0.8–1.5 V) and temperature (−20 to 100 °C) variations. The presented tag is a unique combination of flexible high-performance building blocks. The coordination receiver has a high bandwidth and a low power consumption. This goes at the cost of a drastically decreased input sensitivity. Despite the slightly increased leaking current in the digital blocks, the use of deep-submicron technologies result in a power benefit mainly because of the power reduction (and increased gain-bandwidth and sensitivity) in the input amplifier and other RF building blocks.

The accuracy of the sensor interface can easily be modified by adapting the sampling speed of the output signal depending on the application. Its linearity, voltage and temperature independence surpass the state of the art. Due to the programmability of the tag, the length of the different slots in the data burst can be modified.

Table 9.1 Comparison of the developed tag to the state of the art

	This work	[28]	[200]	[10]
Technology (nm)	40	130	90	180
Rx topology	Inj.-locked, AM-PSK	Inj.-locked, FSK	Uncertain-IF, OOK	–
Rx band	2.4 GHz ISM	45 MHz	2 GHz	900 MHz
Rx power (μW)	72	37.5	52	14.1
Rx sensitivity	−43 dBm	−62.7 dBm	−72 dBm	−18.5 dBm (scav.)
Rx speed	1.8 Mbit/s	200 kbit/s	100 kbit/s	160 kbit/s
Tx modulation	Pulsed UWB	–	–	–
Tx power	75 μW (25 Mp/s, 1 V)	–	–	3–10 GHz UWB
Tx speed	0.47–30 Mbit/s	–	–	10 Mbit/s
Sensor (power)	Resistive (18 μW)	–	–	–
Voltage range (V)	0.8–1.5	0.7	0.5	1.8
RFID power (1 V)	169 μW	–	–	–

This makes the tag a robust solution in all low-energy applications where energy scavenging is used.

9.4 Conclusion

In this chapter, the previously designed building blocks have been combined to a complete wireless tag. The tag is implemented with a programmable shift register which allows to control the content as well as the length of the transmitted data burst. Also the accuracy of the measured data can be controlled in this way. The tag is able to work over a 0.8–1.5 V supply voltage span and a −20 to 100 °C temperature span. This, in combination with the high flexibility, allows to use the tag in very different low-power WSN applications and environments, depending on the available energy and the required accuracy. It was demonstrated that the careful design of the different building blocks results in a highly-flexible yet efficient wireless tag.

Chapter 10
Conclusion

Reasoning draws a conclusion,
but does not make the conclusion certain,
unless the mind discovers it by the path of experience.
Richard Bacon

This work has focused on time-based building blocks for wireless sensor networks. As has been depicted in Chap. 1, the main problems in a WSN are the extremely limited power availability and the changing external parameters such as the temperature and the supply voltage. This results in an important synchronization challenge between the different sensor nodes. Here, a difference can be made between the synchronization within one data transmission burst, which requires an accurate non-drifting oscillator, and the synchronization of the bursts itself, which requires a form of network coordination. A third challenge is the read-out of a sensor value, which also suffers from external variations.

In the first part of this work, the theoretical background has elaborately been discussed. Chapter 2 has focused on the properties of oscillators in general. The different representations of an oscillator signal have been introduced and the main properties of an oscillator circuit have been identified. This allowed to make a difference between the short-term and long-term stability of an oscillator signal, discussed in Chaps. 3 and 4 respectively. Since, in many applications, oscillator phase noise is an important specification, the noise generation mechanisms in an oscillator have been discussed elaborately in Chap. 3. This theory has later been applied to understand the noise generation in the oscillator implementations. Chapter 4 has focused on the long-term oscillator stability, mainly affected by temperature and supply voltage variations. The different sources of frequency instability have been identified and investigated. Afterwards, the state of the art found in literature has been discussed to get a better insight in the design and implementation trade-offs. In the second part, different design cases for temperature and supply voltage stability have been introduced and investigated. This has finally resulted in the implementation of a complete wireless tag, discussed in Chap. 9.

This conclusive chapter is organized as follows: in the first section, the results of the designed oscillator chips will be compared to each other and to the state of the

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art. While doing so, the strengths and drawbacks of each circuit will be identified. Afterwards, in Sect. 10.2, the main contributions of this PhD will be depicted. Finally, in Sect. 10.3, suggestions for future work will be discussed.

10.1 Comparison to the State of the Art

The measurement results of the time references presented in this work are summarized in Table 10.1. They are, from left to right, ordered in the chronological order they were designed. All circuits were designed to obtain an accurate time reference with a variation of the output frequency below ±25–100 ppm during one burst and a variation of maximum ±1 % (10,000 ppm) between two bursts. These target specifications were previously summarized in Table 1.1.

Using different plots, the output specifications are also compared to the state of the art. In Fig. 10.1, the different specifications are shown in a 2-D plot to obtain a better overview. In Appendix D a complete overview of all implementations is found.

10.1.1 The Wien Bridge Implementations

In Chap. 5, two Wien bridge implementations have been developed. The first oscillator was optimized for temperature independence. This can clearly be seen in the second graph, Fig. 10.1b. The power consumption of this implementation is around 66 μW, but it has a small supply voltage range and high voltage dependency (see Fig. 10.1a). This design case, however, proves the fact that on-chip passives can be used to obtain a highly-accurate timing reference. Furthermore, it was shown that, despite the extra circuitry needed to obtain a stable oscillation frequency, the resulting output noise can be in the same order of magnitude as other RC implementations (see Fig. 10.1c).

The second design case has been focusing on voltage independence and a high supply range. This is clearly visible in Fig. 10.1a. Although the temperature can assumed to be constant during one burst, the temperature sensitivity of the voltage-independent oscillator is too high to be practically usable on a wireless sensor node. Temperature fluctuations below 1 °C cannot be guaranteed between two data bursts, which makes a stable communication link impossible. Note, however, that this implementation surpasses the state of the art in terms of power consumption, supply voltage range and supply voltage dependency.

Table 10.1 Comparison of the presented time references

	Chapter 1	Chapter 5		Chapter 6	Chapter 7	
	Target	T-Wien bridge	V-Wien bridge	Pulsed LC	Inj.-lock. 1	Inj.-lock. 2
Topology	–	RC harm.	RC harm.	Pulsed LC	RC harm.	RC harm.
Technology (nm)	–	65	130	130	130	40
Frequency (MHz)	20–50	6	24	48–1,540	950–1,150	23–36
Supply voltage (V)	–	1.2	0.9	1.1	1.0	1.0
Power consumption (μW)	<100	66	33	46	127	72
FoM_{PN} (dB)	–	142.0	–	142.7	–	–
Jitter (ps)	<25	127	–	49.6	–	–
Voltage range (V)	>1	1.08–1.32	0.4–1.4	0.6–1.6	0.7–1.6	0.7–1.5
Rel. volt. range[a] (%)	–	20	111	91	78	73
Voltage sens. (ppm/%)	–	*300*	0.94	0.81	0	0
Temp. range (°C)	−20–100	0–120	–	−40–100	−20–100	−20–100
Temp. coeff. (ppm/°C)	–	86.1 (*33*)	1*e*4	92	0	0
Absolute accuracy (ppm)	±1 %	±8,800	±4,600	±7,600	–	–
Core area (mm^2)	–	0.03	0.03	2.63	0.0022	0.0017
Trimming	No	No	No	No	No	No

[a] $\Delta V_{rel} = 2 \cdot (V_{\max} - V_{\min})/(V_{\max} + V_{\min}) \cdot 100\ \%$

10.1.2 The Pulsed-Harmonic Oscillator

The pulsed harmonic oscillator topology demonstrated in Chap. 6 , delivers a unique combination between low-power design and long-term frequency stability. This is clearly visible in Fig. 10.1a, b. Furthermore, as a result of the large supply voltage range it is suitable for use in a wireless tag. The oscillator relies on a high-Q LC tank which diminishes the losses drastically and contributes, together with the pulsed driving technique, to a decreased impact of the oscillator circuitry. As depicted in

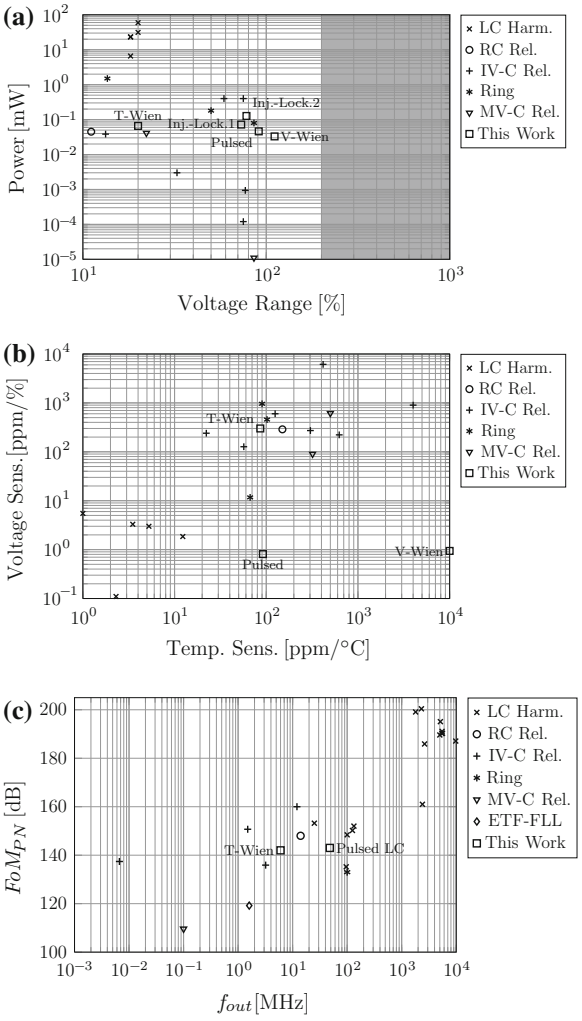

Fig. 10.1 Graphical comparison between the proposed oscillator designs and the state of the art. **a** Shows the power consumption as a function of the available voltage range. Both parameters contribute to the possible burst length. **b** Shows the temperature sensitivity in combination with the supply voltage sensitivity. Important to note are the highly-accurate LC oscillators in the south-west corner, which have a high power consumption and need to be trimmed (the markers correspond to [3, 175, 177, 178, 234]). **c** Shows the noise as a function of the oscillator output frequency. It is clear that all implementations fall within the range of RC (IV-C) implementations

Chap. 6 , although the phase noise benefits from the tank, the noise is dominated by the injected noise during the applied pulsed. Unfortunately, in the current implementation also a large portion of deterministic noise is injected through the supply rails, which makes the 143 dB phase noise FoM an underestimation (see also Sect. 6.7).

10.1.3 The Injection-Locked Oscillators

Since the delivered accuracy of the free-running implementations in terms of long-term frequency stability and absolute accuracy is often not sufficient, also two injection-locked implementations have been designed (see Chap. 7). Both implementations make use of a low-Q RC oscillator, to obtain a large lock range. By locking the oscillator signal to the wirelessly injected power carrier, also the problem of absolute accuracy (which cannot be guaranteed in fully-integrated oscillators) can be solved.

The first implementation has resulted in a 130 nm 127 μW oscillator, which locks to the injected carrier frequency. The injection-locked output frequency is 950–1,150 MHz for a −59.6 dBm signal at the antenna input, which is far below the expected signal strength of the RF power signal [51]. To detect whether the oscillator is locked also an averaging phase detector was implemented. Although this results in a perfectly stable output frequency over a large voltage and temperature range, the power consumption of this implementation is rather high for use on a wireless tag (see Fig. 10.1a). Moreover, also a frequency divider is needed to obtain a usable output signal.

The second implementation has been implemented in a 40 nm CMOS technology. The first improvement of this design is the possibility to lock on the low-frequency envelope of the RF carrier instead of the carrier itself. Furthermore, a second improvement was made by adding an injection-locked receiver to receive network coordination commands. This 30 MHz oscillator only consumes 72 μW, including input amplifiers, envelope detectors and 1.8 Mbit receiver (see Fig. 10.1a). Simulations show that a decrease of the sensitivity to around −43 dBm can be expected because of the increased input noise bandwidth. This signal level is in the same order of magnitude as what can be expected for an RF scavenging signal. The use of a non-drifting clock in combination with a coordination receiver results in a huge overhead and power reduction at both transmitter and receiver side of the communication link.

A severe drawback of the current implementations is the lack of selectivity and possible saturation of the input amplifier by interferer signals. Although the coordination receiver prevents the wireless tag from transmitting useless data bursts, the tag can be activated by signals in ‘any’ transmission band. Although in this application it can be assumed that the signal level of the RF power signal transcends any other interferers, a bandpass filter at the receiver input is advisable to remove any unwanted signals. This, however, strongly depends on the environment where the receiver is used.

10.1.4 The Sensor Interface

Finally, also a highly PVT-independent sensor interface has been designed (see Chap. 8). The duty cycle of the output PWM signal relies on the ratio of the stage

delays in a ring oscillator, which is controlled by a sensor signal. Although a frequency drift is expected as a result of external variations, the ratio of the internal delays stays more or less constant. This implementation has been compared to the state of the art in Sect. 8.5.3. It can be concluded that the presented implementation compares well to the state of the art in terms of energy efficiency. The stability over a wide voltage and temperature range (which is unfortunately not investigated in many state of the art references), makes the topology suitable for use in WSN. Furthermore, it has been shown that the topology scales well towards deep-submicron technologies.

10.1.5 The Wireless Tag

Several of the presented building blocks, the injection-locked oscillator with coordination receiver and the sensor interface, have been integrated in a complete wireless tag (see Chap. 9). It has been shown that the combination of the highly-flexible sensor interface, stable clock reference and coordination receiver result in a highly-versatile wireless RFID. To obtain this flexibility and to do the power management and communication within the tag itself, a programmable, low-power digital controller block was implemented. Depending on the wanted or required measurement accuracy, the available energy and the duty cycle of the measurements and communication bursts, the tag can be reprogrammed through a simple shift register.

10.1.6 General Conclusions

The need for temperature- and supply voltage-independent oscillators has been demonstrated in the introduction chapter. It has been shown that the use of a high-Q resonator enables the possibility for a high accuracy without the need for regulation techniques such as switched DC–DC converters. A considerable drawback of these converters is the output noise, which can have a deteriorating impact on the sensitivity of for instance a receiver circuit.

Concerning the design strategy developed in Sect. 4.2.5: It was shown that the use of first-level design techniques can result in highly-stable time references without the overhead of a high power consumption. When de power constraints are less stringent, second-level techniques have been proven to be useful to increase the frequency stability even further. This appears from the comparison to the state of the art in the previous section.

Compensation techniques can also be avoided in the field of sensor interfaces by exploiting the intrinsic relative matching within one oscillator circuit. The PLL-based as well as the PWM-based sensor interface show that this matching results in a PVT-stable measurement. However, the control linearity as well as the phase noise in the oscillator put an upper limit to the effective number of bits. The output noise can be reduced by increasing the power consumption and/or use oversampling techniques.

However, this also increases the power consumption. When a stable supply voltage is available, the traditional interfacing techniques often result in an increased resolution and/or power efficiency as shown in [267].

In recent years, next to ceramic resonators, also cheaper silicon MEMS resonators became available. Due to their high Q factor, these devices quickly gain popularity. The extra production steps to mount these devices on a CMOS chip, result in an increased cost. When comparing to the free-running implementations, this results in an accuracy increase and/or a decreased cost (area) of the CMOS control circuit, which makes these devices a possibly interesting alternative. When a coordination receiver or RF scavenging is used, however, it is believed that the exact time reference which can be derived from this signal, still has significant benefits, be it at the cost of an external antenna.

10.2 Main Contributions

In this section, the main contributions of this work are listed. The contributions are sorted in chronological order.

- Starting from the master thesis work together with former colleague Pieter De Wit, a temperature-independent Wien bridge oscillator has been designed and implemented in 65 nm CMOS. This design relies on a novel highly-stable common-source topology instead of the classical opamp implementation, see Chap. 5 [53, 54].
- A highly supply voltage-independent Wien bridge oscillator has been designed and processed in 130 nm CMOS, see Chap. 5. Main novelties are the use of two nested voltage regulators to obtain a stable supply voltage and the use of two coupled oscillators to eliminate the impact of the regulator's output resistance. The implementation surpasses other available oscillator designs in terms of supply voltage range and supply voltage independence [55].
- A novel pulsed oscillator topology has been invented, relying on a high-Q LC tank. The oscillator uses an alternative driving technique to obtain a highly voltage- and temperature-independent output frequency. Furthermore, this slightly reduces the power consumption of the oscillator circuit. The power consumption in combination with the long-term frequency stability and supply voltage range are unique and surpass other state of the art timing oscillator implementations [56, 62].
- A synchronization technique using a sub-harmonic injection-locked oscillator has been developed, see Chap. 7. Also two averaging phase detectors were developed for detecting a locked condition and to increase the lock range [57].
- A second injection-locked oscillator has been implemented in 40 nm CMOS, Chap. 7. Main novelty is the fact that the timing circuit locks to the AM-envelope of the RF power signal instead of the carrier frequency. A low-power, exact timing reference working over a wide voltage range has been obtained.

- A novel injection-locked receiver topology has been developed. The receiver makes use of the time difference between phase steps in the signal injected into an oscillator. The working principle of this receiver was elaborately studied starting from the theory of injection-locked oscillators [60]. Also a sensitivity analysis of the receiver chain was performed.
- A novel PLL-based sensor interface has been proposed and developed. This has briefly been discussed in Chap. 8. By matching two oscillators, of which one oscillator is sensor dependent, a highly temperature- and supply voltage-independent sensor read-out is obtained [263–265, 279]. Afterwards, this work was continued by colleagues Hans Danneels and Jelle Van Rethy.
- A novel PWM-based sensor interface topology has been developed and implemented. This topology employs the matching between the stage delays within one oscillator to obtain a highly supply voltage- and temperature-independent sensor value [58, 59, 61].
- An ultra-low-power wireless tag has been developed, containing different previously designed building blocks. This has resulted in several implementations in 130 nm CMOS (together with colleague Hans Danneels) [46]. Finally, also a 40 nm flexible wireless tag containing an injection-locked oscillator, a coordination receiver and a PWM-based sensor interface has been developed and implemented.
- An auto-calibrating technique for temperature-independent oscillators has been proposed and developed during a master thesis project (Wouter Steyaert and Pieter Strouven). This technique has briefly been discussed in Chap. 4. The oscillator applies an oscillating temperature to a replica transistor to adapt the oscillator biasing towards a temperature-independent biasing point. This technique is called *Wobbling* [63].
- A novel highly-stable oscillator topology using transmission lines in a Frequency Locked Loop was developed (master thesis of Florian De Roose). The circuit matches the delay of a transmission line to the delay of an oscillator stage [50].

10.3 Suggestions for Future Work

Different novel oscillator topologies designed for PVT-independence were presented. One of the main disadvantages is the lack of absolute accuracy of the free-running oscillator implementations. Since cost is one of the most important constraints in WSNs, an efficient production or calibration technique to solve this accuracy problem needs to be found.

Another problem with the implemented free-running frequency references is the chip integration. Even in literature, without trimming, none of the fully-integrated designs delivers the required temperature- and supply voltage-stability. Furthermore, an increased accuracy is mostly at the expense of an increased power consumption. Alternative circuit topologies and/or technologies (such as printed inductors, MEMS resonators, etc.) need to be explored.

Alternatively, injection-locked topologies can be used. An unsolved problem here is the frequency selectivity of the presented structures. Except for the lock range of the oscillator, no bandpass filtering or frequency selectivity mechanism is present. In the first implementation (the injection-locked oscillator in 130 nm), this problem can be solved using a bandpass filter at the input. External filters, for instance a SAW- or BAW-filter, however, result in an unwanted cost increase. Also in the second implementation, which makes use of a coordination receiver to increase the robustness, this poses a problem. The receiver circuit is sensitive to signals in 'any' frequency band. A more elaborate study on the injection-locked receiver topology is needed to develop more optimized and robust implementations of this receiver.

Another issue is the use of external antennas for the reception of the 2.4 GHz power and clock signal. Typically, the size of these antennas is around 10 cm, which is too much in many applications. Circuit techniques need to be found to avoid (or reduce the size of) these external antenna, without deteriorating the sensitivity and/or the power consumption. As already mentioned in the introduction, the physical size constraints of an antenna are difficult or even impossible to overcome.

The problem of a low-power wake-up receiver also remains unsolved. When relying on RF-scavenging as an energy source, the power consumption of the available wake-up receiver topologies is just too high for continuous use on a sensor node. At the moment, these receivers also need to be duty-cycled and can only be used to avoid data collisions.

Some of these remaining disadvantages can also be solved in other components of the WSN. Alternative (UWB-)receiver topologies or protocols can be found requiring a lower clock accuracy at the transmitter side. While doing so, the complete power-budget of the transmitter needs to be taken into account instead of only looking at the clock accuracy. Secondly, also an increased power budget, i.e. an improvement of the energy scavenging, energy storage and voltage conversion (DC-DC converters) on the tags, can allow a performance increase of all circuitry on the tag. This will have a repercussion on the performance of the complete WSN. Last but not least, a lot of work needs to be done in the field of network coordination, data capturing and data processing. When thousands of sensors are operational within the same room, this huge amount of data needs to be collected and processed in an efficient way to obtain an adaptive, responsive and smart environment.

Appendix A
Definitions and Conventions Used Throughout the Work

This appendix contains the definitions and conventions which are used throughout the work. They are ordered in the way they are used in the text. In some cases, more than one, slightly different, definition is available for the same subject. In this case a choice is made and if needed, it will be argued why this particular definition is chosen.

A.1 The Fourier Transform and Fourier Series

A signal can be represented in the time domain as well as in the frequency domain. A difference is made between non-periodic and periodic waveforms.

A.1.1 Non-periodic Waveforms

To obtain the frequency spectrum of a signal, the Fourier transform is used [34]:

Definition A.1 The Fourier transform of a waveform $w(t)$ is:

$$W(f) = \mathcal{F}[w(t)] = \int_{-\infty}^{\infty} w(t) \cdot e^{-j \cdot 2 \cdot \pi \cdot f \cdot t} dt \tag{A.1}$$

where $\mathcal{F}[w(t)]$ denotes the Fourier transform of $w(t)$ and f is the frequency parameter with units of Hz. This *defines* the term frequency, which is the parameter f in the Fourier transform.

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Note that instead of the frequency, also the angular frequency $\omega = 2 \cdot \pi \cdot f$ can be used in the Fourier transform. Although this sometimes simplifies the mathematics, it is less intuitive when measuring for instance a spectrum with a spectrum analyzer. The Fourier transform results in a *two-sided* spectrum since both positive and negative frequencies are obtained from the definition. Often the Fourier transform of a waveform is split in a magnitude and a phase function:

$$W(f) = |W(f)| \cdot e^{j \cdot \theta(f)} \tag{A.2}$$

$$\text{in which: } |W(f)| = \sqrt{\Im[W(f)]^2 + \Re[W(f)]^2} \tag{A.3}$$

$$\text{and: } \theta(f) = \arctan\left(\frac{\Im[W(f)]}{\Re[W(f)]}\right) \tag{A.4}$$

which is called the *polar form* of the Fourier transform. The inverse Fourier transform can be used to, starting from a complex frequency spectrum, obtain the original waveform:

Definition A.2 The inverse Fourier transform of a frequency spectrum $F(f)$ is:

$$w(t) = \mathscr{F}^{-1}[W(f)] = \int_{-\infty}^{\infty} W(f) \cdot e^{j \cdot 2 \cdot \pi \cdot f \cdot t} df \tag{A.5}$$

where $\mathscr{F}^{-1}[W(f)]$ denotes the Inverse Fourier transform of $W(f)$.

$w(t)$ and $W(f)$ are called Fourier pairs. The existence of the Fourier transform of a waveform is, however, not always guaranteed since the infinite integral can diverge. Different conditions can be used to check whether the Fourier transform exists for a waveform $w(t)$. These conditions are all *sufficient*, but *not necessary* [34]:

- $w(t)$ is absolutely integrable:

$$\int_{-\infty}^{\infty} |w(t)| dt < \infty \tag{A.6}$$

  and, over any time interval of finite width, the function $w(t)$ is a single-valued function with a finite number of maxima and minima, and the number of discontinuities (if any) is finite.
- The normalized energy (2-norm) of the waveform is finite:

$$E = \int_{-\infty}^{\infty} |w(t)|^2 dt < \infty \tag{A.7}$$

The first conditions are called the *Dirichlet conditions*, the second is the finite-energy condition which is somewhat weaker and satisfied for every physical waveform!

A.1.1.1 Properties of the Fourier transform

When doing calculations with waveforms or when calculating the spectrum of a waveform, different properties can be useful. Some of them are briefly summarized in this section, a more complete overview can be found in [34].

- The spectrum of a real waveform is symmetrical:

$$W(-f) = \overline{W(f)} \tag{A.8}$$

  in which $\overline{W(f)}$ is the complex conjugate. When using the polar notation, this means:

$$W(-f) = |W(f)| \cdot e^{-j\cdot\theta(f)} \tag{A.9}$$

- The frequency f is just a parameter of the Fourier transform that specifies the frequency of interest. The Fourier transform looks for this frequency over all time $-\infty < t < \infty$.
- $W(f)$ can be complex, also for real waveforms $w(t)$.
- Linearity: $\mathscr{F}[a_1 \cdot f(t) + a_2 \cdot g(t)] = a_1 \cdot F(f) + a_2 \cdot G(f)$
- Time delay: $\mathscr{F}[w(t-\tau)] = W(f) \cdot e^{-j\cdot\omega\cdot\tau}$
- Complex signal frequency translation: $\mathscr{F}[w(t) \cdot e^{j\cdot\omega_c\cdot t}] = W(f - f_c)$
- Differentiation:

$$\mathscr{F}\left[\frac{d^n w(t)}{dt^n}\right] = (j \cdot 2 \cdot \pi \cdot f)^n \cdot W(f) \tag{A.10}$$

- Integration:

$$\mathscr{F}\left[\int_{-\infty}^{t} w(t)\right] = (j \cdot 2 \cdot \pi \cdot f)^{-1} \cdot W(f) + \frac{1}{2} \cdot W(0) \cdot \delta(f) \tag{A.11}$$

- Convolution:

$$\mathscr{F}\left[f(t) * g(t)\right] = F(f) \cdot G(f) \tag{A.12}$$

- Multiplication:

$$\mathscr{F}\left[f(t) \cdot g(t)\right] = F(f) * G(f) \tag{A.13}$$

Extra attention is needed for a commonly used property of a signal and its Fourier transform, called *Parseval's theorem*:

Theorem A.1 *For two signals $f(t)$ and $g(t)$, with Fourier transforms $F(f)$ and $G(f)$:*

$$\int_{-\infty}^{\infty} f(t) \cdot \overline{g(t)} dt = \int_{-\infty}^{\infty} F(f) \cdot \overline{G(f)} df \tag{A.14}$$

where $\overline{g(t)}$ denotes the complex conjugate of $g(t)$. When $f(t) = g(t)$, this reduces to:

$$\int_{-\infty}^{\infty} |f(t)|^2 dt = \int_{-\infty}^{\infty} |F(f)|^2 df \tag{A.15}$$

which is known as Rayleigh's energy theorem.

A.1.2 Periodic Waveforms

It can be shown that a waveform $w(t)$ can be represented by a sum of orthogonal functions $\varphi_n(t)$ in the interval (a, b) using the following theorem [34]:

Theorem A.2 *$w(t)$ can be represented over the interval (a, b) by the series*

$$w(t) = \sum_n a_n \cdot \varphi_n(t) \tag{A.16}$$

where the orthogonal coefficients are given by

$$a_n = \frac{1}{K_n} \cdot \int_a^b w(t) \cdot \overline{\varphi_n(t)} dt \tag{A.17}$$

$$and{:}K_n = \int_a^b \varphi_n(t) \cdot \overline{\varphi_n(t)} dt \tag{A.18}$$

and the range of n is over the integer values that correspond to the subscripts that where used to denote the orthogonal functions in the complete orthogonal set.

A complete set $\{\varphi_n(t)\}$ of orthogonal functions means that any function can be represented with an arbitrarily small error using the functions in $\{\varphi_n(t)\}$. This is, however, difficult to prove. A set of complex exponential functions and a set of harmonic sinusoids can, however, be proven to be complete [36]. These sets are used to define the Fourier series.

Theorem A.3 *A physical waveform can be represented over the interval $a < t < a + T_0$ by the complex exponential Fourier series*

$$w(t) = \sum_{n=-\infty}^{n=\infty} c_n \cdot e^{j \cdot n \cdot \omega_0 \cdot t} \tag{A.19}$$

where the complex Fourier coefficients are:

$$c_n = \frac{1}{T_0} \cdot \int_a^{a+T_0} w(t) \cdot e^{-j \cdot n \cdot \omega_0 \cdot t} dt \tag{A.20}$$

and where $\omega_0 = 2 \cdot \pi \cdot f_0 = 2 \cdot \pi / T_0$.

For waveforms which are periodic with period T_0, this Fourier series is a representation of the function over all time because all functions of the orthogonal set are periodic with the same fundamental period as $w(t)$, T_0. The Fourier series can therefore be seen as a special case of the Fourier transform for periodic functions. The spectrum in this case consists of discrete lines at the harmonic frequencies. Also the properties of the Fourier transform can be used for the Fourier series:

- If $w(t)$ is real, $c_n = \overline{c_{-n}}$
- If $w(t)$ is real and $w(t) = w(-t)$, $\Im[c_n] = 0$
- If $w(t)$ is real and $w(t) = -w(-t)$, $\Re[c_n] = 0$
- Parseval's theorem is:

$$\frac{1}{T_0} \cdot \int_a^{a+T_0} |w(t)|^2 dt = \sum_{n=-\infty}^{n=\infty} |c_n|^2 \tag{A.21}$$

In some applications it can be useful to use the *quadrature* form of the Fourier series:

Theorem A.4 *A physical waveform $w(t)$ can be represented over the interval $a < t < a + T_0$ by a sum of sinusoids:*

$$w(t) = \sum_{n=0}^{n=\infty} a_n \cdot \cos(n \cdot \omega_0 \cdot t) + \sum_{n=1}^{n=\infty} b_n \cdot \sin(n \cdot \omega_0 \cdot t) \tag{A.22}$$

where the orthogonal functions are $\sin(n \cdot \omega_0 \cdot t)$ *and* $\cos(n \cdot \omega_0 \cdot t)$*, and the coefficients are given by:*

$$a_n = \begin{cases} \frac{1}{T_0} \cdot \int_a^{a+T_0} w(t) dt & \text{for } n = 0 \\ \frac{2}{T_0} \cdot \int_a^{a+T_0} w(t) \cdot \cos(n \cdot \omega_0 \cdot t) dt & \text{for } n \geq 1 \end{cases} \tag{A.23}$$

and:

$$b_n = \frac{2}{T_0} \cdot \int_a^{a+T_0} w(t) \cdot \sin(n \cdot \omega_0 \cdot t) dt \quad \text{for } n \geq 1 \tag{A.24}$$

The relation between the coefficients of the complex and the quadrature Fourier series is:

$$a_n = \begin{cases} c_0 & \text{for } n = 0 \\ 2 \cdot \Re(c_n) & \text{for } n \geq 1 \end{cases} \tag{A.25}$$

and,

$$b_n = -2 \cdot \Im(c_n) \quad \text{for } n \geq 1 \tag{A.26}$$

A last form of the Fourier series is the polar form:

Theorem A.5 *A physical waveform $w(t)$ can be represented over the interval $a < t < a + T_0$ by a sum of sinusoids:*

$$w(t) = D_0 + \sum_{n=1}^{n=\infty} D_n \cdot \cos(n \cdot \omega_0 \cdot t + \varphi_n) \tag{A.27}$$

where $w(t)$ is real and:

$$D_n = \begin{cases} a_0 = c_0 & \textit{for } n = 0 \\ \sqrt{a_n^2 + b_n^2} = 2 \cdot |c_n| & \textit{for } n \geq 1 \end{cases} \tag{A.28}$$

and:

$$\varphi_n = -arctan\left(\frac{b_n}{a_n}\right) = \angle c_n \quad \textit{for } n \geq 1 \tag{A.29}$$

In this work, both the complex and the quadrature form of the Fourier series are used, depending on the situation. It is clear that both forms have their benefits: the ease of mathematical calculations for the complex waveform and the intuitive approach of the quadrature and polar form.

A.2 The Autocorrelation and PSD of a Signal

The autocorrelation and the Power Spectral Density (PSD) of a time signal contain the same information about a signal since the PSD of a random signal is defined as the Fourier transform of its autocorrelation function [41]. Before formulating the formulas of the autocorrelation and the PSD, the definitions of a stationary signal and an ergodic signal are needed:

Definition A.3 A random process $x(t)$ is said to be stationary to the order N if, for any $t_1, t_2, ..., t_N$:

$$f_x(x(t_1), x(t_2), ..., x(t_N)) = f_x(x(t_1 + t_0), x(t_2 + t_0), ..., x(t_N + t_0)) \tag{A.30}$$

where t_0 is an arbitrary real constant and $f_x(\mathbf{x})$ is an N-dimensional Probability Density Function (PDF). The process is said to be strictly stationary if it is stationary to the order $N \to \infty$.

The first-order stationarity of a random process can thus easily be checked by determining whether its first-order PDF is a function of time.

Definition A.4 A random process is said to be ergodic if all time averages of any sample function are equal to the corresponding ensemble averages (expectations).

Since ergodicity is not the most straightforward concept to understand, an example is given to illustrate this:

Example A.1 In electrical engineering, two commonly used averages are the **dc** and **rms** values. These values are both defined (and measured) as time averages. However, when the process is ergodic, also ensemble averages can be used.

- The dc value of a random process $x(t)$ is by definition equal to:

$$x_{dc} \triangleq \lim_{T\to\infty} \frac{1}{T} \cdot \int_{-T/2}^{T/2} [x(t)]dt \tag{A.31}$$

  which is, in the case of an ergodic process, equivalent to:

$$E[x(t)] = \int_{-\infty}^{\infty} [x \cdot f_x(x)]dx = m_x \tag{A.32}$$

  where $E[x(t)]$ or m_x is the expected or mean value of $x(t)$.
- The rms value of a random process $x(t)$ is by definition equal to:

$$x_{rms} \triangleq \sqrt{\lim_{T\to\infty} \frac{1}{T} \cdot \int_{-T/2}^{T/2} [x(t)^2]dt} \tag{A.33}$$

  which is, in the case of an ergodic process, equivalent to:

$$\sqrt{E[x(t)^2]} = \sqrt{\sigma_x^2 + m_x^2} \tag{A.34}$$

where $E[x(t)^2]$ is the expected or mean value of $x(t)^2$ and σ_x^2 is the variance of $x(t)$.

A.2.1 The Autocorrelation

The autocorrelation of a signal is defined as the correlation between the signal and a time-shifted version of itself.

Definition A.5 The autocorrelation of a quadratically infinitely integrable signal $f(t)$ is most often defined as the continuous cross-correlation of the signal with itself:

$$R_f(\tau) = \int_{-\infty}^{\infty} f(t) \cdot \overline{f(t-\tau)} dt \tag{A.35}$$

$$= \int_{-\infty}^{\infty} f(t+\tau/2) \cdot \overline{f(t-\tau/2)} dt \tag{A.36}$$

$$= \int_{-\infty}^{\infty} f(t+\tau) \cdot \overline{f(t)} dt \tag{A.37}$$

where $\overline{f(t)}$ is the complex conjugate of $f(t)$. For real signals this complex conjugate can be omitted.

For signals which last forever and are therefore often not quadratically infinitely integrable, an alternative definition of the autocorrelation is used:

Definition A.6

$$R_f(\tau) = \lim_{T\to\infty} \frac{1}{T} \cdot \int_{-T/2}^{T/2} \overline{f(t)} \cdot f(\tau - t) dt \tag{A.38}$$

when $f(t)$ is ergodic or stationary in the wide sense.

In this thesis, since most of the discussed signals are oscillator outputs which can last forever, definition (A.6) is used.

A.2.2 The Power Spectral Density

The power spectral density of a signal is a representation of the power in a signal in the frequency domain. It can be defined as the Fourier transform of the autocorrelation function of the signal (the *Wiener-Khinchine* theorem) [34]:

Definition A.7 The Power Spectral Density of a signal $f(t)$ with autocorrelation function $R_f(\tau)$ is calculated as the Fourier transform of $R_f(\tau)$:

$$S_f(\omega) = \int_{-\infty}^{\infty} R_f(\tau) \cdot e^{-j \cdot \omega \cdot \tau} d\tau \tag{A.39}$$

It follows that the autocorrelation of a signal $f(t)$ with PSD $S_f(\omega)$ can be calculated as:

$$R_f(\omega) = \frac{1}{2 \cdot \pi} \cdot \int_{-\infty}^{\infty} R_f(\tau) \cdot e^{j \cdot \omega \cdot \tau} d\tau \tag{A.40}$$

The power of a signal in a certain frequency band $[\omega_1, \omega_2]$ can then be calculated by integrating over positive as well as negative frequencies:

$$P_{\omega_1,\omega_2} = \int_{\omega_1}^{\omega_2} (S_f(\omega) + S_f(-\omega)) d\omega \tag{A.41}$$

For real signals, the PSD is symmetrical around zero. Alternatively, the power spectral density can be defined as follows:

Definition A.8 The average power in a signal $f(t)$ is defined as:

$$\mathscr{P}\{f(t)\} = \lim_{T \to \infty} \frac{1}{T} \cdot \int_{-T/2}^{T/2} |f(t)|^2 dt \tag{A.42}$$

Let:

$$f_T(t) = f(t) \cdot \Pi\left(\frac{t}{T}\right) \tag{A.43}$$

and using Parseval's theorem, this can be written as:

$$\mathscr{P}\{f(t)\} = \lim_{T\to\infty} \frac{1}{T} \cdot \int_{-\infty}^{\infty} |F_T(f)|^2 df \tag{A.44}$$

$$= \int_{-\infty}^{\infty} S_f(f) df \tag{A.45}$$

where

$$S_f(f) = \lim_{T\to\infty} \frac{1}{T} \cdot |F_T(f)|^2 \tag{A.46}$$

is called the *Power Spectral Density*.

It must be noted that both definitions lead to exactly the same result. The first calculation method is often called the *indirect* calculation method; the second, *direct*, calculation method has no need for calculating the autocorrelation first. The unit of the PSD is *watt per hertz*, W/Hz. For practical reasons mostly the single-sided PSD is used, as will be indicated throughout the work.

A.3 Generalized and Special Functions

In this section some of the commonly used functions are defined in order to avoid any confusion with other definitions which are sometimes used. The definitions used are the same as in [34].

A.3.1 The Dirac Delta Function

Definition A.9 The Dirac delta function $\delta(x)$ is defined by:

$$\int_{-\infty}^{\infty} w(x) \cdot \delta(x) = w(0) \tag{A.47}$$

where $w(x)$ is a continuous function at $x = 0$.

Depending on the application x can be time or frequency or some other variable. An alternative definition of $\delta(x)$ is:

Definition A.10 The Dirac delta function $\delta(x)$ is defined by:

$$\int_{-\infty}^{\infty} \delta(x) = 1 \tag{A.48}$$

and:

$$\delta(x) = \begin{cases} \infty & \text{for } x = 0 \\ 0 & \text{for } x \neq 0 \end{cases} \tag{A.49}$$

Since the Dirac function is not a real function (it contains singularities), it is called a singular function. In some situations, it can be useful to use the equivalent integral of the δ function:

$$\delta(x) = \int_{-\infty}^{\infty} e^{\pm j \cdot 2 \cdot \omega \cdot x \cdot y} dy \tag{A.50}$$

This can be proven by noting that the Fourier transform of the delta function is equal to 1. By calculating the inverse Fourier transform, the equivalent integral is obtained.

A.3.2 The Step Function

The step or Heaviside function is often used when calculating Laplace transforms.

Definition A.11 The unit step function $u(t)$ is

$$u(t) = \begin{cases} 1 & \text{for } t > 0 \\ 0 & \text{for } t < 0 \end{cases} \tag{A.51}$$

The relation between the unit step function and the Dirac function is:

$$\int_{-\infty}^{t} \delta(x)dx = u(t) \tag{A.52}$$

$$\frac{du(t)}{t} = \delta(t) \tag{A.53}$$

The Fourier transform of the unit step function is equal to:

$$\mathscr{F}[u(t)] = \frac{1}{2} \cdot \delta(f) + \frac{1}{j \cdot 2 \cdot \pi \cdot f} \tag{A.54}$$

A.3.3 A Rectangular Pulse

A rectangular pulse is often used to consider a function only over a certain interval.

Definition A.12 Let $\Pi[\cdot]$ denote a single rectangular pulse with duration T, then:

$$\Pi\left[\frac{t}{T}\right] \triangleq \begin{cases} 1, & |t| \leq \frac{T}{2} \\ 0, & |t| > \frac{T}{2} \end{cases} \tag{A.55}$$

The Fourier transform of this function is equal to the *sinc* function:

$$\text{sinc}(x) = \frac{\sin(x)}{x} \tag{A.56}$$

which makes:

$$\mathscr{F}\left[\Pi\left(\frac{t}{T}\right)\right] = T \cdot \text{sinc}(\pi \cdot T \cdot f) \tag{A.57}$$

Note that the definition of a Dirac impulse sometimes uses this rectangular pulse:

$$\delta(t) = \lim_{T \to 0} \frac{1}{T} \cdot \Pi\left[\frac{t}{T}\right] \tag{A.58}$$

It is easy to confirm that the properties mentioned above indeed hold for this definition.

A.3.4 A Triangular Pulse

The triangular function is defined as follows.

Definition A.13 Let $\Lambda[\cdot]$ denote the triangular function:

$$\Lambda\left[\frac{t}{T}\right] \triangleq \begin{cases} 1 - \frac{|t|}{T}, & |t| \leq T \\ 0, & |t| > T \end{cases} \tag{A.59}$$

The Fourier transform of this function is equal to:

$$\mathscr{F}\left[\Lambda\left(\frac{t}{T}\right)\right] = T \cdot \text{sinc}(\pi \cdot T \cdot f)^2 \tag{A.60}$$

Indeed, a triangular pulse can be constructed by the convolution of two rectangular pulses. Also this function is sometimes used to define the Dirac impulse:

$$\delta(t) = \lim_{T \to 0} \frac{1}{T} \cdot \Lambda\left[\frac{t}{T}\right] \tag{A.61}$$

A.3.5 The Derivative Triangular Pulse

A last function is the derivative of the triangular pulse. It is defined as:

Definition A.14 Let $\Xi[\cdot]$ denote the derivative triangular function:

$$\Xi\left[\frac{t}{T}\right] \triangleq \begin{cases} \frac{1}{T}, & T \leq t \leq 0 \\ \frac{-1}{T}, & 0 < t \leq T \\ 0, & |t| > T \end{cases} \tag{A.62}$$

The Fourier transform of this function is equal to:

$$\mathscr{F}\left[\Xi\left(\frac{t}{T}\right)\right] = 2 \cdot T \cdot \frac{\sin(\pi \cdot T \cdot f)^2}{-j \cdot \pi \cdot T \cdot f} \tag{A.63}$$

Appendix B
Influence of a Nonlinear Amplifier

This appendix explains some parts of the discussion in Sect. 4.2 on the influence of a nonlinear amplifier on the frequency of a harmonic oscillator. Especially the lengthy mathematical derivations are omitted in the text and derived here.

B.1 Derivation of Eq. (4.37)

In Sect. 4.2 it is shown that when the applied current waveform is known, the resulting frequency shift for a certain feedback network is given by (4.27):

$$\Im\left[Z_1\right] + \sum_{2}^{\infty} \Im\left[k \cdot Z_k\right] \cdot \delta_k^2 = 0 \tag{B.1}$$

where $\delta_k = I_k / I_1$ is the ratio of the harmonics and the fundamental component of the applied current. Z_k is the impedance of the tuned feedback network at the frequency $k \cdot \omega_0$ where ω_0 is the fundamental angular frequency of the oscillator. Assume a parallel RLC network with transfer function (2.66):

$$H_P(s) = \frac{\frac{s}{C}}{s^2 + \frac{1}{C \cdot R_P} \cdot s + \frac{1}{L \cdot C}} = \frac{\omega_n \cdot \sqrt{\frac{L}{C}} \cdot s}{s^2 + \frac{\omega_n}{Q} \cdot s + \omega_n^2} \tag{B.2}$$

When substituting $s = j \cdot k \cdot \omega_0$, the imaginary part of the resulting impedance is equal to:

$$\Im[Z_k] = \frac{-k \cdot \omega_0 \cdot Q^2 \cdot (k^2 \cdot \omega_0^2 - \omega_n^2)}{C \cdot (k^4 \cdot \omega_0^4 \cdot Q^2 - 2 \cdot k^2 \cdot Q^2 \cdot \omega_0^2 \cdot \omega_n^2 + \omega_n^4 \cdot Q^2 + k^2 \cdot \omega_0^2 \cdot \omega_n^2)} \tag{B.3}$$

V. De Smedt et al., *Temperature- and Supply Voltage-Independent Time References for Wireless Sensor Networks*, Analog Circuits and Signal Processing 128,
DOI 10.1007/978-3-319-09003-0

When $k = 1$, this equation simplifies to:

$$\Im[Z_1] = \frac{-\omega_0 \cdot Q^2 \cdot (\omega_0 + \omega_n) \cdot (\omega_0 - \omega_n)}{C \cdot (\omega_0^4 \cdot Q^2 - 2 \cdot Q^2 \omega_0^2 \cdot \omega_n^2 + \omega_n^4 \cdot Q^2 + \omega_0^2 \cdot \omega_n^2)} \tag{B.4}$$

$$= \frac{-\omega_0 \cdot Q^2 \cdot (\omega_0 + \omega_n) \cdot \Delta\omega_0}{C \cdot (\omega_0^4 \cdot Q^2 - 2 \cdot Q^2 \omega_0^2 \cdot \omega_n^2 + \omega_n^4 \cdot Q^2 + \omega_0^2 \cdot \omega_n^2)} \tag{B.5}$$

where $\Delta\omega_0 = \omega_0 - \omega_n$. Apart from the factor $\Delta\omega_0$, which is close to zero, it can be assumed that $\omega_0 \approx \omega_n$:

$$\Im[Z_1] \approx \frac{2 \cdot Q^2 \cdot \Delta\omega_0}{C \cdot \omega_n^2} \tag{B.6}$$

When $k \neq 1$, it can also be assumed that $\omega_0 \approx \omega_n$:

$$\Im[Z_k] = \frac{-k \cdot \omega_n^3 \cdot Q^2 \cdot (k^2 - 1)}{C \cdot (k^4 \cdot \omega_n^4 \cdot Q^2 - 2 \cdot k^2 \cdot Q^2 \cdot \omega_n^4 + \omega_n^4 \cdot Q^2 + k^2 \cdot \omega_n^4)} \tag{B.7}$$

$$= \frac{-k \cdot (k^2 - 1)}{C \cdot \omega_n \cdot (\frac{k^2}{Q^2} + k^4 - 2 \cdot k^2 + 1)} \tag{B.8}$$

$$= \frac{-k \cdot (k^2 - 1)}{C \cdot \omega_n \cdot (\frac{k^2}{Q^2} + (k^2 - 1)^2)} \tag{B.9}$$

When $Q \gg 1$ this simplifies to:

$$\Im[Z_k] = \frac{-k \cdot (k^2 - 1)}{C \cdot \omega_n \cdot (k^2 - 1)^2} = \frac{-k}{C \cdot \omega_n \cdot (k^2 - 1)} \tag{B.10}$$

The estimated frequency deviation, using (4.27), results in Eq. (4.37):

$$\frac{\Delta\omega_0}{\omega_n} = -\frac{1}{2 \cdot Q^2} \cdot \sum_{k=2}^{\infty} \frac{k^2}{k^2 - 1} \cdot \delta_k^2 \tag{B.11}$$

B.2 Waveform in a Nonlinear Harmonic Oscillator

In this section the waveform of a harmonic oscillator with a softly nonlinear amplifier is calculated. This, however, is not an easy task. Instead of the linear oscillator in Fig. B.1a, an oscillator with a linear feedback network (which is mostly the case) and with a nonlinear amplifier is studied, Fig. B.1b. The representation of this oscillator, using s-functions, is not correct since the amplifier is no longer a linear building block.

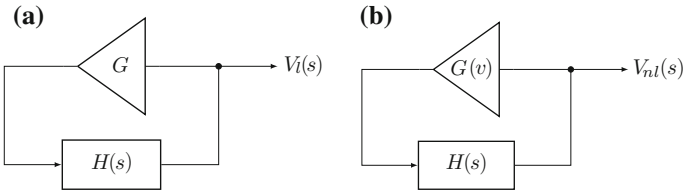

Fig. B.1 Typical block diagram of a harmonic (linear) oscillator (**a**). An oscillator with a linear feedback network and a nonlinear amplifier (**b**)

Similar to the calculations in Sect. 4.2.2, the calculations start with the Fourier series of the nonlinear, but periodic, output waveform:

$$v(t) = \sum_{k=-\infty}^{+\infty} c_k \cdot e^{j \cdot k \cdot \omega_0 \cdot t} \tag{B.12}$$

where, for real waveforms, $c_{-k} = \overline{c_k}$ and ω_0 is the fundamental frequency. This expression will be used to calculate the output current of the transconductance amplifier, which is the input current of the feedback network.

B.2.1 The Feedback Network

This waveform results from the injection of a current into the feedback network $H(s)$. Since the feedback network is assumed to be completely linear, the injected current can easily be calculated by dividing each frequency component c_k of the output voltage by the complex impedance $H(s)$ of the feedback network:

$$V(s) = I(s) \cdot H(s) \tag{B.13}$$

$$\Rightarrow i(t) = \sum_{k=-\infty}^{+\infty} \frac{c_k}{H(j \cdot k \cdot \omega_0)} \cdot e^{j \cdot k \cdot \omega_0 \cdot t} \tag{B.14}$$

For a parallel RLC feedback network, the transfer function can be written as:

$$H(s) = \frac{\frac{s}{C}}{s^2 + \frac{\omega_n}{Q} \cdot s + \omega_n^2} \tag{B.15}$$

where ω_n is the natural frequency of the feedback network and Q represents the quality factor. Since, for the steady-state behavior of the network:

$$1/H(j \cdot k \cdot \omega_0) = \left[j \cdot k \cdot \omega_0 \cdot C + \frac{\omega_n \cdot C}{Q} + \frac{C \cdot \omega_n^2}{j \cdot k \cdot \omega_0} \right] \tag{B.16}$$

$$= \frac{\omega_n \cdot C}{Q} \cdot \left[1 + j \cdot \left(\frac{k \cdot \omega_0 \cdot Q}{\omega_n} - \frac{Q \cdot \omega_n}{k \cdot \omega_0} \right) \right] \tag{B.17}$$

when the frequency deviation due to the nonlinearity of the amplifier is small compared to the natural frequency ω_n, this results in:

$$\frac{1}{H(j \cdot k \cdot \omega_0)} \approx \frac{\omega_n \cdot C}{Q} \cdot \left[1 + j \cdot k \cdot Q \left(1 - \frac{1}{k^2} \right) \right] \tag{B.18}$$

$$= \frac{\omega_n \cdot C}{Q} \cdot \sqrt{1 + k^2 \cdot Q^2 \cdot \left(1 - \frac{1}{k^2} \right)^2} \cdot e^{j \arctan(kQ(1-1/k^2))} \tag{B.19}$$

The complex impedance (conductance) experienced by each harmonic can be calculated with this formula.

B.2.2 The Nonlinear Amplifier

Another relationship between the voltage over the feedback network and the injected current is the amplifier characteristic. Although the Barkhausen criterion (Theorem 2.2) is only valid for linear systems, similar conclusions can be drawn for nonlinear systems. Since it is assumed that the oscillator's output signal is periodic and has a stable amplitude, the current-voltage relationship of both the feedback network and the amplifier must be the same! This equality results in, similar to what the Barkhausen criterion does for linear systems, the oscillator equation:

$$G(v(t)) = i(t) = \sum_{k=-\infty}^{+\infty} \frac{c_k}{H(j \cdot k \cdot \omega_0)} \cdot e^{j \cdot k \cdot \omega_0 \cdot t} \tag{B.20}$$

Solving this equation, if possible, results in the steady-state waveform of the oscillator. Note that startup behavior and transition effects are not taken into account in this equation. An amplifier with the following transfer characteristic is assumed:

$$G(v) = A_1 \cdot v + A_3 \cdot v^3 \tag{B.21}$$

where A_1 and A_3 are real coefficients determining the gain and nonlinearity of the amplifier and v is the input voltage. In order to obtain a stable output waveform, limited by the nonlinearity in the amplifier, A_1 must be positive and A_3 negative. Furthermore, to guarantee the startup of the oscillator, the gain for small input signals A_1 needs to compensate for the attenuation in the tank around the oscillation frequency ω_0. This amplifier characteristic, which is perfectly symmetric, is typical for differential circuits. It results in only odd harmonics in the output waveform.

B.2.2.1 Signals with an Infinite Bandwidth

In a first attempt to calculate the resulting waveform, one can try to insert the Fourier series of the voltage output signal into the amplifier characteristic. This, however, results in an infinite sum of cross products which is rather difficult to handle:

$$G(v(t)) = A_1 \cdot \sum_{k=-\infty}^{+\infty} c_k \cdot e^{j\cdot k\cdot \omega_0 \cdot t} + A_3 \cdot \sum_{k=-\infty}^{+\infty} c_k^3 \cdot e^{j\cdot 3\cdot k\cdot \omega_0 \cdot t} \tag{B.22}$$

$$+ 3 \cdot A_3 \cdot \sum_{k=-\infty}^{+\infty} \left\{ c_k \cdot e^{j\cdot k\cdot \omega_0 \cdot t} \cdot \sum_{l=-\infty}^{+\infty, l\neq k} c_l^2 \cdot e^{j\cdot 2\cdot k\cdot \omega_0 \cdot t} \right\} \tag{B.23}$$

This means that an infinite set of equations is needed to be solved to obtain all Fourier coefficients c_k. An alternative method is calculating the coefficients numerically in an iterative way. As will be shown, however, limiting the bandwidth of the output signal results in a solution with an acceptable accuracy.

B.2.2.2 Bandwidth-Limited Signals

A smarter approach is to assume that the output signal is band limited. A periodic voltage waveform, containing only the first, third and fifth harmonic, is assumed:

$$v(t) = \sum_{k=-5,-3,\ldots 5} c_k \cdot e^{j\cdot k\cdot \omega_0 \cdot t} \tag{B.24}$$

$$\begin{aligned}
G(v(t)) = {} & A_3 \cdot \overline{c_5}^3 \cdot e^{-15\cdot \omega_0 \cdot t} + 3 \cdot A_3 \cdot \overline{c_3} \cdot \overline{c_5}^2 \cdot e^{-13\cdot j\cdot \omega_0 \cdot t} \\
& + 3 \cdot A_3 \cdot (\overline{c_3}^2 \cdot \overline{c_5} + \overline{c_1} \cdot \overline{c_5}^2) \cdot e^{-11\cdot j\cdot \omega_0 \cdot t} \\
& + A_3 \cdot (\overline{c_3}^3 + 3 \cdot c_1 \cdot \overline{c_5}^2) \cdot e^{-9\cdot j\cdot \omega_0 \cdot t} \\
& + 3 \cdot A_3 \cdot (\overline{c_1}^2 \cdot \overline{c_5} + \overline{c_1} \cdot \overline{c_3}^2 + c_3 \cdot \overline{c_5}^2) \cdot e^{-7\cdot j\cdot \omega_0 \cdot t} \\
& + [A_1 \cdot \overline{c_5} + 3 \cdot A_3 \cdot (\overline{c_1}^2 \cdot \overline{c_3} + c_1 \cdot \overline{c_3}^2 + c_5 \cdot \overline{c_5}^2)] \cdot e^{-5\cdot j\cdot \omega_0 \cdot t} \\
& + [A_1 \cdot \overline{c_3} + A_3 \cdot \overline{c_1}^3 + 3 \cdot A_3 \cdot (c_1^2 \cdot \overline{c_5} + c_3 \cdot \overline{c_3}^2)] \cdot e^{-3\cdot j\omega_0 \cdot t} \\
& + [A_1 \cdot \overline{c_1} + 3 \cdot A_3 \cdot (c_1 \cdot \overline{c_1}^2 + \overline{c_3}^2 \cdot c_5)] \cdot e^{-1\cdot j\cdot \omega_0 \cdot t} \\
& + [A_1 \cdot c_1 + 3 \cdot A_3 \cdot (\overline{c_1} \cdot c_1^2 + c_3^2 \cdot \overline{c_5})] \cdot e^{1\cdot j\cdot \omega_0 \cdot t} \\
& + [A_1 \cdot c_3 + A_3 \cdot c_1^3 + 3 \cdot A_3 \cdot (\overline{c_1}^2 \cdot c_5 + \overline{c_3} \cdot c_3^2)] \cdot e^{3\cdot j\omega_0 \cdot t} \\
& + [A_1 \cdot c_5 + 3 \cdot A_3 \cdot (c_1^2 \cdot c_3 + \overline{c_1} \cdot c_3^2 + \overline{c_5} \cdot c_5^2)] \cdot e^{5\cdot j\cdot \omega_0 \cdot t} \\
& + 3 \cdot A_3 \cdot (c_1^2 \cdot c_5 + c_1 \cdot c_3^2 + \overline{c_3} \cdot c_5^2) \cdot e^{7\cdot j\cdot \omega_0 \cdot t} \\
& + A_3 \cdot (c_3^3 + 3 \cdot \overline{c_1} \cdot c_5^2) \cdot e^{9\cdot j\cdot \omega_0 \cdot t} \\
& + 3 \cdot A_3 \cdot (c_3^2 \cdot c_5 + c_1 \cdot c_5^2) \cdot e^{11\cdot j\cdot \omega_0 \cdot t} \\
& + 3 \cdot A_3 \cdot c_3 \cdot c_5^2 \cdot e^{13\cdot j\cdot \omega_0 \cdot t} + A_3 \cdot c_5^3 \cdot e^{15\cdot \omega_0 \cdot t}
\end{aligned} \tag{B.25}$$

where $\overline{x}$ is the complex conjugate of x. Since the signals in the oscillator are real signals, $c_{-k} = \overline{c_k}$. It appears from this expression that in the real system *all* odd

harmonics will be present due to the up-conversion in the nonlinear network. However, except for the harmonics from −5 to 5, higher harmonics are neglected in this derivation. Since the current input of the feedback network is assumed to be equal to the output of the amplifier, using (B.19), this results in 3 independent complex equations. Due to the fact the signals are real, the complex conjugate equations can be left out:

$$c_1 \cdot \frac{\omega_0 \cdot C}{Q} = [A_1 \cdot c_1 + 3 \cdot A_3 \cdot (\overline{c_1} \cdot c_1^2 + \overline{c_5} \cdot c_3^2)] \tag{B.26}$$

$$c_3 \cdot \frac{\omega_0 \cdot C}{Q} \cdot \sqrt{1 + 9 \cdot Q^2 \cdot \left(\frac{8}{9}\right)^2} \cdot e^{j \cdot \arctan\left(3 \cdot Q \cdot \frac{8}{9}\right)} = [A_1 \cdot c_3 + A_3 \cdot c_1^3 + 3 \cdot A_3 \cdot (c_5 \cdot \overline{c_1}^2 + \overline{c_3} \cdot c_3^2)] \tag{B.27}$$

$$c_5 \cdot \frac{\omega_0 \cdot C}{Q} \cdot \sqrt{1 + 25 \cdot Q^2 \cdot \left(\frac{24}{25}\right)^2} \cdot e^{j \cdot \arctan\left(5 \cdot Q \cdot \frac{24}{25}\right)} = [A_1 \cdot c_5 + 3 \cdot A_3 \cdot (c_3 \cdot c_1^2 + \overline{c_1} \cdot c_3^2 + \overline{c_5} \cdot c_5^2)] \tag{B.28}$$

This set of equations can be solved for a certain feedback network and amplifier in order to obtain the output waveform. The bandwidth limitation of the signal, however, requires a careful approach, certainly for a high gain in the amplifier and/or networks with a low Q factor. A high Q results in a sharper peak in the transfer function; hence, this results in a suppression of the harmonics.

B.2.3 Application to a Known Network

Let us illustrate this now with an example. Suppose an oscillator with a feedback network similar to Fig. 2.9a (a parallel RLC-tank). The resonant angular frequency is normalized and therefore equal to 1 rad/s. The Q-factor is assumed to be equal to 10. The transfer function then looks as follows:

$$H(s) = \frac{s/C}{s^2 + \frac{1}{10} \cdot s + 1} \tag{B.29}$$

At the resonant frequency, this transfer function is a real function with a value of (B.19):

$$H(j \cdot \omega_n) = \frac{Q}{\omega_n \cdot C} = \frac{10}{C} \tag{B.30}$$

which means that the higher the value of the capacitor in the network (for a certain resonant frequency and Q-factor), the lower the impedance at resonance. Note that, using $\omega_n = 1/\sqrt{L \cdot C}$ and $Q = R_P \cdot \sqrt{C/L}$ (2.64), this equation equals R_P. For the sake of keeping the problem simple and understandable, the value of the capacitor is chosen equal to 10, which makes the impedance of the network 1 at the resonant

frequency. This means that the gain of a linear amplifier must also be equal to 1, according to Barkhausen. Therefore, the following characteristic is assumed:

$$G(v) = 1.1 \cdot v - 0.1 \cdot v^3 \tag{B.31}$$

This means, for an input voltage of ±1 V, that the gain indeed decreases to 1. As a result, an output amplitude slightly higher than 1 V is expected. Solving the oscillator Eqs. (B.26–B.28), results in the following solution:

$$c_1 = 2.0301 \times 10^{-1} + j \cdot 5.4048 \times 10^{-1} \tag{B.32}$$

$$c_3 = 4.5033 \times 10^{-6} - j \cdot 7.6881 \times 10^{-6} \tag{B.33}$$

$$c_5 = -1.8225 \times 10^{-8} + j \cdot 3.5200 \times 10^{-9} \tag{B.34}$$

It is clearly visible that the impact of the harmonics in the resulting signal is low compared to the fundamental waveform. This, however, changes when the (small-signal) gain, A_1, becomes higher. The resulting coefficients for different values of the gain are shown in Table B.1. Because of the 'soft' distortion in the amplifier, the influence on the frequency is rather low. The case of an amplifier with strong distortion is discussed in Sect. 4.2.2. The waveform of the output voltage over the tank and the output current of the amplifier are shown in Fig. B.2. In this figure, the impact of the nonlinearity is clearly visible in the applied current. The resonant feedback network, however, hides most of these nonlinearities in the output voltage signal.

Note that this method to calculate the harmonics in the output waveform starts from the assumption that the center frequency is fixed. By doing this, one degree of freedom is taken away in the set of equations. When the frequency is left as a variable, another variable (such as the initial phase shift of the fundamental frequency) has to be chosen freely. Furthermore, due to this assumption, this method only works for circuits with a limited amount of harmonics. Increasing the number of harmonics in the output waveform increases the accuracy but also causes an explosion of terms in the output waveform.

B.3 Proof of Eq. (4.42)

The sum of the infinite series in Sect. 4.2.2 can be written as:

$$\sum_{k\in\{3,5,\ldots\}}^{\infty} \frac{1}{k^2-1} = \sum_{k=1}^{\infty} \frac{1}{(2\cdot k+1)^2-1} \tag{B.35}$$

$$= \frac{1}{4} \cdot \sum_{k=1}^{\infty} \frac{1}{k\cdot(k+1)} \tag{B.36}$$

The sum can be calculated using the following formula:

Table B.1 Coefficients of the different harmonics of the output waveform for the example oscillator

	$Q = 10$	$Q = 1$
$i(v) = 1.1 \cdot v - 0.1 \cdot v^3$		
c_1	$2.030 \times 10^{-1} + j \cdot 5.405 \times 10^{-1}$	$4.638 \times 10^{-1} + j \cdot 3.438 \times 10^{-1}$
c_3	$4.503e-6 - j \cdot 7.688e-6$	$-2.156 \times 10^{-5} - j \cdot 1.816 \times 10^{-5}$
c_5	$-1.823e-8 + j \cdot 3.520e-9$	$1.611 \times 10^{-7} - j \cdot 9.622 \times 10^{-8}$
$\Delta\omega_0/\omega_n$	-3.572×10^{-10}	-3.577×10^{-9}
$i(v) = 1.3 \cdot v - 0.1 \cdot v^3$		
c_1	$5.676 \times 10^{-1} - j \cdot 8.233 \times 10^{-1}$	$4.314 \times 10^{-1} - j \cdot 9.022 \times 10^{-1}$
c_3	$1.265 \times 10^{-5} - j \cdot 4.454 \times 10^{-5}$	$1.816 \times 10^{-5} - j \cdot 1.454 \times 10^{-4}$
c_5	$-2.692 \times 10^{-8} - j \cdot 2.881 \times 10^{-7}$	$-1.231 \times 10^{-6} - j \cdot 2.658 \times 10^{-6}$
$\Delta\omega_0/\omega_n$	-3.215×10^{-9}	-3.223×10^{-8}
$i(v) = 1.5 \cdot v - 0.1 \cdot v^3$		
c_1	$4.601 \times 10^{-1} + j \cdot 1.206 \times 10^{0}$	$-6.181 \times 10^{-1} + j \cdot 1.133 \times 10^{0}$
c_3	$4.901 \times 10^{-5} - j \cdot 8.673 \times 10^{-5}$	$-8.824 \times 10^{-5} + j \cdot 3.026 \times 10^{-4}$
c_5	$-1.012 \times 10^{-6} + j \cdot 2.314 \times 10^{-7}$	$1.896 \times 10^{-6} + j \cdot 1.035 \times 10^{-5}$
$\Delta\omega_0/\omega_n$	-8.934×10^{-9}	-8.971×10^{-8}
$i(v) = 2.0 \cdot v - 0.1 \cdot v^3$		
c_1	$-6.213 \times 10^{-1} + j \cdot 1.717 \times 10^{0}$	$7.372 \times 10^{-1} - j \cdot 1.670 \times 10^{0}$
c_3	$1.332 \times 10^{-4} + j \cdot 2.483 \times 10^{-4}$	$2.870 \times 10^{-5} - j \cdot 8.913 \times 10^{-4}$
c_5	$5.772 \times 10^{-6} + j \cdot 1.059 \times 10^{-6}$	$-3.532 \times 10^{-5} - j \cdot 4.815 \times 10^{-5}$
$\Delta\omega_0/\omega_n$	-3.577×10^{-8}	-3.622×10^{-7}

Also the influence of the harmonics on the center frequency is shown in the table

Theorem B.1

$$\sum_{k=1}^{l} \frac{1}{k \cdot (k+1)} = \frac{l}{l+1} \tag{B.37}$$

Proof This proof uses induction: first it is shown that the explicit formula holds for $l = 1$; afterwards it is shown that, if the formula holds for l, it will also hold for $l+1$.

- $l = 1$
  It can easily be seen that:

$$\sum_{k=1}^{l=1} \frac{1}{k \cdot (k+1)} = 1/2 = \frac{l}{l+1} \tag{B.38}$$

- $l + 1$
  When the formula holds for l, the sum of the series from 1 to $l+1$ can be written as:

$$\sum_{k=1}^{l+1} \frac{1}{k \cdot (k+1)} = \sum_{k=1}^{l} \frac{1}{k \cdot (k+1)} + \frac{1}{(l+1) \cdot (l+2)} \tag{B.39}$$

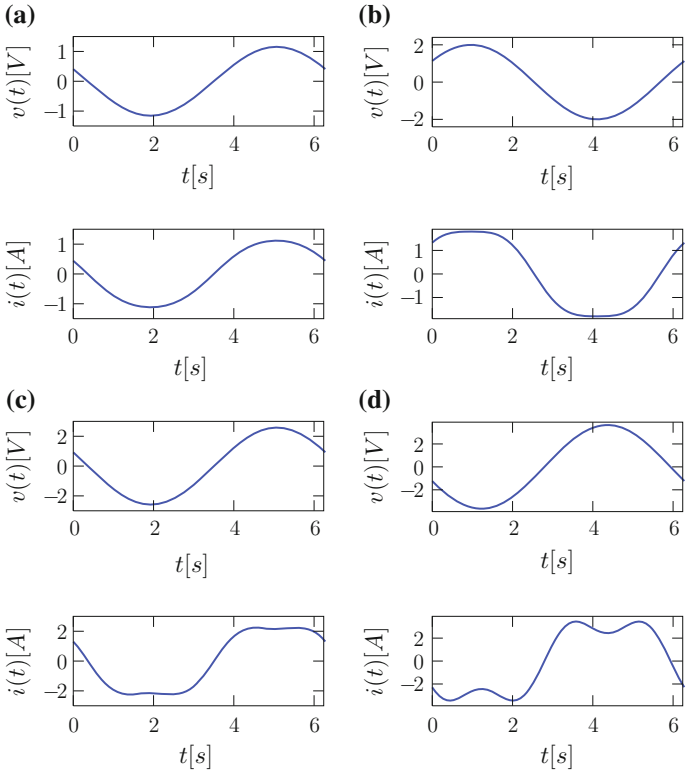

Fig. B.2 Output voltage waveform and injected current for different transconductance amplifiers with soft distortion. The nonlinearity is necessary to control the amplitude but causes harmonics in the output waveform. The harmonics, on their turn, cause a small frequency drop. **a** $Q = 10$, $i(v) = 1.5 \cdot v - 0.1 \cdot v^3$. **b** $Q = 10$, $i(v) = 2.0 \cdot v - 0.1 \cdot v^3$

$$= \frac{l}{l+1} + \frac{1}{(l+1)\cdot(l+2)} \tag{B.40}$$

$$= \frac{l^2 + 2\cdot l + 1}{(l+1)\cdot(l+2)} \tag{B.41}$$

$$= \frac{l+1}{l+2} \tag{B.42}$$

which proves Theorem B.1. ■

It can easily be seen that:

$$\lim_{l\to+\infty} \sum_{k=1}^{l} \frac{1}{k\cdot(k+1)} = \lim_{l\to+\infty} \frac{l}{l+1} = 1 \tag{B.43}$$

which is used to obtain the result of (4.42).

Appendix C
Measurement Issues for Jitter and Phase Noise

Measuring jitter and phase noise in an oscillator output signal is a difficult task. It is mainly the colored noise which complicates the measurements because of the ultra-slow frequency variations, which causes frequency drift. A possible consequence of this, when measuring the cycle-to-cycle jitter, is that the subsequent measurements do not converge! Due to the frequency drift, the measured period 'drifts away' from the average period depending on the moment at which the measurement is performed. In [92, 180] different methods are discussed to overcome these problems.

C.1 White Noise Jitter Divergence

Different measures are available to express the instabilities in an oscillator output signal. Most of them are based on the *variance* of variations in the frequency, phase or phase-time. The phase deviation $\phi(t)$ of an oscillator modulated with white noise is given by a *random walk* about the ideal phase $\omega_0 \cdot t$ (the resulting PSD is proportional to $1/f^2$). When considering the variance σ_ϕ of the phase fluctuations, this causes a continuous increase with the observation time (this is similar to the absolute jitter, Definition 3.1; the uncertainty of the next clock edge will increase over time). This can be understood by the knowledge that the VCO is an ideal integrator, of which the output (the phase) can grow forever. It is this very same integration that shapes the PSD of the phase fluctuations $S_\phi(f)$, which makes the PSD go to infinity. This integration operation is the same as the so-called superposition integral in Hajimiri's theory, Eq. (3.20).

To bound this error, the VCO can be put in a phase-locked loop (PLL), which limits the phase deviation compared to a reference clock. In the time domain, this can be interpreted as a periodical *reset* of the phase deviation. In the frequency domain, this means that the low-frequency content of the output phase deviation is filtered. The transfer function of a PLL acts as a high-pass filter on the oscillator output. In this configuration, the jitter can easily be measured, because it does not drift away from the ideal (reference) phase. Furthermore this technique allows to measure

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the frequency deviation of the oscillator by means of the VCO input signal, which is proportional to the frequency deviation between the oscillator and the reference input. The carrier frequency is not present in this control signal, which allows to exploit the full dynamic range of the measurement setup (if a strong carrier signal is present, the phase noise or frequency is dominated by the carrier signal). The main drawback of this *closed-loop, clock-referenced* technique is the fact the output is filtered by the PLL transfer function, which needs to be corrected afterwards [92, 180, 181].

Another method to avoid the divergence of frequency stability measures in the time domain is limiting the time interval over which they are measured. So-called *open-loop, self-referenced* techniques [180] start a measurement at a certain clock edge and measure the jitter of the following clock edges compared to the first clock edge. When starting a new measurement, ($t = 0$) the phase error is reset. In this way, the phase error can only drift away during the measurement interval. When the jitter of the subsequent clock cycles is uncorrelated, the following standard deviation as a function of the measurement interval t can be expected (3.59):

$$\sigma_{abs,OL}(t) = \sqrt{c} \cdot \sqrt{t} \tag{C.1}$$

which is equivalent to Eq. (3.59) and valid when only white noise is injected in the oscillator ($1/f^2$ in the oscillator spectrum). This means that the cycle-to-cycle jitter is an open-loop, self-referenced jitter measurement for which the measurement time is equal to the oscillator period, $t = 1/f_{osc}$. c is an important Figure of Merit of an oscillator, which is related to the shape of the Lorentzian noise spectrum (3.50). Although the cycle-to-cycle jitter is a straightforward measurement to quantify the phase noise, a high time resolution or a specialized measurement setup is needed to do these measurements [92]. An interesting question is how both measurements, *closed-loop* and *open-loop*, can be related.

The measured jitter of a closed-loop measurement strongly depends on the bandwidth of the PLL. In [180] it is illustrated that, for a PLL of which the transfer function can be approximated by the low-pass characteristic:

$$H(s) = \frac{2 \cdot \pi \cdot f_L}{s + 2 \cdot \pi \cdot f_L} \tag{C.2}$$

where f_L is the loop bandwidth of the PLL, the measured jitter stabilizes when the measurement time is high compared to $1/(2 \cdot \pi \cdot f_L)$. This can be understood as follows: when performing a self-referenced measurement starting at $t = 0$, the jitter increases with the square root of the measurement interval. At the moment the measurement time approaches

$$t_L = \frac{1}{2 \cdot \pi \cdot f_L}, \tag{C.3}$$

the PLL is able to compensate for higher phase deviations and the jitter becomes constant as a function of time. When the absolute jitter of a clock edge, compared

to the reference clock, is called σ_x, than the jitter between two clock edges, which are separated a period $\Delta t \gg t_L$ from each other, is equal to $\sqrt{2} \cdot \sigma_x$, assuming that this jitter is uncorrelated. In [180, 282] this characteristic, which is a function of the PLL bandwidth f_L, is analyzed. It is shown that:

$$\sigma_x = \sqrt{c} \cdot \sqrt{\frac{1}{4 \cdot \pi \cdot f_L}} \tag{C.4}$$

Indeed: the resulting jitter is a factor $\sqrt{2}$ different from the jitter at the -3 dB $(=1/\sqrt{2})$ bandwidth f_L of the PLL. These conclusions are important when performing the *closed-loop, clock-referenced* measurement discussed earlier to compensate for the PLL behavior. The jitter can be reduced in two ways: by improving the oscillator jitter (c) and by increasing the PLL bandwidth (f_L). This clearly shows the relationship between a closed-loop and an open-loop measurement.

C.1.1 Frequency Fluctuations as a Noise Measure

The instantaneous relative frequency fluctuations are represented by (2.41):

$$y(t) = \frac{\frac{d\phi(t)}{dt}}{\omega_0} \tag{C.5}$$

As a matter of fact, the frequency cannot be measured instantaneously (opposite to phase measurements, in the absence of amplitude noise), which makes it necessary to measure the frequency drift over a certain time span τ:

$$\langle y \rangle_{t_0,\tau} = \frac{1}{\tau} \cdot \int_{t_0-\tau/2}^{t_0+\tau/2} y(t)dt. \tag{C.6}$$

Using (2.41), this equation can be written as:

$$\langle y \rangle_{t_0,\tau} = \frac{\phi(t_0+\tau/2) - \phi(t_0-\tau/2)}{\omega_0 \cdot \tau} = \frac{1}{\tau} \cdot [x(t_0+\tau/2) - x(t_0-\tau/2)] \tag{C.7}$$

This means that the averaged instantaneous frequency fluctuations over a certain time interval can be calculated as the normalized phase-time $x(t)$ error over the very same time interval. Since $y(t)$, $\phi(t)$ and therefore also $x(t)$ are random processes, this averaged error is a random variable with a mean value and a standard deviation. The mean value is equal to zero, which makes the variance equal to the mean-square value:

$$\sigma^2_{\langle y \rangle,\tau} = E[\langle y \rangle^2_{t_0,\tau}] \tag{C.8}$$

where $E[\cdot]$ stands for the expected value calculated over an infinite set of samples. It can therefore be stated that $\sigma^2_{\langle y\rangle,\tau}$ is the true variance of $\langle y\rangle_{t_0,\tau}$. In a practical situation, however, it is not possible to create an infinite set of samples, which makes the variance itself a random variable over the different (limited) sample sets. It is considered to be an estimator for the true variance (based on a limited set). A good, unbiased, estimator is an estimator of which the average value converges to the true variance. An unbiased estimator for the variance is given by:

$$s^2_{\langle y\rangle,\tau} = \frac{1}{N-1} \cdot \sum_{i=1}^{N} \left(\langle y\rangle_{t_i,\tau} - \frac{1}{N} \cdot \sum_{j=1}^{N} \langle y\rangle_{t_j,\tau} \right)^2 \tag{C.9}$$

where N is the number of samples of $\langle y\rangle$ in the subset and $N \geq 2$ [217]. This estimator holds as long as the samples are uncorrelated. Note also the difference in notation between the true variance of an infinite set σ^2_x and the estimated variance of a subset s^2_x. The relationship between this variance and the cycle-to-cycle jitter is:

$$\sigma_{\langle y\rangle,T_0} = \frac{\sigma_c}{T_0} \tag{C.10}$$

C.1.2 Relation Between the Variance and the PSD

The link between the PSD and the variance of the fractional frequency fluctuations is obtained by considering the fact that the time interval τ over which the frequency fluctuations are averaged, can be treated as a filter in the time domain. In this way, the samples of $\langle y\rangle_{t_0,\tau}$ are considered to be a moving average operation:

$$\langle y\rangle_{t_0,\tau} = \frac{1}{\tau} \cdot \int_{t_0-\tau/2}^{t_0+\tau/2} y(t)dt \tag{C.11}$$

$$= \frac{1}{\tau} \cdot \int_{-\infty}^{\infty} y(t) \cdot \Pi\left(\frac{t}{\tau}\right) dt \tag{C.12}$$

$$= \frac{1}{\tau} \cdot \int_{-\infty}^{\infty} y(t) \cdot \Pi\left(\frac{t_0 - t}{\tau}\right) dt \tag{C.13}$$

which is a convolution integral. The variance is then obtained by integrating over the PSD of the resulting waveform:

$$\sigma^2_{\langle y \rangle,\tau} = \int_{-\infty}^{\infty} S_y(f) \cdot \left(\frac{\sin(\pi \cdot f \cdot \tau)}{\pi \cdot f \cdot \tau} \right)^2 df \tag{C.14}$$

$$= \int_{-\infty}^{\infty} \frac{f^2}{f_0^2} \cdot S_\phi(f) \cdot \left(\frac{\sin(\pi \cdot f \cdot \tau)}{\pi \cdot f \cdot \tau} \right)^2 df \tag{C.15}$$

where the factor $\left(\frac{\sin(\pi \cdot f \cdot \tau)}{\pi \cdot f \cdot \tau} \right)^2$ is called the *transfer function of the time-domain measure of frequency stability* [92, 217]. Using (C.10) it can be seen that this equation is equivalent to (3.67). In case of a $1/f^2$ phase noise profile, this integral will converge.

The previous discussion assumes white, uncorrelated noise. In Sect. 3.6 it has been shown that in the case of correlated or colored noise sources, the linear increase over time for an open-loop measurement does not hold. Only measuring the jitter over a certain time interval to obtain the cycle-to-cycle jitter, is therefore not sufficient to do a jitter characterization. In the frequency domain, this is comparable to characterizing the noise based on only one frequency value of the PSD. The influence of the frequency noise shaping ($1/f^\alpha$) is closely related to the evolution of the absolute jitter over time (3.65).

C.2 Colored Noise Jitter

When colored noise is injected in an oscillator, this results in an $1/f^\alpha$ region in the phase spectrum. α is in this case greater or equal to 3. In this case, the absolute jitter does no longer increase proportionally to the square root of the observation time, but also a term proportional to the observation time appears, (3.65). As explained in Sect. 3.6.3, the noise injected during subsequent time intervals is therefore correlated, which causes the phase to drift faster away than in the case of uncorrelated noise sources. As stated in [104], it can be assumed in this case that the standard deviation adds instead of the variance.

C.2.1 Frequency Fluctuations as a Colored Noise Measure

As previously shown, the fractional frequency fluctuations are an interesting measure to measure the frequency stability in the time domain. Moreover, due to its relation to the cycle-to-cycle jitter, it gives an intuitive insight in the behavior and the effects of the jitter on for instance the performance of a clocked circuit. Problems arise, however, when the integral (C.15) is calculated for a colored noise spectrum. Keeping in mind that the transfer function of the time-domain measure of frequency stability is equal to 1 around $f = 0$, it is clear that this integral will diverge, see (2.47) with

$\alpha \leq -1$. Typically, this is solved by limiting the minimum frequency to which this integral is calculated around the carrier. Often this is explained as a limit which comes forth from the limited observation time. This, however, is not satisfactory since the calculated variance strongly depends on this value and therefore does not converge when a larger observation time is used [41].

A solution can be to use the PLL measurement method described above: the frequencies within the bandwidth of the PLL, f_L, are suppressed as a result of the PLL feedback mechanism. In this way, as a result of the continuous tuning of the oscillator to the nominal frequency of the frequency reference, the variance of the frequency fluctuations (and the jitter) converges for an increasing number of samples $\langle y \rangle_{t_0,\tau}$ when the total observation time is larger than the inverse of the loop bandwidth [92].

C.2.2 The Allan Variance

A different way to overcome these convergence problems, is the use of an alternative measure instead of the variance. Instead of using the complete set of average frequency fluctuations $\langle y \rangle_{t_0,\tau}$, one can combine the subsequent averages instead. The Allan variance, which is also an IEEE-recommended measure for frequency stability, is defined as [5]:

$$\sigma^2_{A,\langle y \rangle,\tau} = E\left[\sum_{i=1}^{2}\left(\langle y \rangle_{t_i,\tau} - \frac{1}{2}\cdot\sum_{j=1}^{2}\langle y \rangle_{t_j,\tau}\right)^2\right] \tag{C.16}$$

$$= \frac{1}{2}\cdot E[(\langle y \rangle_{t_2,\tau} - \langle y \rangle_{t_1,\tau})^2] \tag{C.17}$$

where $\langle y \rangle_{t_i,\tau}$ is defined as:

$$\langle y \rangle_{t_i,\tau} = \frac{1}{\tau}\cdot\int_{t_i-\tau/2}^{t_i+\tau/2} y(t)dt \tag{C.18}$$

and $t_{i+1} - t_i = \tau$, which means that there is no *dead time* between the subsequent samples. Similar to (C.7), also this equation can be expressed in terms of the phase-time $x(t_k)$ (2.40):

$$\sigma^2_{A,\langle y \rangle,\tau} = \frac{1}{2\cdot\tau^2}\cdot E\left[[x(t_{k+2}) - 2\cdot x(t_{k+1}) + x(t_k)]^2\right] \tag{C.19}$$

which shows the tight connection between the Allan variance and the alternative definition of the cycle-to-cycle jitter, (3.62). Although the difference between the Allan variance and the classic variance is subtle, it has a huge impact on the correlated noise. The correlation between the subsequent samples is, due to the definition of the

Allan variance, canceled. The linear trend in the jitter is compensated by combining several samples. To demonstrate the convergence in case of a colored $(1/f)$ noise source, the transfer function of this frequency measure has to be determined. The Allan variance is the variance of the random variable:

$$\frac{1}{\sqrt{2}} \cdot (\langle y \rangle_{t_{k+1},\tau} - \langle y \rangle_{t_k,\tau}) = \frac{1}{\sqrt{2} \cdot \tau} \cdot \int_{-\infty}^{\infty} y(t) \cdot h_A \left(\frac{t_{k+1} - t}{\tau} \right) dt \tag{C.20}$$

where $h_A(t_{k+1} - t)$ is equal to the *derivative triangular function* (see definition A.14):

$$h_A(t) = \Xi(t/\tau) \triangleq \begin{cases} \frac{1}{\tau}, & \tau \leq t \leq 0 \\ \frac{-1}{\tau}, & 0 < t \leq \tau \\ 0, & |t| > \tau \end{cases} \tag{C.21}$$

The resulting PSD, after performing the filtering operation, can then be integrated to obtain the resulting Allan variance of the oscillator signal:

$$\sigma^2_{A,\langle y \rangle,\tau} = \int_{-\infty}^{\infty} S_y(f) \cdot 2 \cdot \left(\frac{\sin(\pi \cdot f \cdot \tau)^2}{\pi \cdot f \cdot \tau} \right)^2 df \tag{C.22}$$

$$= \int_{-\infty}^{\infty} \frac{f^2}{f_0^2} \cdot S_\phi(f) \cdot 2 \cdot \left(\frac{\sin(\pi \cdot f \cdot \tau)^2}{\pi \cdot f \cdot \tau} \right)^2 df \tag{C.23}$$

Because of the low-frequency filtering operation of the Allan variance, the integral is convergent also when $1/f$ noise is injected in the oscillator. However, an upper limit for the noise integration is still needed for white and flicker noise. Typically this bound is taken at the cutoff frequency f_h which is existing in each system. In a nonlinear oscillator, it is reasonable to integrate until 1.5 times the oscillation frequency; every higher frequency is also represented in this bandwidth. In Table C.1 an overview is given of the resulting Allan variance for different slopes of the frequency (phase) spectrum, as a function of the observation time τ. It is clearly seen that only for *flicker frequency fluctuations* the Allan variance is independent of the observation time.

An interesting conclusion after using the Allan variance is the observation that by combining measurements of subsequent periods, the low-frequency content can be filtered away. However, from Table C.1 it appears that the Allan variance is only able to compensate for the first-order colored noise contributions. In the following section, a methodology is demonstrated to also compensate for the higher-order contributions in order to quantify them in the time domain.

Table C.1 The Allan variance for different slopes of the (single-sided) PSD

$S_y(f)$	$S_\phi(f)$	$\sigma^2_{A,\langle y\rangle,\tau}$	Description
$h_{-2}\cdot f^{-2}$	$f_0^2\cdot h_{-2}\cdot f^{-4}$	$\frac{2\cdot\pi^2\cdot h_{-2}\cdot\tau}{3}$	Random walk frequency fluctuations
$h_{-1}\cdot f^{-1}$	$f_0^2\cdot h_{-1}\cdot f^{-3}$	$2\cdot\ln(2)\cdot h_{-1}$	Flicker frequency fluctuations
$h_0\cdot f^0$	$f_0^2\cdot h_0\cdot f^{-2}$	$\frac{h_0}{2\cdot\tau}$	White frequency fluctuations
$h_1\cdot f^1$	$f_0^2\cdot h_1\cdot f^{-1}$	$\frac{h_1}{4\cdot\pi^2\cdot\tau^2}\cdot[1.038+3\cdot\ln(2\cdot\pi\cdot f_h\cdot\tau)]$	Flicker phase fluctuations
$h_2\cdot f^2$	$f_0^2\cdot h_2\cdot f^0$	$\frac{3\cdot h_2\cdot f_h}{4\cdot\pi^2\cdot\tau^2}$	White phase fluctuations

It is clearly seen that only for $1/f$ noise injected in the oscillator, a constant value is obtained [5, 217]

C.2.3 The Use of Structure Functions

The use of structure functions in the area of oscillator phase noise analysis was first introduced by Lindsey and Chie [164]. It will be shown below that this theory succeeds in capturing the previously discussed time-domain noise measures (variances) in a unifying methodology. Structure functions are a mathematical tool which can be used to avoid the singularities which appear at low frequencies in the case of colored noise sources. The underlying idea is that the structure functions are able to de-trend the measurement data, similar to what the Allan variance does for first-order colored noise sources.

C.2.3.1 Increments of a Function

The increment of a random process $x(t)$ is defined as follows:

Definition C.1 Let $\Delta^N x(t,\tau)$ denote the N-th increment of $x(t)$ with time step τ. The first-order increment of a random process $x(t)$ is defined as:

$$\Delta^1 x(t,\tau) = x(t+\tau) - x(t) \tag{C.24}$$

The N-th-order increment of a function can recursively be defined as:

$$\Delta^N x(t,\tau) = \Delta^{N-1}[\Delta^1 x(t,\tau)] = \Delta^1[\Delta^{N-1}x(t,\tau)] \tag{C.25}$$

or can be written explicitly as:

$$\Delta^N x(t,\tau) = \sum_{k=0}^{N}(-1)^k\cdot\binom{N}{k}\cdot x[t+(N-k)\cdot\tau] \tag{C.26}$$

where $\binom{N}{k}$ denotes *the combinations of k samples out of N*.

Note that this definition results in the same formulas as used to approximate the N-th-order derivative of $x(t)$ using only forward differences. This observation helps to understand the working principle of this method. When calculating the N-th-order increment, $N+1$, τ-spaced samples of the function are needed. Moreover, when M, τ-spaced samples are available, $M-N$ N-th-order increments can be calculated, which results in a high data utilization for large numbers of samples. Because the adjacent samples are combined, the increments are able to detect or cancel trends or correlations between the different data points. Generally speaking, the *variance* of the result of a certain increment is larger for uncorrelated samples than for correlated data samples. This is the same working principle of the Allan variance for adjacent oscillation periods! Note that the N-th increment of a polynomial of an order smaller than N, is equal to zero. This corresponds to the fact that these increments are an estimator of the N-th derivative.

C.2.3.2 Structure Functions

Based on these increments, structure functions can be defined:

Definition C.2 The N-th-order structure function $D_x^N(t_s, \tau)$ is defined as the autocorrelation function of the N-th increment:

$$D_x^N(t_s, \tau) \triangleq \left\langle (\Delta^N x(t, \tau)) \cdot (\Delta^N x(t + t_s, \tau)) \right\rangle \tag{C.27}$$

$$= \lim_{T \to \infty} \int_{-T/2}^{T/2} (\Delta^N x(t, \tau)) \cdot (\Delta^N x(t + t_s, \tau) dt \tag{C.28}$$

When the time shift t_s is equal to zero, this can shortly be written as:

$$D_x^N(\tau) = \left\langle (\Delta^N x(t, \tau))^2 \right\rangle \tag{C.29}$$

In this work, the term *structure function* refers to the structure function with $t_s = 0$, which is in fact the variance of the N-th-order increment of $x(t)$. In [164] it is shown that these functions can easily be related to the output PSD of the oscillator [92].

$$D_x^N(\tau) = 2^{2 \cdot N} \cdot \int_{-\infty}^{\infty} S_x(f) \cdot \sin^{2 \cdot N}(\pi \cdot f \cdot \tau) df \tag{C.30}$$

$$D_x^N(\tau) = 2^{2 \cdot N - 2} \cdot \int_{-\infty}^{\infty} S_y(f) \cdot \frac{\sin^{2 \cdot N}(\pi \cdot f \cdot \tau)}{(\pi \cdot f)^2} df \tag{C.31}$$

$$\frac{D_x^N(\tau)}{\tau^2} = 2^{2 \cdot N - 2} \cdot \int_{-\infty}^{\infty} S_y(f) \cdot \frac{\sin^{2 \cdot N}(\pi \cdot f \cdot \tau)}{(\pi \cdot f \cdot \tau)^2} df \tag{C.32}$$

where the last equation is just the structure function normalized to the observation interval τ. These equations can be obtained by using the *gated integration* approach as previously demonstrated for the variance and the Allan variance. If f is close to zero, the transfer function of the timing measure can be approximated by:

$$|H_{D,N}(f)| = \left| \frac{\sin^N(\pi \cdot f \cdot \tau)}{(\pi \cdot f \cdot \tau)} \right| \approx (\pi \cdot f \cdot \tau)^{N-1} \tag{C.33}$$

This means that the singularities in the spectrum can be compensated by using the correct structure function. Since:

$$S_y(f) \cdot \frac{\sin^{2\cdot N}(\pi \cdot f \cdot \tau)}{(\pi \cdot f \cdot \tau)^2} \sim f^{\alpha} \cdot f^{2N-2} \tag{C.34}$$

the integration of the spectrum is convergent as long as $\alpha > -(2 \cdot N - 1)$ or $N > \frac{1-\alpha}{2}$. This indicates that it is always possible to take a high enough order of increment N to obtain a bounded structure function. The effect of taking a higher-order structure function is demonstrated in Table C.2. Interesting to note is the fact that the structure functions have a close relationship with the previously defined time-domain jitter measures:

$$\sigma^2_{\langle y \rangle, \tau} = \frac{1}{\tau^2} \cdot D^1_x(\tau) \tag{C.35}$$

$$\sigma^2_{A, \langle y \rangle, \tau} = \frac{1}{2 \cdot \tau^2} \cdot D^2_x(\tau) \tag{C.36}$$

C.2.3.3 Structure Functions to Measure Polynomial Drift

Colored or correlated noise sources result in a polynomial drift in for instance the phase-time error. It is interesting to compare the results of the random noise process

Table C.2 Values of the different structure functions, corresponding to the different areas in the power-law noise spectrum

$S_\phi(f)$	$D^1_x(\tau)$	$D^2_x(\tau)$	$D^3_x(\tau)$
$f_0^2 \cdot h_{-2} \cdot f^{-4}$	Non-convergent	$\frac{4}{3} \cdot \pi^2 \cdot h_{-2} \cdot \tau^3$	$2 \cdot \pi^2 \cdot h_{-2} \cdot \tau^3$
$f_0^2 \cdot h_{-1} \cdot f^{-3}$	Non-convergent	$4 \cdot \ln(2) \cdot h_{-1} \cdot \tau^2$	$6.75 \cdot h_{-1} \cdot \tau^2$
$f_0^2 \cdot h_0 \cdot f^{-2}$	$\frac{1}{2} \cdot h_0 \cdot \tau$	$h_0 \cdot \tau$	$3 \cdot h_0 \cdot \tau$
$f_0^2 \cdot h_1 \cdot f^{-1}$	$\frac{1}{2 \cdot \pi^2} \cdot h_1 \cdot [\ln(\pi \cdot \tau \cdot f_h) + 1.27]$	$\frac{3}{2 \cdot \pi^2} \cdot h_1 \cdot [\ln(\pi \cdot \tau \cdot f_h) + 1.04]$	$\frac{6}{\pi^2} \cdot h_1 \cdot [\ln(\pi \cdot \tau \cdot f_h) + 0.96]$
$f_0^2 \cdot h_2 \cdot f^0$	$\frac{1}{2 \cdot \pi^2} \cdot h_2 \cdot f_h$	$\frac{3}{2 \cdot \pi^2} \cdot h_2 \cdot f_h$	$\frac{5}{\pi^2} \cdot h_2 \cdot f_h$

A single-sided (positive) PSD is assumed, which requires integration form 0 to infinity. It can clearly be seen that, although it has an impact on the convergence, the dependence on τ does not change as a function of the order of the structure function [92, 164]

as it was previously analyzed to the outcome of structure functions of a deterministic function. Assume the following deterministic phase time error:

$$x(t) = \sum_{k=0}^{M} \frac{A_k}{k!} \cdot t^k \tag{C.37}$$

where M denotes the maximum polynomial drift order. Since the N-th increment of this function corresponds to the N-th derivative (or at least its numerical approximation), the outcome of the increment is equal to zero. This means that the drift on the time-domain measurement of the phase error can completely be suppressed by choosing a high order of the structure function. If $N = M$ the outcome will be independent of t and be equal to:

$$\Delta^M x(t) = \tau^N \cdot A_N = \sqrt{D_x^M(\tau)} \tag{C.38}$$

which only depends on the observation time τ. The τ-dependency of this deterministic increment looks very similar to the previously obtained values of the stochastic process in Table C.2. Can a distinction be made between these types of processes? Table C.3 compares the τ-dependency of the structure functions for different orders of polynomial drift. This shows that the dependency to τ of the structure functions is always different for deterministic and stochastic processes. This allows to determine unambiguously the highest polynomial phase drift order. By subtracting the resulting orders, it is possible to determine the lower-order terms and even the complete polynomial. In this way, noise measurements can completely be detrended and analyzed in detail.

In [164] an algorithm to determine the highest-order of frequency drift and for the presence of (higher order) Flicker-noise:

- [Initialize] Set order $i = 1$

Table C.3 τ-dependency of structure functions of deterministic and stochastic processes

Deterministic		Stochastic	
M	$\frac{\sqrt{D_x^M(\tau)}}{\tau}$	α_m	$\frac{\sqrt{D_x^M(\tau)}}{\tau}$
2	$A_2 \cdot \tau$	-2	$\sim\tau^{1/2}$
3	$A_3 \cdot \tau^2$	-4	$\sim\tau^{3/2}$
4	$A_4 \cdot \tau^3$	-6	$\sim\tau^{5/2}$

In the left column, the maximum order of the polynomial is given. The second column shows the outcome of the structure function of order $N = M$. The third column shows the lowest α, α_m for which the stochastic process $S_y(f) = h_\alpha \cdot f^\alpha$ has a bounded structure function of order M. The last column shows the outcome of the normalized structure function for the particular α_m power-law in $S_y(f)$ [92, 164]

- [Test for stationarity] Calculate $\hat{D}_{\phi}^{(i)}(\tau)$ and check whether it is stationary (time-independent), using several samples. If not, increase i by 1 and try again. If yes, set order of frequency drift to $i-1$ and go further.
- [Test for boundedness] If $\hat{D}_{\phi}^{(i)}(\tau)$ is not bounded; increase i by 1 and try again. If yes, set $M=i$ and go further.
- [End] Calculate $S_{\phi}(\omega)$ from $\hat{D}_{\phi}^{(i)}(l\tau)$, $l=1, ..., l_{max}$.

The last step, however, appears to be a difficult task; in [164] two approaches are demonstrated. One can also use $\hat{D}_{\phi}^{(i)}(l\tau)$, $l=1, ..., l_{max}$ to do a curve-fitting using the terms in Table C.2.

Appendix D
Comparison to the State of the Art

This appendix contains four tables containing a comparison of oscillator implementations from literature. The reported specifications of all references are spread over 4 tables, Tables D.1, D.2, D.3 and D.4. The specifications of the implementations which have been discussed in Part II of this work are found at the bottom of every table. Values and references printed in italic, are based on simulations only.

Some of the phase noise FoM values are calculated using (3.63) when only the jitter is reported. Note that this results in an overestimate of the noise spectrum, since this also includes jitter coming from the output circuitry (which is not accumulated in the oscillator).

Table D.1 Comparison to the state of the art

References	Tech. (µm)	f_{tank} (f_{out}) (MHz)	Topology	Voltage (V)	Power (mW)
[178], JSSC	0.35	1,536 (96)	LC harm.	5 (3.3)	31.35
	0.35	1,536 (12)	LC harm.	5 (3.3)	31.35
[177], ISCAS	0.25	900 (25)	LC harm.	3.3	59.4
	0.25	900 (25)	LC harm.	3.3	59.4
[175], FCS	0.13	3,000 (6–133)	LC harm.	3.3	6.6
[281], ISSCC	0.35	9,800	LC harm.	2.2	11.88
	0.35	9,800	LC harm.	2.2	11.88
[252], MWCL	0.18	4,610	LC harm.	1.5	3
	0.18	5,000	LC harm.	1.5	3
[117], MWCL	0.18	5,600	LC harm.	1.2	2.4
[165], EL	0.18	5,470	LC harm.	1.2	5.04
	0.18	5,470	LC harm.	1.2	5.04
[166], EL	0.18	5,500	LC harm.	1.2	3
[77], WAS	0.25	1,800	LC harm.	1.1	0.17
	0.25	1,800	LC harm.	1.1	0.17

(continued)

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Table D.1 (continued)

References	Tech. (µm)	f_{tank} (f_{out})(MHz)	Topology	Voltage (V)	Power (mW)
[150], MWCL	0.18	2,300	LC harm.	1.5	0.97
	0.18	2,300	LC harm.	1.5	0.97
[148], MWCL	0.18	2,630	LC harm.	0.45	0.43
	0.18	2,645	LC harm.	0.45	0.43
[119], ICECS	0.25	2,400	LC harm.	1.5	0.08
	0.25	2,400	LC harm.	1.5	0.08
[155], JSSC	0.13	5,121	LC Ring	0.5	4.01
	0.13	5,341	LC harm.	0.5	1.01
[234], FCS	0.18	1,700 (1–133)	LC harm.	3.3	23.1 (25 MHz)
[3], FCS	0.18	−(1–133)	LC harm.	3.3	23.43 (25 MHz)
[238], ISSSE	Bip.	0.01–10	LR	–	–
[250, 251], JSSC	0.18	14	RC rel.	1.8	45 µ
	0.18	14	RC rel.	1.8	45 µ
[29], ISSCC	0.13	3.2	IV-C rel.	1.5	38.4 µ
[94], JSSC	0.8	1.5	IV-C ring	5	1.8
[90], ISSCC	65 n	12	IV-C rel.	1.2	90 µ
[192], SBCCI	0.5	12.8	IV-C rel.	3	0.4
[275], SBCCI	0.5	11.6/21.4	IV-C rel.	3	0.4
[195], ISCAS	0.13	2	IV-C rel.	1.8	3 µ
[162], ESSCIRC	0.18	31.25 k	IV-C rel.	1.8	360 n
[254], ICECS	0.18	6.66 k	IV-C rel.	1.5	940 n
	0.18	6.66 k	IV-C rel.	1.5	940 n
[197], ISSCC	65 n	9–30 k	IV-C rel.	1	120 n
	65 n	9–30 k	IV-C rel.	1	120 n
[244], JSSC	0.25	7	Ring	2.4	1.5
[149], VLSI	0.18	10	Ring	1.2	80 µ
[257], ESSCIRC	0.35	2–100	Ring	1.8	0.18 (30 MHz)
	0.35	2–100	Ring	1.8	0.18 (30 MHz)
[225], JSSC	65 n	0.1	MV-C rel.	1.2	41 µ
[227], JSSC	65 n	0.15 (20 Hz)	MV-C rel.	1.2	51 µ
	65 n	0.15 (20 Hz)	MV-C rel.	1.2	51 µ
[71], TCAS-I	0.35	3.3 k	MV-C rel.	1	11 n
[126], JSSC	0.7	1.6	ETF-FLL	5	7.8
T-Wien bridge	65 n	6	RC harm.	1.2	66 µ
	65 n	6	RC harm.	1.2	66 µ
V-Wien bridge	0.13	24	RC harm.	0.9	33 µ
Pulsed oscillator	0.13	48–1,540	Pulsed LC	1.1	46 µ
Inj.-locked 1	0.13	950–1,150	RC harm.	1.0	127 µ
Inj.-locked 2	40 n	23–36	RC harm.	1.0	72 µ

Table D.2 Comparison to the state of the art: noise

References	Jit. (ps)	PN (Δf) (dB) (MHz)	FoM_{PN} (dB)	Tuning (Range) (%/V) (V)	$FoM_{PN,tuned}$ (dB)
[178]	6.78	–	128.6[a]	–	–
	8.96	–	135.2[a]	–	–
[177]	3.927	−114(0.1)	136.4[a]	–	–
	3.927	−143(1)	153.2	–	–
[175]	2	−73.97 (12 k)	152.0[a]	–	–
[281]	–	−93 (0.1)	182.1	1.37 (2)	183.5
	–	−118 (1)	187.1	1.37 (2)	188.5
[252]	–	−120.99 (1)	189.5	3.38 (2.4)	194.8
	–	−120.42 (1)	189.6	3.38 (2.4)	194.9
[117]	–	−119.13 (1)	190.3	8.93 (1.2)	199.8
[165]	–	−102 (0.1)	190.2	–	–
	–	−122.4 (1)	189.7	–	–
[166]	–	−121.3 (1)	191.1	–	–
[77]	–	−126.2 (1)	199.0	–	–
	–	−144.4 (8)	199.1	–	–
[150]	–	−111 (1)	179.2	8.99 (1.5)	188.7
	–	−133 (1, locked)	200.4	–	–
[148]	–	−105.9 (0.4)	185.9	7.30 (1.05)	194.6
	–	−106.4 (0.4)	184.8	7.30 (1.05)	193.4
[119]	–	−73.62 (0.6)	156.6	5.19 (1.5)	163.8
	–	−82.44 (1)	161.0	5.19 (1.5)	168.2
[155]	–	−121.6 (0.6)	194.2	–	–
	–	−116.1 (0.6)	195.1	–	–
[234]	2.8 (100 MHz)	−82 (0.01)	148.4	–	–
[3]	2 (125 MHz)	−82 (0.01)	150.2	–	–
[238]	–	–	–	–	–
[250, 251]	–	– (4, 100 k)	146.0	–	–
	–	– (10 k)	148.0	–	–
[29]	455	–	135.9[a]	–	–
[94]	65	−102 (10 k)	150.7	–	–
[90]	–	−82.125 (10 k)	162.0	–	–
[192]	<0.1 %	–	–	–	–
[275]	<0.1 %	–	–	–	–
[195]	–	–	–	–	–
[162]	–	–	–	–	–
[254]	–	−50 (10 Hz)	136.7	–	–
	–	−89 (1 kHz)	137.4	–	–
[197]	–	–	–	–	–
	–	–	–	–	–
[244]	–	–	–	–	–

(continued)

Table D.2 (continued)

References	Jit. (ps)	PN (Δf) (dB) (MHz)	FoM_{PN} (dB)	Tuning (Range) (%/V) (V)	$FoM_{PN,tuned}$ (dB)
[149]	–	–	–	–	–
[257]	–	−32 (1 k)	129.0	–	–
	–	−96 (1)	133.0	–	–
[225]	52 n	–	109.6[a]	–	–
[227]	–	–	–	–	–
	–	–	–	–	–
[71]	–	–	–	–	–
[126]	320	–	119.2[a]	–	–
T-Wien bridge	127[a]	−73.7 (10 k)	141.1	–	–
	127[a]	−94.6 (100 k)	142.0	–	–
V-Wien bridge	–	–	–	–	–
Pulsed oscillator	49.6	–	142.7[a]	–	–
Inj.-locked 1	–	–	–	–	–
Inj.-locked 2	–	–	–	–	–

[a] Calculation based on the reported jitter/phase noise value, using (3.63)

Table D.3 Comparison to the state of the art: voltage dependency

References	V-range (V)	Rel. V-range (%)	Sensitivity (ppm/V)	Sensitivity (ppm/%)	Remarks
[178]	4.5–5.5	20.0	38	1.85	Bandgap reg.
	4.5–5.5	20.0	38	1.85	Bandgap reg.
[177]	2.97–3.63	20.0	91	3.00	Open loop, bandgap
	2.97–3.63	20.0	91	3.00	Open loop, bandgap
[175]	3.0–3.6	18.2	3.3[a]	0.11[a]	Bandgap reg.
[281]	–	–	–	–	–
	–	–	–	–	–
[252]	–	–	–	–	–
	–	–	–	–	–
[117]	–	–	–	–	–
[165]	–	–	–	–	–
	–	–	–	–	–
[166]	–	–	–	–	–
[77]	–	–	–	–	–
	–	–	–	–	–
[150]	–	–	–	–	–
	–	–	–	–	–

(continued)

Table D.3 (continued)

References	V-range (V)	Rel. V-range (%)	Sensitivity (ppm/V)	Sensitivity (ppm/%)	Remarks
[148]	–	–	–	–	–
	–	–	–	–	–
[119]	–	–	–	–	–
	–	–	–	–	–
[155]	–	–	–	–	–
	–	–	–	–	–
[234]	3–3.6	18.2	100	3.3	T-Null
[3]	3–3.6	18.2	167	5.5	T-Null
[238]	–	–	–	–	–
[250, 251]	1.7–1.9	11.1	16,000	288	V-avg. feedback
	1.7–1.9	11.1	16,000	288	V-avg. feedback
[29]	1.4–1.6	13.3	40,000	600	Offset canceling
[94]	–	–	–	–	–
[90]	–	–	–	–	–
[192]	2.5–5.5	75.0	5,500	222	Bandgap reg.
[275]	3.0–5.5	58.8	6,400	272	Bandgap reg.
[195]	1.8–2.5	32.6	2.8*e*5	6140	Self-biasing
[162]	–	–	50,000	900	Self-biasing
[254]	0.8–1.8	76.9	9,800	127	PN-resistor
	0.8–1.8	76.9	9,800	127	PN-resistor
[197]	1.5–3.3	75.0	10,000	240	Bandgap ref.
	1.5–3.3	75.0	10,000	240	Bandgap ref.
[244]	2.4–2.75	13.6	17,700	456	Bandgap reg.
[149]	1.2–3.0	85.7	556	11.7	Bandgap reg.
[257]	1.8–3.0	50.0	40,000	960	Ext. voltage,
	1.8–3.0	50.0	40,000	960	PN-resistor
[225]	1.12–1.4	22.2	7,140	90	Ext. PTAT
[227]	–	–	–	–	–
	–	–	–	–	–
[71]	1.0–2.5	85.7	35,000	613	MOS PTAT
[126]	–	–	–	–	–
T-Wien bridge	1.08–1.32	20	*25,000*	*300*	PN-resistor
	1.08–1.32	20	*25,000*	*300*	PN-resistor
V-Wien bridge	0.4–1.4	111	104	0.94	Dual. reg.
Pulsed oscillator	0.6–1.6	91	74	0.81	(External) Self-biasing
Inj.-locked 1	0.7–1.6	78	0	0	Inj. locked
Inj.-locked 2	0.7–1.5	73	0	0	AM-Inj. locked

[a] Estimated value from total reported frequency deviation

Table D.4 Comparison to the state of the art: temperature dependency

References	T-Range (°C)	Sensitivity (ppm/°C)	Trimming/ Calibration	Area (core) (mm^2)	Abs. accuracy (ppm)
[178]	−10–85	12.3 (8.1)	Digital	(0.22)	±100
	−10–85	12.3 (8.1)	Digital	(0.22)	±100
[177]	−5–75	5.25 (3.8)	Digital	–	±152[a]
	−5–75	5.25 (3.8)	Digital	–	±152[a]
[175]	0–70	2.3	Digital	0.81	±277[a]
[281]	–	–	–	0.40 (0.14)	–
	–	–	–	0.40 (0.14)	–
[252]	–	–	–	0.41	–
	–	–	–	0.41	–
[117]	–	–	–	0.60	–
[165]	–	–	–	–	–
	–	–	–	–	–
[166]	–	–	–	0.30	–
[77]	–	–	–	–	–
	–	–	–	–	–
[150]	–	–	–	0.79	–
	–	–	–	0.79	–
[148]	–	–	–	2.00	–
	–	–	–	2.00	–
[119]	–	–	–	0.59	–
	–	–	–	0.59	–
[155]	–	–	–	0.73	–
	–	–	–	0.73	–
[234]	−40–85	3.5 (1.6)	Dig.ext.wobble	–	±40
[3]	0–70	1 (0.29)	Dig.ext.wobble	–	±50
[238]	–	–	–	–	–
[250, 251]	−40–125	150 (91)	No	(0.04)	*±4,000*
	−40–125	150 (91)	No	(0.04)	*±4,000*
[29]	20–60	125	Digital, 1-pt.	(0.073)	±1,500
[94]	–	–	–	(1.17)	–
[90]	–	–	–	(0.03)	–
[192]	−40–125	625 (424)	Digital, 1-pt.	(0.18)	–
[275]	−40–125	303	Digital, 1-pt.	(0.19)	–
[195]	−35–85	417	1-Point	2.9 (0.015)	–

(continued)

Table D.4 (continued)

References	T-Range (°C)	Sensitivity (ppm/°C)	Trimming/ Calibration	Area (core) (mm^2)	Abs. accuracy (ppm)
[162]	−45–80	4,000	1-Point	(0.016)	±155
[254]	−40–120	56.9	No	(0.09)	±8,000
	−40–120	56.9	No	(0.09)	±8,000
[197]	0–90	22.2	No	(0.032)	–
	−40–90	38.5	No	(0.032)	–
[244]	−40–125	315 (60–102)	No	1.6	±22,000
[149]	−20–120	66.7	No	(0.22)	–
[257]	−20–100	90	No	(0.08)	±27,000
	−20– 100	90	No	(0.08)	±27,000
[225]	−40–85	320	1-Point	(0.11)	±37,00
[227]	−55–125	55.6	2-Point	(0.2)	±60,000[b]
	−55–125	300	1-Point	(0.2)	±60,000[b]
[71]	−20–80	500	No	(0.1)	±2*e*5
[126]	−55–125	11.2	1-Point	6.75	±1,000
T-Wien bridge	0–120	86.1 (75)	No	(0.03)	±8,800
	0–120	*33*	No	(0.03)	±8,800
V-Wien bridge	–	1*e*4	No	(0.03)	±4,600
Pulsed oscillator	−40–100	48–1,540	No	2.63	±7,600
Inj.-locked 1	−20–100	950–1,150	No	0.18 (0.0022)	–
Inj.-locked 2	−20–100	23–36	No	0.165 (0.0017)	–

[a] Including all external variations
[b] Uncompensated, before trimming

References

1. Adams, J.: An introduction to IEEE std 802.15.4. In: Aerospace Conference, 2006 IEEE, 8 pp. (2006). doi:10.1109/AERO.2006.1655947
2. Adler, R.: A study of locking phenomena in oscillators. In: Proceedings of the IRE **34**(6), 351–357 (1946). doi:10.1109/JRPROC.1946.229930
3. Ahmed, A., Hanafi, B., Hosny, S., Sinoussi, N., Hamed, A., Samir, M., Essam, M., El-Kholy, A., Weheiba, M., Helmy, A.: A highly stable cmos self-compensated oscillator (sco) based on an lc tank temperature null concept. In: Frequency Control and the European Frequency and Time Forum (FCS), 2011 Joint Conference of the IEEE International, pp. 1–5 (2011). doi:10.1109/FCS.2011.5977850
4. Alford, R.C., Stengel, R.E., Weisman, D.H., Marlin, G.W.: Method of forming a three-dimensional integrated inductor (1999). US Patent 6,008,102
5. Allan, D.: Should the classical variance be used as a basic measure in standards metrology? IEEE Trans. Instrum. Measur. **IM-36**(2), 646–654 (1987). doi:10.1109/TIM.1987.6312761
6. Andreani, P., Sjoland, H.: Tail current noise suppression in rf cmos vcos. IEEE J. Solid-State Circ. **37**(3), 342–348 (2002). doi:10.1109/4.987086
7. Appleton, E., Greaves, W.: XLIII on the solution of the representative differential equation of the triode oscillator. Lond. Edinb. Dublin Philos. Mag. J. Sci. **45**(267), 401–414 (1923)
8. Arden, W.M.: The international technology roadmap for semiconductorsperspectives and challenges for the next 15 years. Curr. Opin. Solid State Mater. Sci. **6**(5), 371–377 (2002)
9. Atalla, M., Tannenbaum, E., Scheibner, E.: Stabilization of silicon surfaces by thermally grown oxides. Bell Syst.Tech. J. **38**, 749–783 (1959)
10. Baghaei-Nejad, M., Mendoza, D., Zou, Z., Radiom, S., Gielen, G., Zheng, L.R., Tenhunen, H.: A remote-powered rfid tag with 10mb/s uwb uplink and −18.5 dbm sensitivity uhf downlink in 0.18 μm cmos. In: Solid-State Circuits Conference—Digest of Technical Papers, 2009. ISSCC 2009. IEEE International, pp. 198–199,199a (2009). doi:10.1109/ISSCC.2009.4977376
11. Ball, P.: Nature news - precise atomic clock may redefine time. http://www.nature.com/news/precise-atomic-clock-may-redefine-time-1.13363 (2013)
12. Bastos, J., Steyaert, M., Graindourze, B., Sansen, W.: Matching of mos transistors with different layout styles. In: ICMTS 1996. Proceedings. IEEE International Conference on Microelectronic Test Structures, pp. 17–18 (1996). doi:10.1109/ICMTS.1996.535615
13. Batur, O., Akdag, E., Akkurt, H., Oncu, A., Koca, M., Dundar, G.: An ultra low-power dual-band ir-uwb transmitter in 130-nm cmos. IEEE Trans. Circ. Syst. II: Express Briefs **59**(11), 701–705 (2012). doi:10.1109/TCSII.2012.2218474
14. Behzad, A., Shi, Z.M., Anand, S., Lin, L., Carter, K., Kappes, M., Lin, T.H., Nguyen, T., Yuan, D., Wu, S., Wong, Y.C., Fong, V., Rofougaran, A.: A 5-GHz direct-conversion CMOS transceiver utilizing automatic frequency control for the IEEE 802.11 a wireless LAN standard. IEEE J. Solid State Circ. **38**(12), 2209–2220 (2003). doi:10.1109/JSSC.2003.819085
15. Bellis, M.: History of electromagnetism—innovations using magnetic fields. http://inventors.about.com/od/estartinventions/a/Electromagnets.htm (2013)

V. De Smedt et al., *Temperature- and Supply Voltage-Independent Time References for Wireless Sensor Networks*, Analog Circuits and Signal Processing 128,
DOI 10.1007/978-3-319-09003-0

16. Bellis, M.: The history of the integrated circuit aka microchip. http://inventors.about.com/od/istartinventions/a/intergrated_circuit.htm (2013)
17. Belmans, R.: Elektrische energie-Dl 2. Garant (2002)
18. Beow Yew Tan, P., Victor Kordesch, A., Sidek, O.: Analysis of Poly Resistor Mismatch. ICSE'06. IEEE International Conference on Semiconductor Electronics, 2006, pp. 1028–1029 (2006). doi:10.1109/SMELEC.2006.380795
19. Bracke, W., Merken, P., Puers, R., Van Hoof, C.: Ultra-low-power interface chip for autonomous capacitive sensor systems. IEEE Trans. Circ. Syst. I: Regul. Pap. **54**(1), 130–140 (2007). doi:10.1109/TCSI.2006.887978
20. Brandt, L.: Rückblick auf die deutsche funkmeßtechnik. In: Forschen und Gestalten. Springer, Berlin, pp. 53–79 (1962)
21. Bucher, M., Lallement, C., Enz, C., Krummenacher, F.: Accurate mos modelling for analog circuit simulation using the ekv model. In: 1996 IEEE International Symposium on Circuits and Systems, 1996. ISCAS'96, Connecting the World, vol. 4, pp. 703–706 (1996). doi:10.1109/ISCAS.1996.542121
22. Budak, A., Nay, K.: Operational amplifier circuits for the Wien-bridge oscillator. IEEE Trans. Circ. Syst. **28**(9), 930–934 (1981)
23. Buisson, O.R.D., Morin, G.: Mosfet matching in a deep submicron technology. In: Solid State Device Research Conference, 1996. ESSDERC'96. Proceedings of the 26th European, pp. 731–734 (1996)
24. Canada, R.W.: Boost in rfid from gigantic growth of internet of things (iot) and internet of objects (ioo). http://www.rfidworld.ca/boost-in-rfid-from-gigantic-growth-of-internet-of-things-iot-and-internet-of-objects-ioo/1691 (2013)
25. Carnes, J., Vytyaz, I., Hanumolu, P., Mayaram, K., Moon, U.K.: Design and analysis of noise tolerant ring oscillators using maneatis delay cells. In: 14th IEEE International Conference on Electronics, Circuits and Systems, 2007. ICECS 2007, pp. 494–497 (2007). doi:10.1109/ICECS.2007.4511037
26. Chee, Y.H., Niknejad, A., Rabaey, J.: An ultra-low-power injection locked transmitter for wireless sensor networks. IEEE J. Solid State Circ. **41**(8), 1740–1748 (2006). doi:10.1109/JSSC.2006.877254
27. Cheng, Y.: The influence and modeling of process variation and device mismatch for analog/rf circuit design. In: Proceedings of the Fourth IEEE International Caracas Conference on Devices, Circuits and Systems, 2002, pp. D046-1–D046-8 (2002). doi:10.1109/ICCDCS.2002.1004068
28. Cho, H., Bae, J., Yoo, H.J.: A 37.5 μw body channel communication wake-up receiver with injection-locking ring oscillator for wireless body area network. In: IEEE Trans. Circ. Syst. I: Regul. Pap. **60**(5), 1200–1208 (2013). doi:10.1109/TCSI.2013.2249173
29. Choe, K., Bernal, O., Nuttman, D., Je, M.: A precision relaxation oscillator with a self-clocked offset-cancellation scheme for implantable biomedical socs. In: Solid-State Circuits Conference—Digest of Technical Papers, 2009. ISSCC 2009. IEEE International, pp. 402–403, 403a (2009). doi:10.1109/ISSCC.2009.4977478
30. Choi, Y.S., Yoon, J.B.: Experimental analysis of the effect of metal thickness on the quality factor in integrated spiral inductors for RF ICS. IEEE Electron Device Lett. **25**(2), 76–79 (2004). doi:10.1109/LED.2003.822652
31. Chuang, H.M., Thei, K.B., Tsai, S.F., Liu, W.C.: Temperature-dependent characteristics of polysilicon and diffused resistors. IEEE Trans. Electron Devices **50**(5), 1413–1415 (2003). doi:10.1109/TED.2003.813472
32. Clarke, K.: Wien bridge oscillator design. Proc. IRE **41**(2), 246–249 (1953). doi:10.1109/JRPROC.1953.274213
33. Compaq, Hewlett-Packard, Intel, Lucent, Microsoft, NEC, Philips: Universal serial bus specification, rev.2.0, apr. 27, 2000. Sec 7(1) (2000)
34. Couch, L.W., Kulkarni, M., Acharya, U.S.: Digital and analog communication systems, vol. 6. Prentice Hall, Upper Saddle River (1997)

35. Couch, L.W.: A study of a driven oscillator with fm feedback by use of a phase-lock-loop model. IEEE Trans. Microwave Theor. Techniques **19**(4), 357–366 (1971). doi:10.1109/TMTT.1971.1127520
36. Courant, R., Hilbert, D.: Methods of Mathematical Physics, vol. 1. Wiley, London (2008)
37. Craninckx, J., Steyaert, M.: A 1.8-GHz CMOS low-phase-noise voltage-controlled oscillator with prescaler. IEEE J. Solid-State Circ. **30**(12), 1474–1482 (1995). doi:10.1109/4.482195
38. Craninckx, J., Steyaert, M.: Low-noise voltage-controlled oscillators using enhanced LC-tanks. IEEE Trans. Circ. Syst. II Analog Digital Signal Process. **42**(12), 794–804 (1995). doi:10.1109/82.476177
39. Crepaldi, M., Li, C., Fernandes, J., Kinget, P.: An ultra-wideband impulse-radio transceiver chipset using synchronized-OOK modulation. IEEE J. Solid-State Circ. **46**(10), 2284–2299 (2011). doi:10.1109/JSSC.2011.2161214
40. Cunha, A., Schneider, M., Galup-Montoro, C.: An MOS transistor model for analog circuit design. IEEE J. Solid-State Circ. **33**(10), 1510–1519 (1998). doi:10.1109/4.720397
41. Cutler, L., Searle, C.: Some aspects of the theory and measurement of frequency fluctuations in frequency standards. Proc. IEEE **54**(2), 136–154 (1966). doi:10.1109/PROC.1966.4627
42. D'Angelo, K.P., Wrathall, R.S.: Compact low dropout voltage regulator using enhancement and depletion mode MOS transistors (1999)
43. Danneels, H.: CMOS, time-based, digital-oriented, integrated sensor interfaces (CMOS, tijdsgebaseerde, digitaal georienteerde, geintegreerde sensor interfaces) (2013)
44. Danneels, H., Coddens, K., Gielen, G.: An enhanced, highly linear, fully-differential PLL-based sensor interface. Procedia Engineering, vol 46. (2011)
45. Danneels, H., Coddens, K., Gielen, G.: A fully-digital, 0.3v, 270 nw capacitive sensor interface without external references. In: 2011 Proceedings of the ESSCIRC (ESSCIRC), pp. 287–290 (2011). doi:10.1109/ESSCIRC.2011.6044963
46. Danneels, H., De Smedt, V., De Roover, C., Radiom, S., Van Helleputte, N., Walravens, C., Li, Z., Steyaert, M., Verhelst, M., Dehaene, W., et al.: An ultra-low-power, batteryless microsystem for wireless sensor networks. Procedia Eng. **47**, 1406–1409 (2012)
47. Darabi, H., Abidi, A.: Noise in rf-cmos mixers: a simple physical model. IEEE J. Solid State Circ. **35**(1), 15–25 (2000). doi:10.1109/4.818916
48. De Muer, B., Borremans, M., Steyaert, M., Li Puma, G.: A 2-GHz low-phase-noise integrated lc-vco set with flicker-noise upconversion minimization. IEEE J. Solid State Circ. **35**(7), 1034–1038 (2000). doi:10.1109/4.848213
49. De Muer, B., Itoh, N., Borremans, M., Steyaert, M.: A 1.8 GHz highly-tunable low-phase-noise CMOS VCO. In: Proceedings of the IEEE 2000 Custom Integrated Circuits Conference, 2000. CICC, pp. 585–588 (2000). doi:10.1109/CICC.2000.852736
50. De Roose, F., De Smedt, V., Volkaerts, W., Steyaert, M., Gielen, G., Reynaert, P., Dehaene, W.: Design of a frequency reference based on a PVT-independent transmission line delay. In: IEEE International Symposium on Circuits and Systems, 2014. ISCAS '14, 1996, Accepted for publication. (2014)
51. De Roover, C.: Wireless energy supply and low power circuits for RFID applications (draadloze energievoorziening en laag vermogen schakelingen voor rfid toepassingen). status: published (2011)
52. De Roover, C., Steyaert, M.: A fully integrated wireless power supply for pinless active RFID-devices in 130 nm CMOS. Solid-State Circuits Conference, 2007. ASSCC '07. IEEE Asian pp. 123–126 (2007). doi:10.1109/ASSCC.2007.4425747
53. De Smedt, V., De Wit, P., Vereecken, W., Steyaert, M.: A fully-integrated wienbridge topology for ultra-low-power 86 ppm/°c 65nm CMOS 6 MHz clock reference with amplitude regulation. In: Solid-State Circuits Conference, 2008. ESSCIRC 2008. 34th European, pp. 394–397 (2008). doi:10.1109/ESSCIRC.2008.4681875
54. De Smedt, V., De Wit, P., Vereecken, W., Steyaert, M.: A 66 μw 86 ppm/c fully-integrated 6 mhz wienbridge oscillator with a 172 db phase noise fom. IEEE J. Solid State Circ. JSSC **44**(7), 1990–2001 (2009). doi:10.1109/JSSC.2009.2021914

55. De Smedt, V., Dehaene, W., Gielen, G.: A 0.4–1.4 v 24mhz fully integrated 33 μw, 104ppm/v supply-independent oscillator for rfids. In: Proceedings of ESSCIRC, 2009. ESSCIRC '09. pp. 396–399 (2009). doi:10.1109/ESSCIRC.2009.5325966
56. De Smedt, V., Gielen, G., Dehaene, W.: A 0.6v to 1.6v, 46 μw voltage and temperature independent 48 mhz pulsed lc oscillator for RFID tags. In: Solid State Circuits Conference (A-SSCC), 2011 IEEE Asian, pp. 109–112 (2011). doi:10.1109/ASSCC.2011.6123616
57. De Smedt, V., Gielen, G., Dehaene, W.: A 127 μw exact timing reference for wireless sensor networks based on injection locking. In: Proceedings of the ESSCIRC (ESSCIRC), 2012, pp. 262–264 (2012). doi:10.1109/ESSCIRC.2012.6341335
58. De Smedt, V., Gielen, G., Dehaene, W.: A novel, highly linear, voltage and temperature independent sensor interface using pulse width modulation. Procedia Engineering 47(0), 1215–1218 (2012). http://dx.doi.org/10.1016/j.proeng.2012.09.371. http://www.sciencedirect.com/science/article/pii/S1877705812044347. 26th European Conference on Solid-State Transducers, EUROSENSORS 2012
59. De Smedt, V., Gielen, G., Dehaene, W.: A 40nm-cmos, 18 μw, temperature and supply voltage independent sensor interface for RFID tags. In: Solid-State Circuits Conference (A-SSCC), 2013 IEEE Asian, pp. 113–116 (2013). doi:10.1109/ASSCC.2013.6690995
60. De Smedt, V., Gielen, G., Dehaene, W.: Development of an ultra-low-power injection-locked PSK receiver architecture. IEEE Transactions on Circuits and Systems—TCAS II, Accepted for publication (2014)
61. De Smedt, V., Gielen, G., Dehaene, W.: Impact analysis of deep-submicron CMOS technologies on the voltage- and temperature-independence of a time-domain sensor interface. Analog integrated Circuits and Signal Processing, Minor revisions (2014)
62. De Smedt, V., Gielen, G.G.E., Dehaene, W.: Transient behavior and phase noise performance of pulsed-harmonic oscillators, In: IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 61, no.7, pp.2119–2128 (2014). doi:10.1109/TCSI.2014.2304670
63. De Smedt, V., Steyaert, W., Dehaene, W., Gielen, G.: Wobble-based on-chip calibration circuit for temperature independent oscillators. Electron. Lett. **48**(16), 1000–1001 (2012)
64. De Wit, M.: Temperature independent resistor (1995). US Patent 5,448,103
65. De Wit, P., Gielen, G.: Design for Variability and Reliability of Analog Integrated Circuits in Nanometer CMOS Technology. KU Leuven—PhD (2013)
66. Dehaene, W., Gielen, G., Steyaert, M., Danneels, H., Desmedt, V., De Roover, C., Li, Z., Verhelst, M., Van Helleputtea, N., Radioma, S., Walravens, C., Pleysier, L.: RFID, where are they? In: Proceedings of ESSCIRC, 2009. ESSCIRC '09. pp. 36–43 (2009). doi:10.1109/ESSCIRC.2009.5325928
67. Demir, A.: Phase noise in oscillators: Daes and colored noise sources. In: Proceedings of the 1998 IEEE/ACM International Conference on Computer-Aided Design, pp. 170–177. ACM (1998)
68. Demir, A.: Phase noise and timing jitter in oscillators with colored-noise sources. IEEE Trans. Circ. Syst. I: Fundam. Theory Appl. **49**(12), 1782–1791 (2002). doi:10.1109/TCSI.2002.805707
69. Demir, A., Mehrotra, A., Roychowdhury, J.: Phase noise and timing jitter in oscillators. In: Proceedings of the IEEE 1998 Custom Integrated Circuits Conference, 1998, pp. 45–48. IEEE (1998)
70. Demir, A., Mehrotra, A., Roychowdhury, J.: Phase noise in oscillators: a unifying theory and numerical methods for characterization. IEEE Trans. Circ. Syst. I: Fundam. Theory Appl. **47**(5), 655–674 (2000). doi:10.1109/81.847872
71. Denier, U.: Analysis and design of an ultralow-power cmos relaxation oscillator. IEEE Trans. Circ. Syst. I: Regular Papers **57**(8), 1973–1982 (2010). doi:10.1109/TCSI.2010.2041504
72. Deval, Y., Tomas, J., Begueret, J., Lapuyade, H., Dom, J.: 1-V low-noise 200 MHz relaxation oscillator. Solid-State Circuits Conference, 1997. ESSCIRC '97. Proceedings of the 23rd European pp. 220–223 (1997)
73. Dictionary, C.: Wireless sensor network (2013). http://www.collinsdictionary.com/dictionary/english/wireless-sensor-networking

74. Dictionary, T.F.: Oscillator (2013). http://www.thefreedictionary.com/oscillator
75. Dierickx, B., Simoen, E.: The decrease of random telegraph signalnoise in metal-oxide-semiconductor field-effect transistors when cycled from inversion to accumulation. J. Appl. Phys. **71**(4), 2028–2029 (1992)
76. Djurhuus, T., Krozer, V.: Theory of injection-locked oscillator phase noise. IEEE Trans. Circ. Syst. I Reg. Pap. **58**(2), 312–325 (2011). doi:10.1109/TCSI.2010.2071770
77. Ebrahimzadeh, M.: Design of an ultra low power low phase noise cmos LC oscillator. World Academy of Science (2011)
78. Elrazaz, Z., Sinha, N.: On the selection of the dominant poles of a system to be retained in a low-order model. IEEE Trans. Autom. Control **24**(5), 792–793 (1979). doi:10.1109/TAC.1979.1102141
79. Office of Engineering and Technology, Federal Communications Commission.: Understanding the fcc regulations for low-power, non-licensed transmitters (1993)
80. Enz, C.C., Krummenacher, F., Vittoz, E.A.: An analytical MOS transistor model valid in all regions of operation and dedicated to low-voltage and low-current applications. Analog Integr. Circ. Sig. Process. **8**(1), 83–114 (1995)
81. Erc, E.R.C.: Spinoff company: Mobius microsystems (2013). http://erc-assoc.org/about/erc_data/spinoff-company-mobius-microsystems
82. Ferre-Pikal, E., Vig, J., Camparo, J., Cutler, L., Maleki, L., Riley, W., Stein, S., Thomas, C., Walls, F., White, J.: Draft revision of IEEE std 1139–1988 standard definitions of physical quantities for fundamental, frequency and time metrology-random instabilities. In: Proceedings of the 1997 IEEE International Frequency Control Symposium, 1997, pp. 338–357 (1997) doi:10.1109/FREQ.1997.638567.
83. Filanovsky, I., Allam, A.: Mutual compensation of mobility and threshold voltage temperature effects with applications in cmos circuits. IEEE Trans. Circ. Syst. I Fundame. Theory Appl. **48**(7), 876–884 (2001). doi:10.1109/81.933328
84. Fraedrich, K.: Estimating weather and climate predictability on attractors. J. Atmos. Sci. **44**(4), 722–728 (1987)
85. Frishman, F.: On the Arithmetic Means and Variances of Products and Ratios of Random Variables. Springer, Berlin (1975)
86. Fuhring, J.: An early coherer radio receiver (2012). http://www.geojohn.org/Radios/MyRadios/Coherer/Coherer.html
87. Galindo, F.J., Palacio, J.: Estimating the instabilities of n correlated clocks. Tech. rep, DTIC Document (1999)
88. Gambini, S., Pletcher, N., Rabaey, J.M.: Sensitivity analysis for am detectors. EECS Department, University of California, Berkeley, Tech. Rep. UCB/EECS-2008-31 (2008)
89. Gangasani, G., Kinget, P.: A time-domain model for predicting the injection locking bandwidth of nonharmonic oscillators. IEEE Trans. Circ. Syst. II: Exp. Briefs **53**(10), 1035–1038 (2006). doi:10.1109/TCSII.2006.882239
90. Geraedts, P., Van Tuijl, E., Klumperink, E., Wienk, G., Nauta, B.: A 90 μw 12 mhz relaxation oscillator with a −162 db fom. In: IEEE International Solid-State Circuits Conference, 2008. ISSCC 2008. Digest of Technical Papers, pp. 348–618 (2008). doi:10.1109/ISSCC.2008.4523200
91. Geraedts, P.F., Tuijl, E.A., Klumperink, E.A., Wienk, G.J., Nauta, B.: Towards minimum achievable phase noise of relaxation oscillators. International Journal of Circuit Theory and Applications (2012)
92. Gierkink, S.L.J.: Control linearity and jitter of relaxation oscillators. Universiteit Twente (1999)
93. Gierkink, S.L.J., Klumperink, E., van der Wel, A., Hoogzaad, G., Van Tuijl, E., Nauta, B.: Intrinsic 1/f device noise reduction and its effect on phase noise in cmos ring oscillators. IEEE J. Solid State Circ. **34**(7), 1022–1025 (1999). doi:10.1109/4.772418
94. Gierkink, S.L.J., van Tuijl, E.: A coupled sawtooth oscillator combining low jitter with high control linearity. IEEE J. Solid State Circ. **37**(6), 702–710 (2002). doi:10.1109/JSSC.2002.1004574

95. Goebel, G.: The british invention of radar (2011). http://www.vectorsite.net/ttwiz_01.html
96. Gonzalez, R., Gordon, B.M., Horowitz, M.A.: Supply and threshold voltage scaling for low power CMOS. IEEE J. Solid-State Circ. **32**(8), 1210–1216 (1997)
97. Grey, P.R., Meyer, R.G.: Analysis and Design of Analog Integrated Circuits. Wiley, New York (1993)
98. Groszkowski, J.: The interdependence of frequency variation and harmonic content, and the problem of constant-frequency oscillators. Proc. Insti. Radio Eng. **21**(7), 958–981 (1933). doi:10.1109/JRPROC.1933.227821
99. Ha, H., Suh, Y., Lee, S.K., Park, H.J., Sim, J.Y.: A 0.5v, 11.3-μw, 1-ks/s resistive sensor interface circuit with correlated double sampling. In: Custom Integrated Circuits Conference (CICC), 2012 IEEE, pp. 1–4 (2012). doi:10.1109/CICC.2012.6330702
100. Hajimiri, A., Lee, T.: Corrections to "a general theory of phase noise in electrical oscillators". IEEE J. Solid State Circ. 33(6), 928–928 (1998). doi:10.1109/4.678662
101. Hajimiri, A., Lee, T.: A general theory of phase noise in electrical oscillators. IEEE J. Solid State Circ. **33**(2), 179–194 (1998). doi:10.1109/4.658619
102. Hajimiri, A., Lee, T.: Design issues in cmos differential LC oscillators. IEEE J. Solid State Circ. **34**(5), 717–724 (1999). doi:10.1109/4.760384
103. Hajimiri, A., Lee, T.H.: Phase noise in CMOS differential LC oscillators. In: 1998 Symposium on VLSI Circuits, 1998. Digest of Technical Papers. pp. 48–51. IEEE (1998)
104. Hajimiri, A., Limotyrakis, S., Lee, T.: Jitter and phase noise in ring oscillators. IEEE J. Solid State Circ. **34**(6), 790–804 (1999). doi:10.1109/4.766813
105. Han, J., Nguyen, C.: On the development of a compact sub-nanosecond tunable monocycle pulse transmitter for UWB applications. IEEE Trans. Microwave Theory Tech. **54**(1), 285–293 (2006). doi:10.1109/TMTT.2005.860299
106. Hanson, S., Zhai, B., Bernstein, K., Blaauw, D., Bryant, A., Chang, L., Das, K.K., Haensch, W., Nowak, E.J., Sylvester, D.M.: Ultralow-voltage, minimum-energy CMOS. IBM J. Res. Dev. **50**(4/5), 469–490 (2006). http://dl.acm.org/citation.cfm?id=1167704.1167714
107. Harris, D.: Lecture 21: Scaling and economics (2004). http://www.cmosvlsi.com/lect21.pdf
108. Hashemi, S., Ghafoorifard, H., Abdipour, A.: Amplitude noise of electrical oscillators based on the LTV model. Electron. Electr. Eng. **18**(8), 31–36 (2012)
109. Helmy, A., Sinoussi, N., Elkholy, A., Essam, M., Hassanein, A., Ahmed, A.: A monolithic CMOS self-compensated LC oscillator across temperature. In: Frequency References, Power Management for SoC, and Smart Wireless Interfaces, pp. 3–22. Springer, Berlin (2014)
110. Herzel, F., Razavi, B.: A study of oscillator jitter due to supply and substrate noise. Circuits and Systems II: Analog and Digital Signal Processing, IEEE Transactions on 46(1), 56–62 (1999). doi:10.1109/82.749085.
111. Hocquet, C., Kamel, D., Regazzoni, F., Legat, J.D., Flandre, D., Bol, D., Standaert, F.X.: Harvesting the potential of nano-CMOS for lightweight cryptography: an ultra-low-voltage 65 nm AES coprocessor for passive RFID tags. J. Cryptographic Eng. **1**(1), 79–86 (2011)
112. Hsiao, K.J.: A 1.89nw/0.15v self-charged XO for real-time clock generation. In: Solid-State Circuits Conference, 2014. ISSCC 2014. Digest of Technical Papers. IEEE International, pp. 298–299 (2014)
113. Huang, X., Ba, A., Harpe, P., Dolmans, G., de Groot, H., Long, J.: A 915mhz 120 μw-rx/900 μw-tx envelope-detection transceiver with 20db in-band interference tolerance. In: 2012 IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC), pp. 454–456 (2012). doi:10.1109/ISSCC.2012.6177088
114. Irwin, J.D., Nelms, R.M.: Basic Engineering Circuit Analysis. Wiley, New York (2008)
115. Iwai, H.: CMOS downsizing toward sub-10 nm. Solid-State Electron. **48**(4), 497–503 (2004)
116. Jana, P., Nandi, R.: Single current conveyor tunable sinewave RC oscillator. Electron. Lett. **20**(1), 44–45 (1984). doi:10.1049/el:19840031
117. Jang, S.L., Liu, C.C., Wu, C.Y., Juang, M.H.: A 5.6 GHz low power balanced vco in 0.18 μm CMOS. Microwave Wireless Compon. Lett. IEEE **19**(4), 233–235 (2009). doi:10.1109/LMWC.2009.2015507

118. Johnson, J.B.: Thermal agitation of electricity in conductors. Phys. Rev. **32**, 97–109 (1928). doi:10.1103/PhysRev.32.97.http://link.aps.org/doi/10.1103/PhysRev.32.97
119. Jou, C.F., Cheng, K.H., Hsieh, H.C.: An ultra low power 2.4 GHz CMOS VCO. In: Proceedings of the 2003 10th IEEE International Conference on Electronics, Circuits and Systems, 2003. ICECS 2003, vol. 3, pp. 1098–1100. IEEE (2003)
120. Kaajakari, V.: Theory and analysis of MEMS resonators (2011). http://www.ieee-uffc.org/frequency-control/learning/pdf/Kaajakari-MEMS_Resonators_v2b.pdf
121. Kaertner, F.X.: Analysis of white and f- α noise in oscillators. Int. J. Circ. Theory Appl. **18**(5), 485–519 (1990)
122. Kahng, D.: Electric field controlled semiconductor device (1963)
123. Kalia, S., Elbadry, M., Sadhu, B., Patnaik, S., Qiu, J., Harjani, R.: A simple, unified phase noise model for injection-locked oscillators. In: Radio Frequency Integrated Circuits Symposium (RFIC), 2011 IEEE, pp. 1–4 (2011). doi:10.1109/RFIC.2011.5940707
124. Kamon, M., Tsuk, M.J., White, J.: Fasthenry: a multipole-accelerated 3-d inductance extraction program pp. 678–683 (1993). http://doi.acm.org/10.1145/157485.165090
125. Kashmiri, S., Makinwa, K.A.A.: Measuring the thermal diffusivity of cmos chips. In: Sensors, 2009 IEEE, pp. 45–48 (2009). doi:10.1109/ICSENS.2009.5398125
126. Kashmiri, S., Pertijs, M.A.P., Makinwa, K.A.A.: A thermal-diffusivity-based frequency reference in standard CMOS with an absolute inaccuracy of ± 0.1 % from -55 °C to 125 °C. IEEE J. Solid-State Circ. **45**(12), 2510–2520 (2010). doi:10.1109/JSSC.2010.2076343
127. Kashmiri, S.M., Makinwa, K.A.: Silicon-based frequency references. In: Electrothermal Frequency References in Standard CMOS. Springer, Berlin, pp. 15–44 (2013)
128. Keller, V.: Re-entangling the thermometer: cornelis drebbels description of his self-regulating oven, the regiment of fire, and the early history of temperature (2013). http://blogs.uoregon.edu/verakeller/files/2013/08/Keller-on-Drebbels-Self-regulating-oven-in-nuncius-v4k192.pdf
129. Kilby, J.: Invention of the integrated circuit. IEEE Trans. Electron Dev. **23**(7), 648–654 (1976). doi:10.1109/T-ED.1976.18467
130. Kilby, J.S.: Method of making miniaturized electronic circuits (1966). http://www.freepatentsonline.com/3261081.html
131. Kim, S.J., Lee, Y.G., Yun, S.K., Lee, H.Y.: Realization of high-q inductors using wirebonding technology. In: The First IEEE Asia Pacific Conference on ASICs, 1999. AP-ASIC '99. pp. 13–16 (1999). doi:10.1109/APASIC.1999.824149
132. King Liu, T.J.: Bulk CMOS scaling to the end of the roadmap (2012). http://www.eecs.berkeley.edu/~tking/presentations/KingLiu_2012VLSI-Cshortcourse
133. Kinget, P.: A fully integrated 2.7 v 0.35 /spl mu/m CMOS VCO for 5 GHz wireless applications. In: 1998 IEEE International Solid-State Circuits Conference, 1998. Digest of Technical Papers. pp. 226–227 (1998). doi:10.1109/ISSCC.1998.672446
134. Kinget, P.: Integrated ghz voltage controlled oscillators. In: Analog Circuit Design, pp. 353–381. Springer, Berlin (1999)
135. Klass, F., Amir, C., Das, A., Aingaran, K., Truong, C., Wang, R., Mehta, A., Heald, R., Yee, G.: A new family of semidynamic and dynamic flip-flops with embedded logic for high-performance processors. IEEE J. Solid State Circ. **34**(5), 712–716 (1999). doi:10.1109/4.760383
136. Klimovitch, G.: Near-carrier oscillator spectrum due to flicker and white noise. In: The 2000 IEEE International Symposium on Circuits and Systems, 2000. Proceedings. ISCAS 2000 Geneva. vol. 1, pp. 703–706 (2000). doi:10.1109/ISCAS.2000.857192
137. Klimovitch, G.: A nonlinear theory of near-carrier phase noise in free-running oscillators. In: Proceedings of the 2000 Third IEEE International Caracas Conference on Devices, Circuits and Systems, 2000, pp. T80/1–T80/6 (2000). doi:10.1109/ICCDCS.2000.869882
138. Koutsoyannopoulos, Y., Papananos, Y.: Systematic analysis and modeling of integrated inductors and transformers in RF IC design. IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing **47**(8), 699–713 (2000). doi:10.1109/82.861403

139. Ku, Y., Sun, X.: Chaos in van der pol's equation. J. Franklin Inst. **327**(2), 197–207 (1990). doi:10.1016/0016-0032(90)90016-C. http://www.sciencedirect.com/science/article/pii/001600329090016C
140. Kuhn, W., Ibrahim, N.: Analysis of current crowding effects in multiturn spiral inductors. IEEE Trans. Microwave Theory Tech. **49**(1), 31–38 (2001). doi:10.1109/22.899959
141. Kuhn, W., Yanduru, N.: Spiral inductor substrate loss modeling in silicon RF ics. In: Radio and Wireless Conference, 1998. RAWCON 98. 1998 IEEE, pp. 305–308 (1998). doi:10.1109/RAWCON.1998.709197
142. LM555 data sheet
143. Laker, K.R., Sansen, W.M.: Design of Analog Integrated circuits and systems, vol. 1. McGraw-Hill, New York (1994)
144. Lam, C.S.: A review of the recent development of mems and crystal oscillators and their impacts on the frequency control products industry. In: Ultrasonics Symposium, 2008. IUS 2008. IEEE, pp. 694–704 (2008). doi:10.1109/ULTSYM.2008.0167
145. Landt, J.: The history of RFID. IEEE Potentials **24**(4), 8–11 (2005)
146. Lane, W., Wrixon, G.T.: The design of thin-film polysilicon resistors for analog IC applications. IEEE Trans. Electron. Dev. 36(4), 738–744 (1989). doi:10.1109/16.22479
147. Lawes, R.: Future trends in high-resolution lithography. Appl. Surf. Sci. **154**, 519–526 (2000)
148. Lee, H., Mohammadi, S.: A subthreshold low phase noise cmos LC VCO for ultra low power applications. Microwave Wireless Compon. Lett. IEEE **17**(11), 796–798 (2007)
149. Lee, J., Cho, S.: A 10mhz 80 μw 67 ppm/ °C CMOS reference clock oscillator with a temperature compensated feedback loop in 0.18 μm CMOS In: 2009 Symposium on VLSI Circuits, pp. 226–227 (2009)
150. Lee, S.H., Jang, S.L., Chuang, Y.H., Chao, J.J., Lee, J.F., Juang, M.H.: A low power injection locked LC-tank oscillator with current reused topology. Microwave and Wireless Compon. Lett. IEEE **17**(3), 220–222 (2007)
151. Lee, T., Hajimiri, A.: Oscillator phase noise: a tutorial. J. Solid State Circ. IEEE **35**(3), 326–336 (2000). doi:10.1109/4.826814
152. Lee, T.H.: Planar Microwave Engineering: A Practical Guide to Theory, Measurement, and Circuits. Cambridge University Press, Cambridge (2004)
153. Lee, Y.G., Yun, S.K., Lee, H.Y.: Novel high-q bondwire inductor for mmic. In: Electron Devices Meeting, 1998. IEDM '98. Technical Digest., International, pp. 548–551 (1998). doi:10.1109/IEDM.1998.746418
154. Leeson, D.: A simple model of feedback oscillator noise spectrum. Proc. IEEE **54**(2), 329–330 (1966). doi:10.1109/PROC.1966.4682
155. Li, G., Afshari, E.: A low-phase-noise multi-phase oscillator based on left-handed LC-ring. IEEE J. Solid-State Circ. **45**(9), 1822–1833 (2010). doi:10.1109/JSSC.2010.2054591
156. Li, Z.: System-Level Exploration for Ultra-Low-Power Wireless Sensor Networks. Status: published (2011)
157. Li, Z., Dehaene, W., Gielen, G.: A 3-tier UWB-based indoor localization scheme for ultra-low-power sensor nodes. In: IEEE International Conference on Signal Processing and Communications, 2007. ICSPC 2007, pp. 995–998 (2007). doi:10.1109/ICSPC.2007.4728489
158. Li, Z., Dehaene, W., Gielen, G.: A 3-tier uwb-based indoor localization system for ultra-low-power sensor networks. IEEE Trans. Wireless Commun. **8**(6), 2813–2818 (2009). doi:10.1109/TWC.2009.080602
159. Libelium: Libelium case studies, 50 sensor applications for a smarter world (2013). URL http://www.libelium.com/case-studies/,http://www.libelium.com/top_50_iot_sensor_applications_ranking/
160. Lilienfeld, J.S.E.: Method and apparatus for controlling electric currents (1930). US Patent 1,745,175
161. Lilienfeld, J.S.E.: Device for controlling electric current (1933). US Patent 1,900,018
162. Lim, J., Lee, K., Cho, K.: Ultra low power RC oscillator for system wake-up using highly precise auto-calibration technique. In: 2010 Proceedings of the ESSCIRC, pp. 274–277 (2010). doi:10.1109/ESSCIRC.2010.5619876

163. Lin, J., Yeh, T., Lee, C., Chen, C., Tsay, J., Chen, S., Hsu, H., Chen, C., Huang, C., Chiang, J., Chang, A., Chang, R., Chang, C., Wang, S., Wu, C., Lin, C., Chu, Y., Chen, S., Hsu, C., Liou, R., Wong, S., Tang, D., Sun, J.: State-of-the-art RF/analog foundry technology. In: Proceedings of the 2002 Bipolar/BiCMOS Circuits and Technology Meeting, 2002. pp. 73–79 (2002) doi:10.1109/BIPOL.2002.1042890
164. Lindsey, W., Chie, C.M.: Identification of power-law type oscillator phase noise spectra from measurements. IEEE Trans. Ins. Meas. 27(1), 46–53 (1978). doi:10.1109/TIM.1978.4314616
165. Liu, P., Upadhyaya, P., Jung, J., Heo, D., Kim, J.H., Kim, B.S.: Dynamically switched low-phase-noise LC VCO with harmonic filtering. Electron. Lett. **47**(14), 792–793 (2011)
166. Liu, P., Upadhyaya, P., Jung, J., Heo, D., Kim, J.H., Kim, B.S.: Low phase noise LC VCO with reduced drain current duty cycle. Electron. Lett. **48**(2), 77–78 (2012)
167. Lopez-Villegas, J., Samitier, J., Cane, C., Losantos, P., Bausells, J.: Improvement of the quality factor of rf integrated inductors by layout optimization. IEEE Trans. Microw. Theory Tech. **48**(1), 76–83 (2000). doi:10.1109/22.817474
168. Lu, N.C., Gerzberg, L., Lu, C.Y., Meindl, J.: Modeling and optimization of monolithic polycrystalline silicon resistors. IEEE Trans. Electron Dev. **28**(7), 818–830 (1981). doi:10.1109/T-ED.1981.20437
169. Maffezzoni, P.: Frequency-shift induced by colored noise in nonlinear oscillators. IEEE Trans. Circ. Syst. II Exp. Briefs **54**(10), 887–891 (2007). doi:10.1109/TCSII.2007.902241
170. Makinwa, K.A.A., Snoeij, M.: A CMOS temperature-to-frequency converter with an inaccuracy of less than ± 0.5°C ($3\,\sigma$) from -40°C to 105°C. IEEE J. Solid State Circ **41**(12), 2992–2997 (2006). doi:10.1109/JSSC.2006.884865
171. Maneatis, J.: Low-jitter process-independent DLL and PLL based on self-biased techniques. IEEE J. Solid State Circ. **31**(11), 1723–1732 (1996). doi:10.1109/JSSC.1996.542317
172. Maricau, E., Gielen, G.: Analog IC Reliability in Nanometer CMOS. Springer, Berlin (2013)
173. Martins, N., Lima, L., Pinto, H.: Computing dominant poles of power system transfer functions. IEEE Trans. Power Syst. **11**(1), 162–170 (1996). doi:10.1109/59.486093
174. McCorquodale, M., Carichner, G., O'Day, J., Pernia, S., Kubba, S., Marsman, E., Kuhn, J., Brown, R.: A 25-MHz self-referenced solid-state frequency source suitable for xo-replacement. IEEE Trans. Circ. Syst. I Reg. Pap. **56**(5), 943–956 (2009). doi:10.1109/TCSI.2009.2016133
175. McCorquodale, M., Gupta, B., Armstrong, W.E., Beaudouin, R., Carichner, G., Chaudhari, P., Fayyaz, N., Gaskin, N., Kuhn, J., Linebarger, D., Marsman, E., O'Day, J., Pernia, S., Senderowicz, D.: A silicon die as a frequency source. In: 2010 IEEE International Frequency Control Symposium (FCS), pp. 103–108 (2010). doi:10.1109/FREQ.2010.5556366
176. McCorquodale, M., Gupta, V.: A history of the development of CMOS oscillators: The dark horse in frequency control. In: Frequency Control and the European Frequency and Time Forum (FCS), 2011 Joint Conference of the IEEE International, pp. 1–6 (2011). doi:10.1109/FCS.2011.5977872
177. McCorquodale, M., Pernia, S., Kubba, S., Carichner, G., O'Day, J., Marsman, E., Kuhn, J., Brown, R.: A 25 MHz all-CMOS reference clock generator for xo-replacement in serial wire interfaces. In: IEEE International Symposium on Circuits and Systems, 2008. ISCAS 2008, pp. 2837–2840 (2008). doi:10.1109/ISCAS.2008.4542048
178. McCorquodale, M.S., O'Day, J.D., Pernia, S.M., Carichner, G.A., Kubba, S., Brown, R.B.: A monolithic and self-referenced RF LC clock generator compliant with usb 2.0. IEEE J. Solid State Cir. **42**(2), 385–399 (2007). doi:10.1109/JSSC.2006.883337
179. McCreary, J.: Matching properties, and voltage and temperature dependence of mos capacitors. IEEE J. Solid State Circ. **16**(6), 608–616 (1981). doi:10.1109/JSSC.1981.1051651
180. McNeill, J.: Jitter in ring oscillators. IEEE J. Solid-State Circ. **32**(6), 870–879 (1997). doi:10.1109/4.585289
181. McNeill, J.A., Ricketts, D.S.: The Designer's Guide to Jitter in Ring Oscillators. Springer, Berlin (2009)
182. Mercier, P., Daly, D., Chandrakasan, A.: A 19pj/pulse UWB transmitter with dual capacitively-coupled digital power amplifiers. In: Radio Frequency Integrated Circuits Symposium, 2008. RFIC 2008. IEEE, pp. 47–50 (2008). doi:10.1109/RFIC.2008.4561383

183. Mercier, P.P., Daly, D.C., Chandrakasan, A.P.: An energy-efficient all-digital UWB transmitter employing dual capacitively-coupled pulse-shaping drivers. IEEE J. Solid State Circ. **44**(6), 1679–1688 (2009)
184. Mernyei, F., Darrer, F., Pardoen, M., Sibrai, A.: Reducing the substrate losses of RF integrated inductors. Microwave and Guided Wave Lett. IEEE **8**(9), 300–301 (1998). doi:10.1109/75.720461
185. Mukherjee, J., Roblin, P., Akhtar, S.: An analytic circuit-based model for white and flicker LC oscillators. IEEE Trans. Circ. Syst. I Reg. Pap. **54**(7), 1584–1598 (2007)
186. Namajunas, A., Tamasevicius, A.: Modified wien-bridge oscillator for chaos. Electron. Lett. **31**(5), 335–336 (1995). doi:10.1049/el:19950250
187. Navid, R., Lee, T.H., Dutton, R.W.: Minimum achievable phase noise of RC oscillators. IEEE J. Solid State Circ **40**(3), 630–637 (2005)
188. Nicolson, S., Phang, K.: Improvements in biasing and compensation of CMOS opamps. In: Proceedings of the 2004 International Symposium on Circuits and Systems, 2004. ISCAS '04, vol. 1, pp. I-665–I-6658 (2004). doi:10.1109/ISCAS.2004.1328282
189. Niknejad, A.M.: Injection locking, eecs 242 lecture 26 (2013). http://rfic.eecs.berkeley.edu/~niknejad/ee242/pdf/eecs242_lect26_injectionlocking.pdf
190. NIST, U.N.I.F.S., Technology: Causes of noise sources in a signal source. tf.nist.gov/phase/Properties/twelve.htm
191. Nyquist, H.: Thermal agitation of electric charge in conductors. Phys. Rev. **32**(1), 110–113 (1928)
192. Olmos, A.: A temperature compensated fully trimmable on-chip IC oscillator. Proceedings. 16th Symposium on Integrated Circuits and Systems Design, 2003. SBCCI 2003. pp. 181–186 (2003)
193. Organization: S.A.I.: Serial ATA revision 3.0, June 2, 2009 gold revision (2009)
194. PIC18F2525/2620/4525/4620 data sheet
195. Paavola, M., Laiho, M., Saukoski, M., Halonen, K.: A 3 μW, 2 MHz CMOS frequency reference for capacitive sensor applications. 2006 IEEE International Symposium on Circuits and Systems, 2006. ISCAS 2006. Proceedings. 4 pp. (2006). doi:10.1109/ISCAS.2006.1693602
196. Paciorek, L.J.: Injection locking of oscillators. Proceedings of the IEEE **53**(11), 1723–1727 (1965). doi:10.1109/PROC.1965.4345
197. Paidimarri, A., Griffith, D., Wang, A., Chandrakasan, A., Burra, G.: A 120nw 18.5khz rc oscillator with comparator offset cancellation for $\pm$0.25 temperature stability. In: Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2013 IEEE International, pp. 184–185 (2013). doi:10.1109/ISSCC.2013.6487692
198. Pelgrom, M., Duinmaijer, A., Welbers, A.: Matching properties of MOS transistors. Solid-State Circuits, IEEE Journal of 24(5), 1433–1439 (1989). doi:10.1109/JSSC.1989.572629
199. Pletcher, N., Gambini, S., Rabaey, J.: A 2ghz 52 μw wake-up receiver with -72dbm sensitivity using uncertain-if architecture. In: Solid-State Circuits Conference, 2008. ISSCC 2008. Digest of Technical Papers. IEEE International, pp. 524–633 (2008). doi:10.1109/ISSCC.2008.4523288
200. Pletcher, N., Gambini, S., Rabaey, J.: A 52 μ w wake-up receiver with $-$72 dbm sensitivity using an uncertain-if architecture. Solid-State Circuits, IEEE Journal of 44(1), 269–280 (2009). doi:10.1109/JSSC.2008.2007438
201. Pletcher, N.M.: Ultra-low power wake-up receivers for wireless sensor networks. ProQuest (2008).
202. Pogge, R.W.: Real-world relativity: The gps navigation system (2009). http://www.astronomy.ohio-state.edu/~pogge/Ast162/Unit5/gps.html
203. Poore, R.: Phase noise and jitter. Agilent EEs of EDA (May 2001)
204. Qian, L., Yeh, W.C.S.: Inductor with cobalt/nickel core for integrated circuit structure with high inductance and high q-factor (2000). US Patent 6,166,422
205. Rabaey, J.: The swarm at the edge of the cloud—a new perspective on wireless. In: VLSI Circuits (VLSIC), 2011 Symposium on, pp. 6–8 (2011)

206. Rabaey, J.M., Chandrakasan, A.P., Nikolic, B.: Digital integrated circuits, vol. 2. Prentice hall Englewood Cliffs (2002)
207. Radiom, S., Baghaei-Nejad, M., Aghdam, K., Vandenbosch, G., Zheng, L.R., Gielen, G.G.E.: Far-field on-chip antennas monolithically integrated in a wireless-powered 5.8-ghz downlink/uwb uplink rfid tag in 0.18-μm standard cmos. Solid-State Circuits, IEEE Journal of 45(9), 1746–1758 (2010). doi:10.1109/JSSC.2010.2055630
208. Radiom, S., Baghaei-Nejad, M., Vandenbosch, G., Zheng, L.R., Gielen, G.: Far-field rf powering system for rfid and implantable devices with monolithically integrated on-chip antenna. In: Radio Frequency Integrated Circuits Symposium (RFIC), 2010 IEEE, pp. 113–116 (2010). doi:10.1109/RFIC.2010.5477377
209. Radiom, S., Enayati, A., Vandenbosch, G., De Raedt, W., Gielen, G.G.E.: Miniaturization of a bow-tie antenna for a pulsed-uwb transceiver in the 300–960 mhz band. In: Antennas and Propagation, 2009. EuCAP 2009. 3rd European Conference on, pp. 3315–3317 (2009)
210. Ramirez, F., Ponton, M., Sancho, S., Suarez, A.: Phase-noise analysis of injection-locked oscillators and analog frequency dividers. Microwave Theory and Techniques, IEEE Transactions on 56(2), 393–407 (2008). doi:10.1109/TMTT.2007.914375
211. Razavi, B.: A study of phase noise in CMOS oscillators. Solid-State Circuits, IEEE Journal of 31(3), 331–343 (1996). doi:10.1109/4.494195
212. Razavi, B.: Design of Analog CMOS Integrated Circuits. McGraw-Hill (2001)
213. Razavi, B.: A study of injection locking and pulling in oscillators. Solid-State Circuits, IEEE Journal of 39(9), 1415–1424 (2004). doi:10.1109/JSSC.2004.831608
214. Reimbold, G., Gentil, P.: White noise of mos transistors operating in weak inversion. Electron Devices, IEEE Transactions on 29(11), 1722–1725 (1982). doi:10.1109/T-ED.1982.21016
215. Risch, L.: Pushing cmos beyond the roadmap. In: Solid-State Circuits Conference, 2005. ESSCIRC 2005. Proceedings of the 31st European, pp. 63–68 (2005). doi:10.1109/ESSCIR.2005.1541558
216. Rommes, J., Sleijpen, G.L.G.: Convergence of the Dominant Pole Algorythm and Reyleigh Quotient Iteration. SIAM Journal on Matrix Analysis and Applications 30(1), 346–363 (2008). doi:10.1137/060671401
217. Rutman, J.: Characterization of phase and frequency instabilities in precision frequency sources: Fifteen years of progress. Proceedings of the IEEE 66(9), 1048–1075 (1978). doi:10.1109/PROC.1978.11080
218. Ryckaert, J., Verhelst, M., Badaroglu, M., D'Amico, S., De Heyn, V., Desset, C., Nuzzo, P., Van Poucke, B., Wambacq, P., Baschirotto, A., Dehaene, W., Van der Plas, G.: A CMOS Ultra-Wideband Receiver for Low Data-Rate Communication. Solid-State Circuits, IEEE Journal of 42(11), 2515–2527 (2007). doi:10.1109/JSSC.2007.907195
219. Sansen, W.: Analog Design Essentials. Springer (2006)
220. Sayed, D., Dessouky, M.: Automatic generation of common-centroid capacitor arrays with arbitrary capacitor ratio. In: Design, Automation and Test in Europe Conference and Exhibition, 2002. Proceedings, pp. 576–580 (2002). doi:10.1109/DATE.2002.998358
221. Schaefer, C.: Rfid in 2011...and beyond (2011). http://www.rfidjournal.net/masterPresentations/rfid_latam2011/np/schaefer_1129_340.pdf
222. Schaller, R.R.: Moore's law: past, present and future. Spectrum, IEEE **34**(6), 52–59 (1997)
223. Schutz, B.: Gravity from the ground up: An Introductory guide to gravity and general relativity. Cambridge University Press (2003)
224. Sebastiano, F., Breems, L., Makinwa, K., Drago, S., Leenaerts, D., Nauta, B.: A low-voltage mobility-based frequency reference for crystal-less ULP radios. Solid-State Circuits Conference, 2008. ESSCIRC 2008. 34th European pp. 306–309 (2008). doi:10.1109/ESSCIRC.2008.4681853
225. Sebastiano, F., Breems, L., Makinwa, K.A.A., Drago, S., Leenaerts, D., Nauta, B.: A low-voltage mobility-based frequency reference for crystal-less ulp radios. Solid-State Circuits, IEEE Journal of 44(7), 2002–2009 (2009). doi:10.1109/JSSC.2009.2020247
226. Sebastiano, F., Breems, L., Makinwa, K.A.A., Drago, S., Leenaerts, D., Nauta, B.: A 1.2-v 10-μw npn-based temperature sensor in 65-nm cmos with an inaccuracy of 0.2 °C (3 σ) from

−70 °C to 125 °C. IEEE J Solid-State Circuits 45(12), 2591–2601 (2010). doi:10.1109/JSSC.2010.2076610
227. Sebastiano, F., Breems, L., Makinwa, K.A.A., Drago, S., Leenaerts, D., Nauta, B.: A 65-nm cmos temperature-compensated mobility-based frequency reference for wireless sensor networks. IEEE J Solid-State Circuits 46(7), 1544–1552 (2011). doi:10.1109/JSSC.2011.2143630
228. Sheng, H., Orlik, P., Haimovich, A., Cimini, L., Zhang, J.: On the spectral and power requirements for ultra-wideband transmission. In: Communications, 2003. ICC '03. IEEE International Conference on, vol. 1, pp. 738–742 (2003). doi:10.1109/ICC.2003.1204271
229. Sheng, W., Xia, B., Emira, A., Xin, C., Valero-Lopez, A., Moon, S.T., Sanchez-Sinencio, E.: A 3-v, 0.35- μm cmos bluetooth receiver ic. Solid-State Circuits, IEEE Journal of 38(1), 30–42 (2003). doi:10.1109/JSSC.2002.806277
230. Shumakher, E., Eisenstein, G.: On the noise properties of injection-locked oscillators. Microwave Theory and Techniques, IEEE Transactions on 52(5), 1523–1537 (2004). doi:10.1109/TMTT.2004.827035
231. Shyu, Y.S., Wu, J.C.: A process and temperature compensated ring oscillator. ASICs, 1999. AP-ASIC '99. The First IEEE Asia Pacific Conference on pp. 283–286 (1999). doi:10.1109/APASIC.1999.824084
232. Siegman, A.E.: Lasers. University Science Books - Mill Valley, CA (1986)
233. Singularity.com: The singularity is near—when humans transcend biology (2014). http://www.singularity.com/charts/page67.html
234. Sinoussi, N., Hamed, A., Essam, M., El-Kholy, A., Hassanein, A., Saeed, M., Helmy, A., Ahmed, A.: A single LC tank self-compensated CMOS oscillator with frequency stability of ±100ppm from −40 °C to 85 °C. In: Frequency Control Symposium (FCS), 2012 IEEE International, pp. 1–5 (2012). doi:10.1109/FCS.2012.6243676
235. Skotnicki, T., Hutchby, J.A., King, T.J., Wong, H.S., Boeuf, F.: The end of CMOS scaling: toward the introduction of new materials and structural changes to improve mosfet performance. Circ. Dev. Mag. IEEE **21**(1), 16–26 (2005)
236. Soltani, N., Yuan, F.: Nonharmonic injection-locked phase-locked loops with applications in remote frequency calibration of passive wireless transponders. IEEE Trans. Circ. Syst. I Reg. Pap. **57**(9), 2381–2393 (2010). doi:10.1109/TCSI.2010.2046228
237. Sparkmuseum: Marconi magnetic detector (2012). http://www.sparkmuseum.com/MAGGIE.HTM
238. Srisuchinwong, B., Trung, N.V.: An integratable current-tunable R-L oscillator. In: 1995 URSI International Symposium on Signals, Systems, and Electronics, 1995. ISSSE '95, Proceedings, pp. 541–544 (1995). doi:10.1109/ISSSE.1995.498051
239. Stanton, T.: Removing the accuracy drift and synchronising the GPS clocks using true relativity and the universal clock (2009). http://www.gsjournal.net/old/science/stanton2.pdf
240. Stork, H.: Economics of CMOS scaling (2005). http://www.etv.tudelft.nl/maxwell/9/1/column.pdf
241. Stork, H.: Economies of CMOS scaling (2005). http://www.nist.gov/pml/div683/conference/upload/Stork_2005.pdf
242. Strogatz, S.: Nonlinear dynamics and chaos: with applications to physics, biology, chemistry, and engineering. Studies in nonlinearity. Sarat Book House (1994). http://books.google.be/books?id=PHmED2xxrE8C
243. Sudevalayam, S., Kulkarni, P.: Energy harvesting sensor nodes: survey and implications. Commun. Surv. Tutorials IEEE **13**(3), 443–461 (2011). doi:10.1109/SURV.2011.060710.00094
244. Sundaresan, K., Allen, P., Ayazi, F.: Process and temperature compensation in a 7-MHz CMOS clock oscillator. IEEE J. Solid State Circ. **41**(2), 433–442 (2006). doi:10.1109/JSSC.2005.863149
245. Svelto, F., Deantoni, S., Castello, R.: A 1.3 GHz low-phase noise fully tunable CMOS LC VCO. IEEE J. Solid State Circ. **35**(3), 356–361 (2000). doi:10.1109/4.826817

246. Székely, V.: Thermal monitoring of microelectronic structures. Microelectron. J. **25**(3), 157–170 (1994)
247. Tanaka, K., Kuramochi, Y., Kurashina, T., Okada, K., Matsuzawa, A.: A 0.026 mm^2 capacitance-to-digital converter for biotelemetry applications using a charge redistribution technique. In: IEEE Asian Solid-State Circuits Conference, 2007. ASSCC '07, pp. 244–247 (2007). doi:10.1109/ASSCC.2007.4425776
248. Tesla, N.: Method of operating arc lamps (1891). US Patent 447,920
249. Tesla, N.: Apparatus for transmitting electrical energy (1914). US Patent 1,119,732
250. Tokunaga, Y., Sakiyama, S., Matsumoto, A., Dosho, S.: An on-chip CMOS relaxation oscillator with power averaging feedback using a reference proportional to supply voltage. IEEE International Solid-State Circuits Conference, 2009. ISSCC 2009. pp. 404–406 (2009)
251. Tokunaga, Y., Sakiyama, S., Matsumoto, A., Dosho, S.: An on-chip CMOS relaxation oscillator with voltage averaging feedback. IEEE J. Solid State Circ. **45**(6), 1150–1158 (2010). doi:10.1109/JSSC.2010.2048732
252. Tsai, M.D., Cho, Y.H., Wang, H.: A 5-GHz low phase noise differential colpitts CMOS VCO. Microw. Wireless Compon. Lett. IEEE **15**(5), 327–329 (2005)
253. Tsividis, Y., McAndrew, C.: Operation and Modeling of the MOS Transistor, vol. 2. Oxford University Press, New York (1999)
254. Tsubaki, K., Hirose, T., Osaki, Y., Shiga, S., Kuroki, N., Numa, M.: A 6.66-khz, 940-nw, 56ppm/°c, fully on-chip PVT variation tolerant CMOS relaxation oscillator. In: 2012 19th IEEE International Conference on Electronics, Circuits and Systems (ICECS), pp. 97–100 (2012). doi:10.1109/ICECS.2012.6463790
255. Tuttlebee, W.: Software-defined radio: facets of a developing technology. Pers. Commun. IEEE 6(2), 38–44 (1999). doi:10.1109/98.760422
256. Ueda, Y., Akamatsu, N.: Chaotically transitional phenomena in the forced negative-resistance oscillator. IEEE Trans. Circ. Syst. **28**(3), 217–224 (1981). doi:10.1109/TCS.1981.1084975
257. Ueno, K., Asai, T., Amemiya, Y.: A 30-MHz, 90-ppm/°c fully-integrated clock reference generator with frequency-locked loop. In: Proceedings of ESSCIRC, 2009. ESSCIRC '09, pp. 392–395 (2009). doi:10.1109/ESSCIRC.2009.5325940
258. USB30: 3.0 specification. Hewlett-Packard Company, Intel Corporation, Microsoft Corporation, NEC Corporation, ST-NXP Wireless, Texas Intruments, rev 1 (2008). www.usb.org
259. Vadasz, L., Grove, A.: Temperature dependence of mos transistor characteristics below saturation. IEEE Trans. Electron Dev. **13**(12), 863–866 (1966). doi:10.1109/T-ED.1966.15860
260. Van Breussegem, T.: Monolithic capacitive CMOS DC–DC converters (monolitische capacitieve CMOS DC–DC convertoren). status: published (2012)
261. Van Helleputte, N.: An ultra-low-power complex analog correlating receiver architecture for UWB impulse radio receivers. status: published (2008)
262. Van Helleputte, N., Verhelst, M., Dehaene, W., Gielen, G.: A reconfigurable, 130 nm CMOS 108 pj/pulse, fully integrated IR-UWB receiver for communication and precise ranging. IEEE J. Solid State Circ. **45**(1), 69–83 (2010)
263. Van Rethy, J., Danneels, H., De Smedt, V., Dehaene, W., Gielen, G.: An energy-efficient BBPLL-based force-balanced wheatstone bridge sensor-to-digital interface in 130 nm CMOS. In: Solid State Circuits Conference (A-SSCC), 2012 IEEE Asian, pp. 41–44 (2012)
264. Van Rethy, J., Danneels, H., De Smedt, V., Dehaene, W., Gielen, G.: Supply-noise-resilient design of a bbpll-based force-balanced wheatstone bridge interface in 130-nm CMOS. IEEE J. Solid State Circ. **48**(11), 2618–2627 (2013). doi:10.1109/JSSC.2013.2274831
265. Van Rethy, J., Danneels, H., De Smedt, V., Gielen, G., Dehaene, W.: A low-power and low-vltage bbpll-based sensor interface in 130 nm CMOS for wireless sensor networks. In: DATE 2013, Grenoble, France, pp. 1431–1435 (2013)
266. Van Rethy, J., Danneels, H., Gielen, G.: Performance analysis of energy-efficient bbpll-based sensor-to-digital converters. IEEE Trans. Circ. Syst. I Reg. Pap. **60**(8), 2130–2138 (2013). doi:10.1109/TCSI.2013.2239097
267. Van Rethy, J., De Smedt, V., Gielen, G., Dehaene, W.: Towards energy-efficient CMOS integrated sensor-to-digital interface circuits. In: AACD '14, Workshop on Advances in Analog Circuit Design, 2014 (2014)

268. Van Rethy, J., Gielen, G.: An energy-efficient capacitance-controlled oscillator-based sensor interface for mems sensors. In: 2013 IEEE Asian Solid State Circuits Conference (A-SSCC), pp. 443–446 (2013)
269. Vanassche, P., Gielen, G., Sansen, W.: On the difference between two widely publicized methods for analyzing oscillator phase behavior. In: Proceedings of the 2002 IEEE/ACM International Conference on Computer-aided Design, pp. 229–233. ACM (2002)
270. Vannerson, E., Smith, K.: Fast amplitude stabilization of an RC oscillator. IEEE J. Solid State Circ. **9**(4), 176–179 (1974)
271. Verhelst, M., Dehaene, W.: System design of an ultra-low power, low data rate, pulsed UWB receiver in the 0–960 MHz band. In: 2005 IEEE International Conference on Communications, 2005. ICC 2005, vol. 4, pp. 2812–2817 (2005). doi:10.1109/ICC.2005.1494864
272. Verhelst, M., Dehaene, W.: A flexible, ultra-low-energy 35 pj/pulse digital back-end for a QAC ir-uwb receiver. IEEE J. Solid State Circ. **43**(7), 1677–1687 (2008). doi:10.1109/JSSC.2008.922711
273. Verhelst, M., Dehaene, W.: Energy Scalable Radio Design: For Pulsed UWB Communication and Ranging. Springer, Berlin (2009)
274. Verhelst, M., Van Helleputte, N., Gielen, G., Dehaene, W.: A reconfigurable, 0.13 um CMOS110pj/pulse, fully integrated IR-UWB receiver for communication and sub-cm ranging. In: Solid-State Circuits Conference—Digest of Technical Papers, 2009. ISSCC 2009. IEEE International, pp. 250–251, 251a (2009). doi:10.1109/ISSCC.2009.4977402
275. Vilas Boas, A., Soldera, J., Olmos, A.: A 1.8 V supply multi-frequency digitally trimmable on-chip IC oscillator with low-voltage detection capability. Integrated Circuits and Systems Design, 2004. SBCCI 2004. pp. 44–48 (2004)
276. Visualisations, C.: The internet of things (2011). http://share.cisco.com/internet-of-things.html
277. Vittoz, E.: Low-power design: ways to approach the limits. In: 1994 IEEE International Solid-State Circuits Conference, 1994. Digest of Technical Papers. 41st ISSCC, pp. 14–18 (1994). doi:10.1109/ISSCC.1994.344744
278. Vittoz, E., Degrauwe, M., Bitz, S.: High-performance crystal oscillator circuits: theory and application. IEEE J. Solid State Circ. **23**(3), 774–783 (1988). doi:10.1109/4.318
279. Volkaerts, W., Marien, B., Danneels, H., De Smedt, V., Reynaert, P., Dehaene, W., Gielen, G.: A 0.5 v–1.4 v supply-independent frequency-based analog-to-digital converter with fast start-up time for wireless sensor networks. In: Proceedings of 2010 IEEE International Symposium on Circuits and Systems (ISCAS), pp. 3096–3099 (2010). doi:10.1109/ISCAS.2010.5537971
280. Walden, R.: Analog-to-digital converter survey and analysis. IEEE J. Sel. Areas Commun. **17**(4), 539–550 (1999). doi:10.1109/49.761034
281. Wang, H.: A 9.8 GHz back-gate tuned VCO in 0.35 μm CMOS. In: Solid-State Circuits Conference, 1999. Digest of Technical Papers. ISSCC. 1999 IEEE International, pp. 406–407. IEEE (1999)
282. Weigandt, T.C., Kim, B., Gray, P.R.: Analysis of timing jitter in CMOS ring oscillators. In: 1994 IEEE International Symposium on Circuits and Systems, 1994. ISCAS'94, vol. 4, pp. 27–30. IEEE (1994)
283. Van der Wel, A., Klumperink, E., Gierkink, S., Wassenaar, R., Wallinga, H.: Mosfet 1/f noise measurement under switched bias conditions. Electron Dev. Lett. IEEE **21**(1), 43–46 (2000)
284. Wens, M.: Monolithic inductive CMOS DC–DC converters: theoretical study & implementation (monolitische inductieve cmos DC–DC convertoren: Theoretische studie & implementatie). status: published (2010)
285. Wens, M., Cornelissens, K., Steyaert, M.: A fully-integrated 0.18 um CMOS DC–DC step-up converter, using a bondwire spiral inductor. In: ESSCIRC 2007, pp. 268–271 (2007). doi:10.1109/ESSCIRC.2007.4430295
286. Wentzloff, D., Chandrakasan, A.: Gaussian pulse generators for subbanded ultra-wideband transmitters. IEEE Trans. Microw. Theory Tech 54(4), 1647–1655 (2006). doi:10.1109/TMTT.2006.872053

287. Wikipedia: Cat's-whisker detector (2012). http://en.wikipedia.org/wiki/Cat's-whisker_detector
288. Wikipedia: Eniac (2012). http://en.wikipedia.org/wiki/ENIAC
289. Wikipedia: History of radar (2012). http://en.wikipedia.org/wiki/History_of_radar
290. Wikipedia: Leon theremin (2012). http://en.wikipedia.org/wiki/L%C3%A9on_Theremin
291. Wikipedia: Nikola tesla (2012). http://en.wikipedia.org/wiki/Nikola_Tesla
292. Wikipedia: Thing (listening device) (2012). http://en.wikipedia.org/wiki/Thing_(listening_device)
293. Wikipedia: Vacuum tube (2012). http://en.wikipedia.org/wiki/Vacuum_tube
294. Wikipedia: Amplitude modulation (2013). http://en.wikipedia.org/wiki/Amplitude_modulation
295. Wikipedia: Clock drift (2013). http://en.wikipedia.org/wiki/Clock_drift
296. Wikipedia: Edwin Howard Armstrong (2013). http://en.wikipedia.org/wiki/Edwin_Howard_Armstrong
297. Wikipedia: Gauss's law (2013). http://en.wikipedia.org/wiki/Gauss's_law
298. Wikipedia: Guglielmo marconi (2013). http://en.wikipedia.org/wiki/Guglielmo_Marconi
299. Wikipedia: History of the transistor (2013). http://en.wikipedia.org/wiki/History_of_the_transistor
300. Wikipedia: Invention of radio (2013). http://en.wikipedia.org/wiki/Invention_of_radio
301. Wikipedia: Invention of the Integrated Circuit (2013). http://en.wikipedia.org/wiki/Invention_of_the_integrated_circuit
302. Wikipedia: Magnetic detector (2013). http://en.wikipedia.org/wiki/Magnetic_detector
303. Wikipedia: Max wien (2013). http://en.wikipedia.org/wiki/Max_Wien
304. Wikipedia: Michael faraday (2013). http://en.wikipedia.org/wiki/Michael_Faraday
305. Wikipedia: Multivibrator (2013). http://en.wikipedia.org/wiki/Multivibrator
306. Wikipedia: Radio frequency identification (2013). http://en.wikipedia.org/wiki/Radio-frequency_identification
307. Wikipedia: Regenerative circuit (2013). http://en.wikipedia.org/wiki/Regenerative_circuit
308. Wikipedia: RMS titanic (2013). http://en.wikipedia.org/wiki/RMS_Titanic
309. Wikipedia: Spark-gap transmitter (2013). http://en.wikipedia.org/wiki/Spark-gap_transmitter
310. Wikipedia: Time (2013). http://en.wikipedia.org/wiki/Time
311. Wikipedia: Timeline of radio (2013). http://en.wikipedia.org/wiki/Timeline_of_radio
312. Wikipedia: Transistor radio (2013). http://en.wikipedia.org/wiki/Transistor_radio
313. Wikipedia: Wireless power (2013). http://en.wikipedia.org/wiki/Wireless_power
314. Wikipedia: Wireless sensor network (2013). http://en.wikipedia.org/wiki/Wireless_sensor_network
315. Wikipedia: James clerk maxwell (2014). http://en.wikipedia.org/wiki/James_Clerk_Maxwell
316. Williams, J.: Max wien, mr. hewlett, and a rainy sunday afternoon. In: Jim, W (ed.) Analog Circuit Design: Art, Science, and Personalities. Butterworth-Heinemann, Boston, pp. 43–55 (1991)
317. Williamson, T.: Oscillators for microcontrollers. Intel Application Note AP-155 (1983)
318. Wu, N.C., Nystrom, M., Lin, T.R., Yu, H.C.: Challenges to global rfid adoption. Technovation **26**(12), 1317–1323 (2006)
319. Wu, R., Chae, Y., Huijsing, J., Makinwa, K.A.A.: A 20-b 40-mv range read-out IC with 50-nv offset and 0.04 IEEE J. Solid State Circ. **47**(9), 2152–2163 (2012). doi:10.1109/JSSC.2012.2197929
320. Xu, Y.: Receiver architecture and methods for demodulating binary phase shift keying signals (2013). US Patent App. 14/034,426
321. Young, D., Keller, C., Bliss, D., Forsythe, K.: Ultra-wideband (UWB) transmitter location using time difference of arrival (TDOA) techniques. In: Conference Record of the Thirty-Seventh Asilomar Conference on Signals, Systems and Computers, 2004, vol. 2, pp. 1225–1229 (2003). doi:10.1109/ACSSC.2003.1292184

322. Zanchi, A., Bonfanti, A., Levantino, S., Samori, C.: General SSCR vs. cycle-to-cycle jitter relationship with application to the phase noise in PLL. In: 2001 Southwest Symposium on Mixed-Signal Design, 2001. SSMSD, pp. 32–37 (2001). doi:10.1109/SSMSD.2001.914933
323. van der Ziel, A.: On the noise spectra of semi-conductor noise and of flicker effect. Physica **16**(4), 359–372 (1950). doi:10.1016/0031-8914(50)90078-4.http://www.sciencedirect.com/science/article/pii/0031891450900784
324. van der Ziel, A.: Theory of shot noise in junction diodes and junction transistors. Proceedings of the IRE **43**(11), 1639–1646 (1955). doi:10.1109/JRPROC.1955.277990

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